Study of High Speed Buffer Amplifier using Microwind

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ABSTRACT

This paper propose a verilog implementation of high speed buffer amplifier for reduce the quiescent current consumption a current reuse technique is used in the output stage of the buffer amplifier. The proposed buffer amplifier implemented in a 0.25 µA CMOS technology demonstrate that an average value of 0.1 µA static current. The settling time 0.2% of the final voltage is 2 ns under a 30 KΩ resistance and 30 pF capacitance load. The area of buffer amplifier is 23.123 µm * 78.250 µm.

Keywords
Quiescent current, buffer amplifier, CMOS, PMOS, NMOS.

1. INTRODUCTION
An LCD driver is composed of gate drivers, a timing controller, column drivers, and a reference source. The column drivers are important for achieving high speed driving, low-power dissipation and high resolution. There are the hundreds of buffer amplifiers built into a single chip, the buffer amplifier occupy a small die area, and its static power consumption should be small. For the high-resolution displays dot inversion method is used. A Flat-panel displays are employed in battery-powered portable system, the static power consumption of output buffers should be minimized and to extend the battery lifetime.
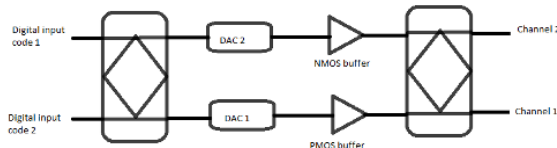

Fig. 1: A Rail-to-Rail Dot-Inversion Driving Scheme

Fig. 1 shows Two channels of driving circuits, in which one channel takes the responsibility for driving positive polarity and another for driving negative polarity, these +ve and −ve polarity are grouped to drive a pair of adjacent column lines. To drive positive-to-negative polarity operation PMOS input buffers are used, and for the transition of negative-to-positive polarity NMOS input buffers are used. The PMOS input buffers have a large discharge capability whereas the NMOS input buffers have small discharge capability. In our work, we combine these two buffers as a two-input/output buffer amplifier. To reduce the quiescent power consumption a current reuse technique is employed in the proposed buffer amplifier. The output buffers must be all driven by a step-wise function, and display pixels are always updated row by row; so, output voltage should be settled within the horizontal scanning time.

2. PROPOSED BUFFER AMPLIFIER
To the reduction of quiescent power dissipation, we combine the NMOS input and PMOS input buffer amplifiers into a two input/ output buffer amplifier and apply current reuse technique is employed in the output stage. Fig. 2 shows the architecture of the proposed two input/output buffer amplifier. It consists an PMOS input and a NMOS input one-stage differential amplifiers, a complementary common source amplifier, M11-M12, and a floating bias circuit, Ib1, Ib2, and M13-M16. Two outputs, out1 and out2, are isolated by M13 and M15. two floating current mirrors are M13-M14 and M15-M16. The quiescent current, I11 and I12, of the complementary common source amplifier, M11-M12, is biased by the two floating current mirrors. That is:

$$I_{11} = I_{12} = I_{b1}\left[1 + \frac{(W/L)_{13}}{(W/L)14} + \frac{(W/L)_{15}}{(W/L)_{16}}\right]$$

where Ib1 = Ib2. Although two additional bias currents, Ib1 and Ib2, are required, they consume smaller currents than that of the complementary common source amplifier.
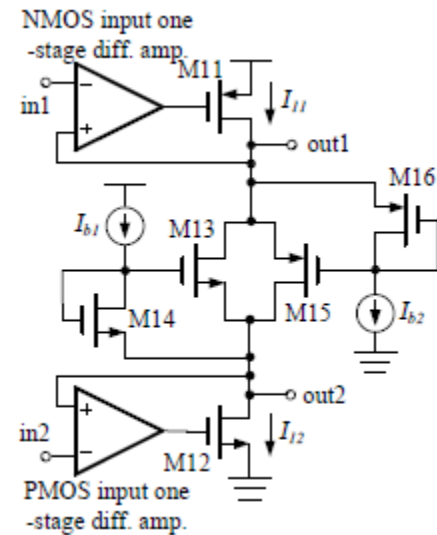

Fig. 2: Architecture of the Proposed Two-Input/Output Buffer Amplifier

Fig. 2 shows the schematic of the proposed buffer amplifier. The NMOS input and PMOS input one-stage differential amplifiers are consisted of M1-M5 and M6-M10, respectively. The capacitors, CC1 – CC4 are the Miller compensation capacitors. In the stable state, the currents flowing in M9 and M10 are both Ib3/2 where Ib3 is the bias current for NMOS input one-stage differential amplifier. The quiescent current of M12 is mirrored from M4. Since the complementary common source amplifier is biased by the floating bias circuit and two one-stage differential amplifiers, the circuit may suffer from a systematic output dc offset voltage. However, the dc offset voltage can be eliminated by sizing the transistors so as to satisfy the following constraint.

$$\frac{I_{b3}}{2}\frac{(W/L)_{11}}{(W/L)_9} = \frac{I_{b4}}{2}\frac{(W/L)_{12}}{(W/L)_4}$$

$$= I_{b1}[1 + \frac{(W/L)_{13}}{(W/L)_{14}} + \frac{(W/L)_{15}}{(W/L)_{16}}]$$

where Ib4 is the bias current for PMOS input one-stage differential amplifier.
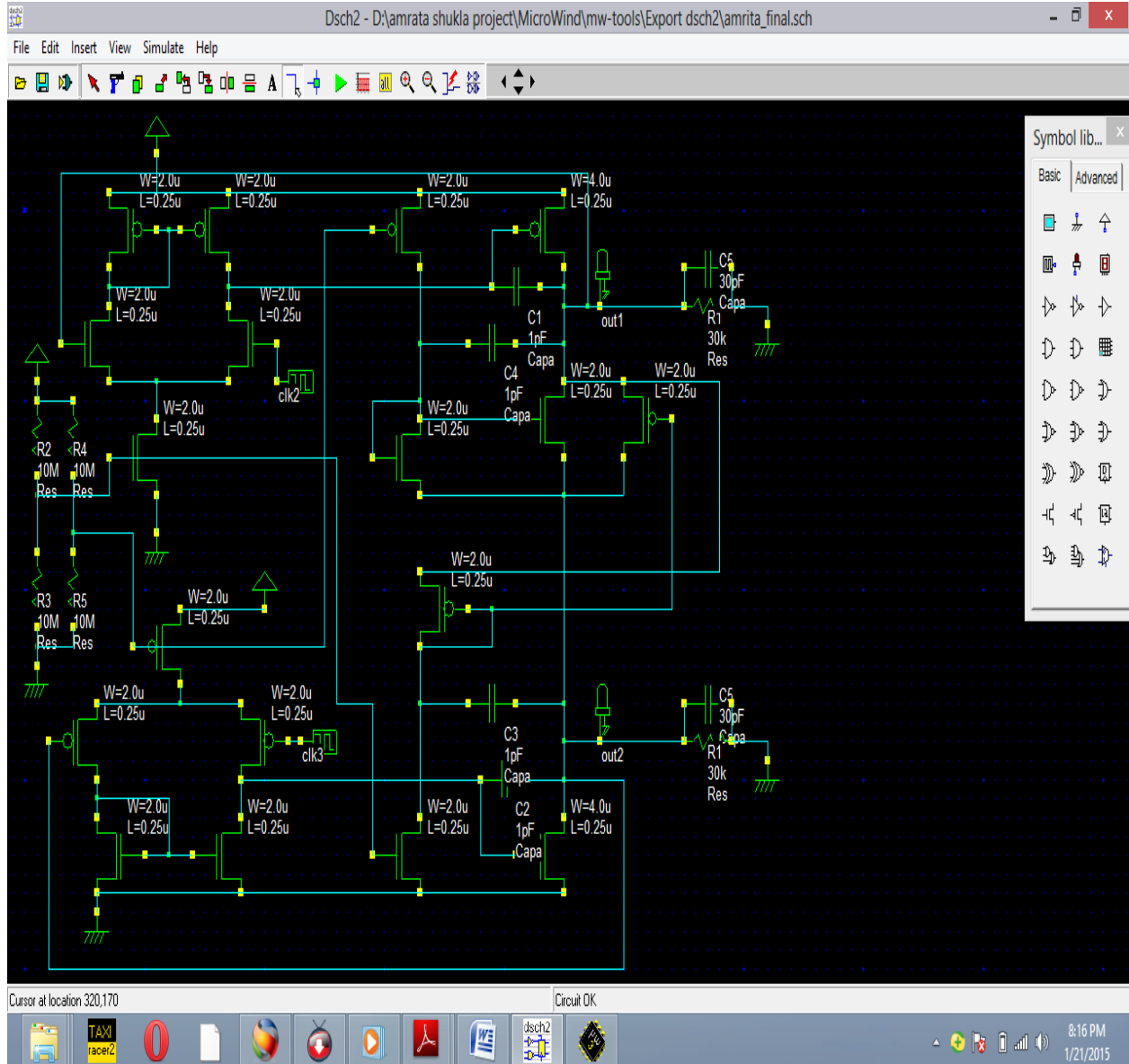

Fig. 3: Schematic circuit dig of the Proposed Buffer Amplifier.

3. METHODOLOGY

Inversion method which alternates the positive and negative polarities between the liquid-crystal cell with respect to a common backside electrode. There are three inversion methods, which are frame, line and dot inversions for LCD driving. The dot inversion method is preferred in the high-resolution displays. A two-stage amplifier requires compensation for stability. Some buffer amplifiers adopt the output node as a dominant pole to achieve enough stability without a Miller capacitance.

However, a charge conservation technique is commonly used in some LCD drivers to reduce the dynamic power Dissipation all column lines are isolated from the buffers. the buffer amplifiers experience no load for a period of time, these amplifiers require the Miller compensation.
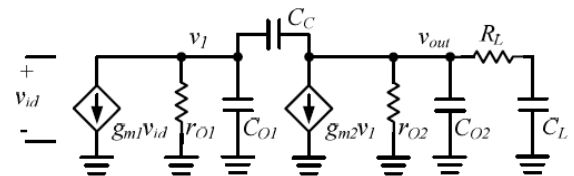

Fig 4 : Equivalent circuit of a typical two-stage op amp

4. MEASUREMENT RESULT

A 6-bit 12 channel LCD column driver with buffer amplifier was designed and fabricated using 0.25-µm CMOS technology. The area of one two-input/output buffer amplifier is 23.12 µm × 78.25 µm. The two-input/output buffer amplifier consumes 0.1 µA static current. The measured o/p waveform with 30 kΩ and 30 pF load when digital data change from 000000 to 111111. Settling time to settle within 0.2%.
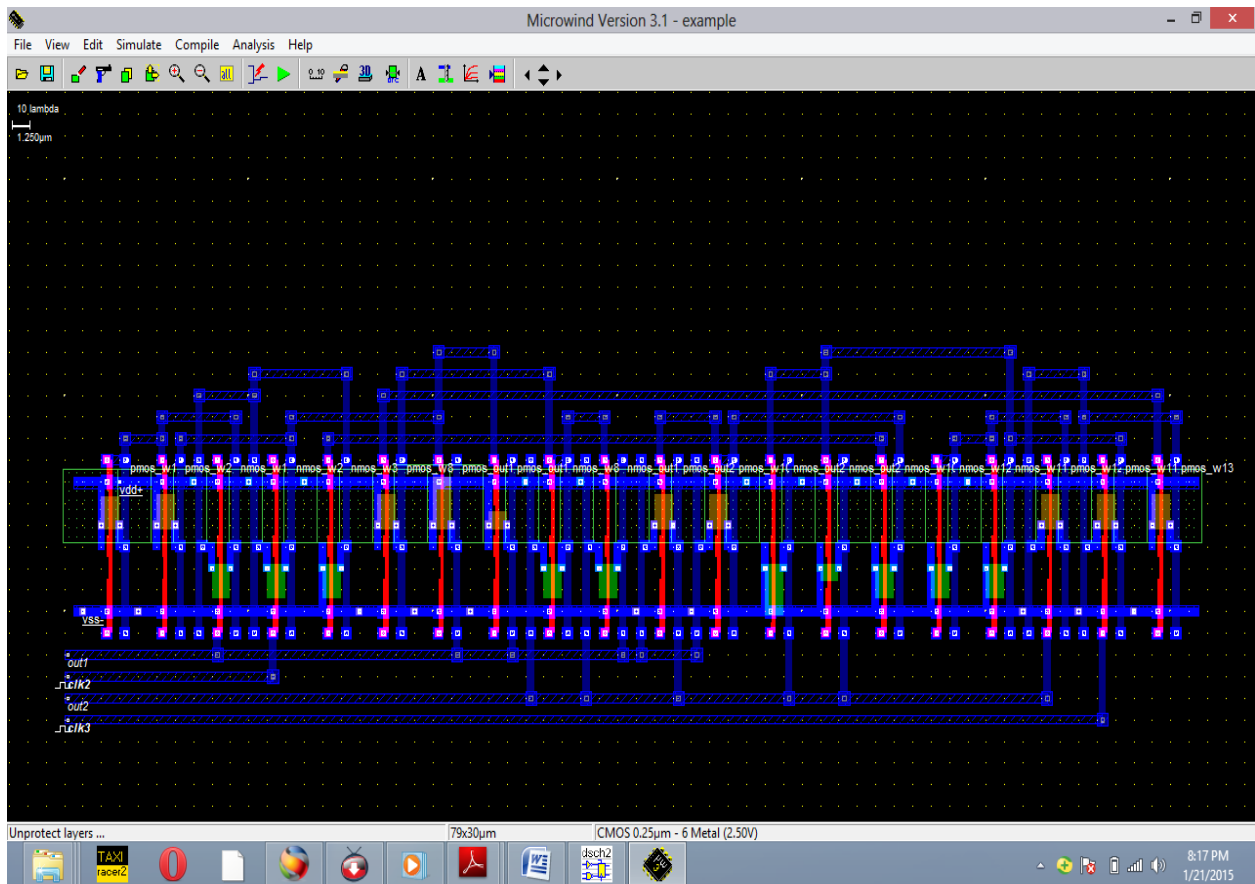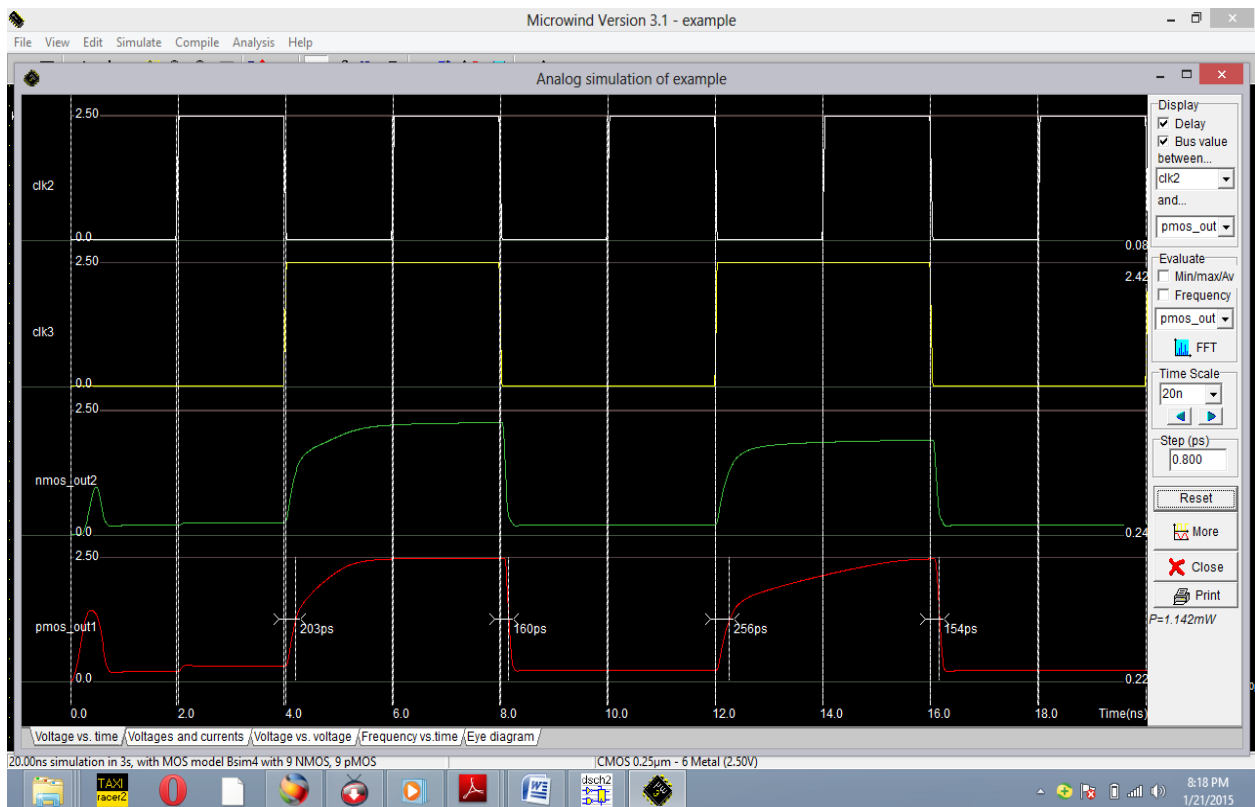
Fig 5: Area of layout
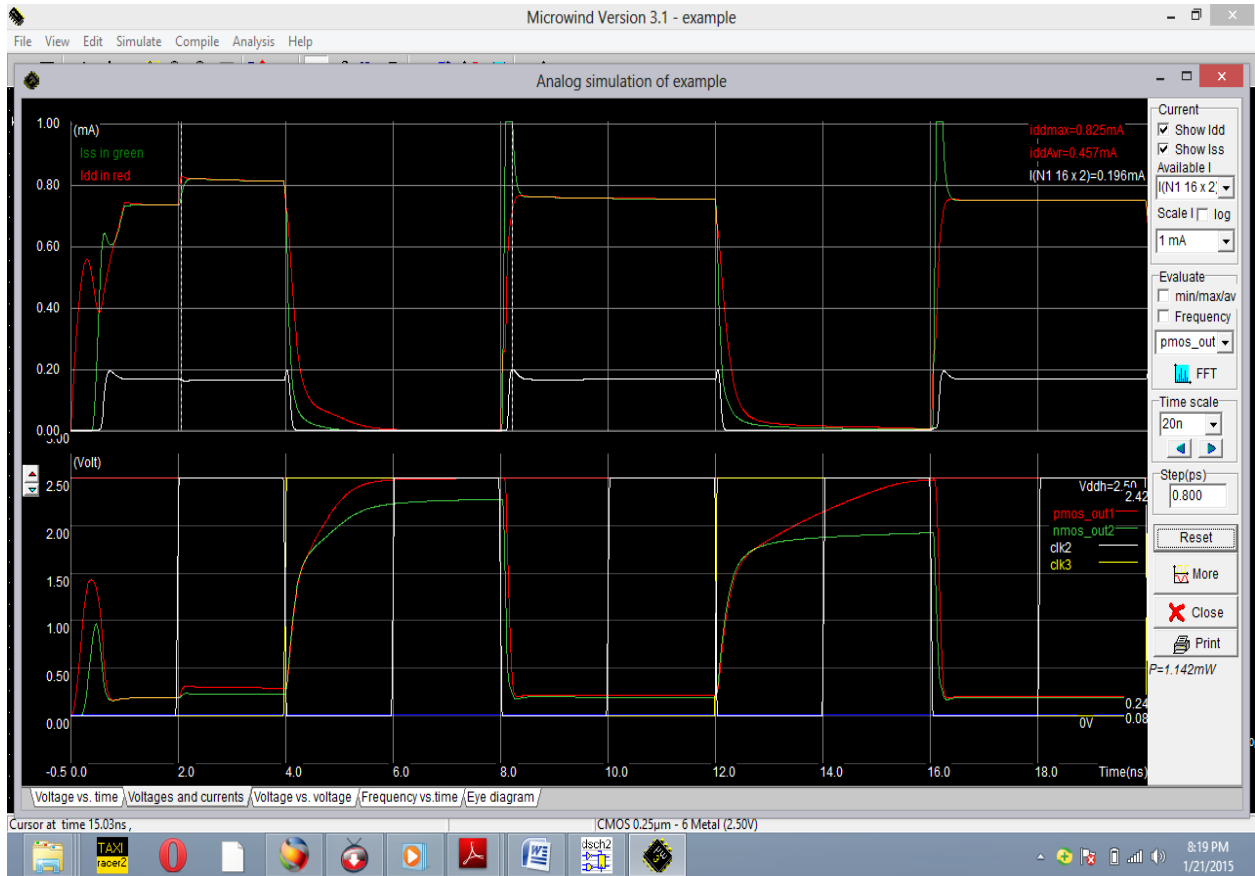
5. ANALOG SIMULATION

Fig 6: Voltage vs time
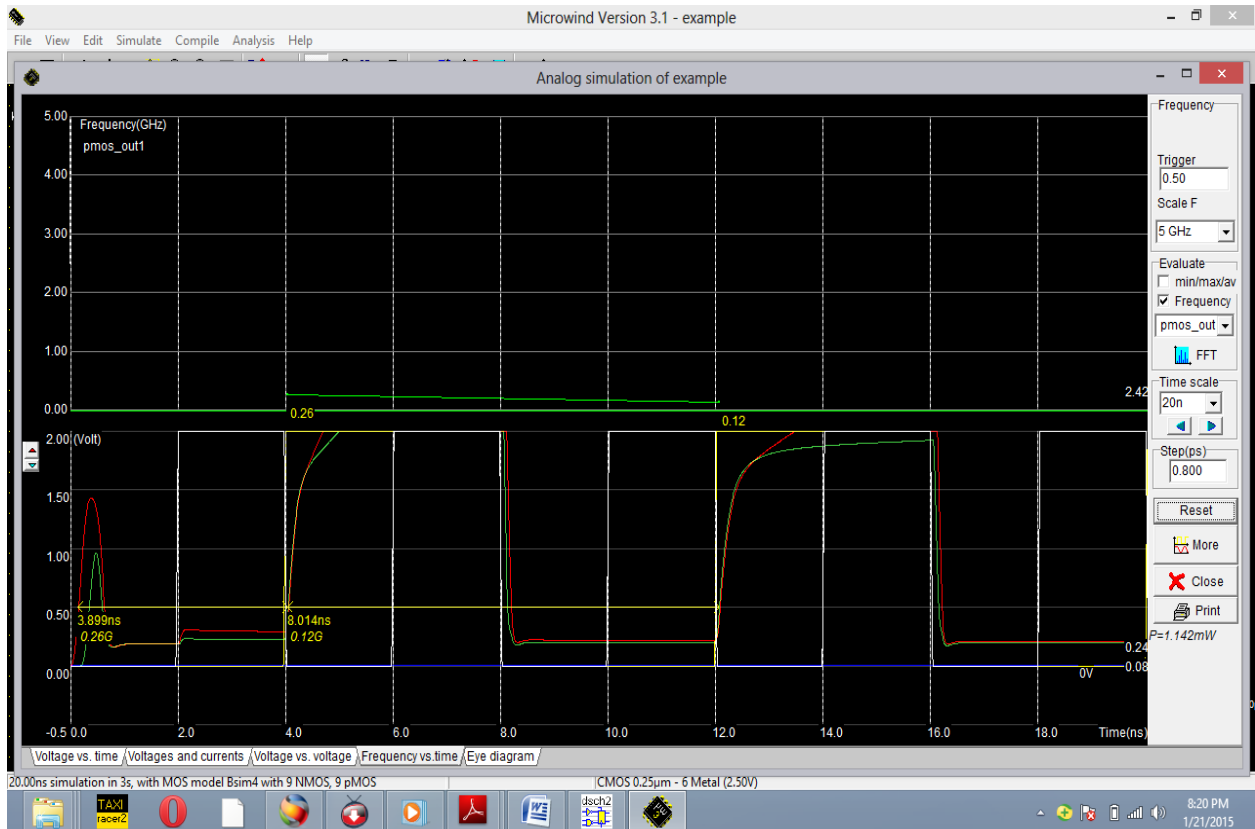
Fig 7: Voltage vs Current

Fig 8: Frequency vs time

Table 1: Performance Comparison

Author	Chih-Wen Lu Ping-Yeh Yin Kuo, Hsuan-Lun Salvatore Pennisi	Davide Marano Gaetano Palumbo Salvatore Pennisi	Arnon Kanjanop and Varakorn Kasemsuwan	Jia-Hui Wang, Jing-Chuan Qiu, Chien-Hung Tsai	Our Work
CMOS Technology	0.35-µm	0.35- µm	0.13-µm	0.35-µm	0.25-µm
Supply Voltage	5 V	3 V	0.7 V	5 V	2.5 V
Quiescent Current	0.6 µA	3 µA	—	3.8 µA	0.1 µA
Loads	R= 30 KΩ C= 30 pF	—	—	—	R= 30 KΩ C= 30 pF
Area	21.5 µm × 190 µm	—	—	—	23.12 µm × 78.25 µm

6. CONCLUSION

This work presents a low-quiescent current two input/output buffer amplifier. A current reuse technique is employed in the output stage of the buffer amplifier to reduce the quiescent current consumption upto 0.1µA. The proposed buffer amplifiers was implemented in a 0.25-µm CMOS technology. The result show that the proposed buffer amplifier is very suitable for dot-inversion LCD column drivers.

In future we reduce the area and quiescent current of the buffer amplifier.

7. REFERENCES

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