

# Comparative Analysis of Low Power 1-Bit CMOS Full Adder at 45 nm Technology

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## ABSTRACT

Design and simulation of conventional CMOS full adder using 45nm technology at specified node has been presented here. This research work shows comparison about post layout simulations of designed low power CMOS full adder. It also explains about performance analysis of optimized low power CMOS full adder at different loads. This design has achieved 63.1nW active power consumption with propagation delay of 0.254ns and having leakage current of 0.798nA at the supply voltage of 0.7V. Cadence's virtuoso tool has been used for circuit design.

## Keywords

Low power CMOS Circuits, 1 bit Full adder, Performance comparison, 45 nm Technology et. al.

## 1. INTRODUCTION

Low power circuits have been major design challenge in VLSI technology. Area, power, cost and delays are the mainly concern parameters for CMOS circuit development. Technology enhancements reduce the area for a single chip and increase the number of transistors on a single dice. High number of transistors on single chip leads to high power dissipation. Power optimization and minimization becomes very useful for reducing high power dissipation and it also helps in long operating life of battery for portable device. Performance of the overall system can be increased by enhancement in the performance of the critical components of a processor used in the ALU like a 1-bit CMOS full adder which is used in the Floating Point Unit, and address generation for cache and memory accesses. Speed of a circuit can be increased by minimization of the delays for basic building block. Hence various works have been done for low power and high speed 1-bit full adder cell with smaller size. 1-bit CMOS full adder is consists of three input block along with two output blocks. Area, regularity, power dissipation, noise immunity, performance and good driving capability are some parameters which effects full adder design. Most of the portable devices are battery operated and should have capability of low power and high throughput requirement. Most generous technique used to reduce power dissipation is decrement in the supply voltage and operate CMOS devices in Sub-threshold region [2]. This study show to new logic based design approach for low power 1-bit CMOS full adder with better driving capability i.e. using Majority function, GDI (Gate Diffusion Input) technique which have the advantages of low power, low delay and low PDP.

## 2. REVIEW OF 1-BIT FULL ADDER TOPOLOGIES

Various different logic styles have been proposed to implement 1-bit adder cells in the literature. All these logic styles have investigated with different approaches realizing adders using CMOS technology, each having its own pros and

cons. Efficient Full adder design involves various issues, to name few of them are low power consumption, performance enhancement, minimum area, noise immunity, regularity and good driving ability. There are two different modes for circuit design i.e. Voltage mode and Current mode, in Voltage mode in a general contains two networks. Each of these networks contains transistors which behave like a switch. Logical "1" is produced by the pull up network and the pull down network is responsible to produce logical "0". In these circuits, a group of switches is connected and the other group is disconnected in every instant. So we need two groups of switches in constructing these gates, which usually have a contrary operation with each other and is dependent to the output function. The CMOS family gates are good example for comprehension of the structure of these circuits [38].

Usually Low-power 1-bit adder cells have been implemented using Static CMOS logic styles. In general, they can be broadly divided into two major categories: the Complementary CMOS and the Pass-Transistor logic circuits. The complementary CMOS (C-CMOS) full adder in Fig. 1 (a) is based on the regular CMOS structure with P type Metal Oxide Semiconductor (pMOS) pull-up and N type Metal Oxide Semiconductor (nMOS) pull-down transistors.

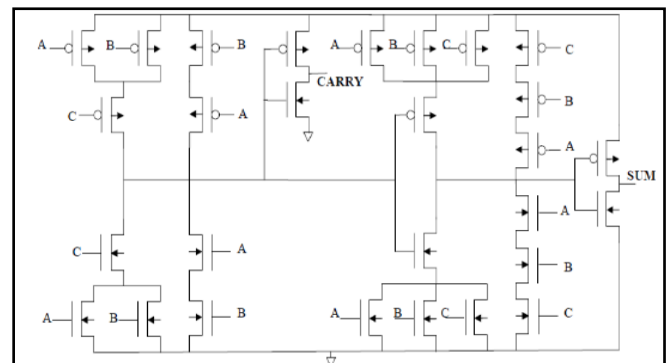


Fig 1(a). C-CMOS full adder cell

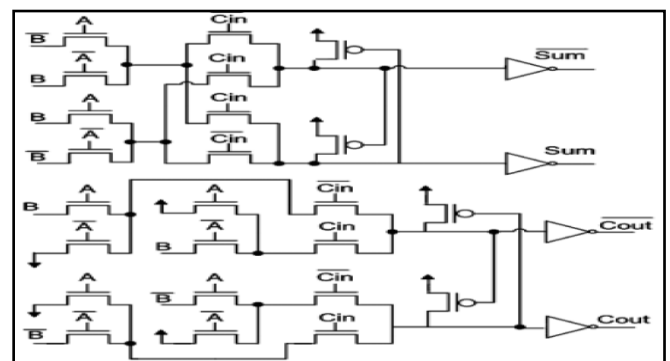


Fig 1(b). CPL Full Adder cell

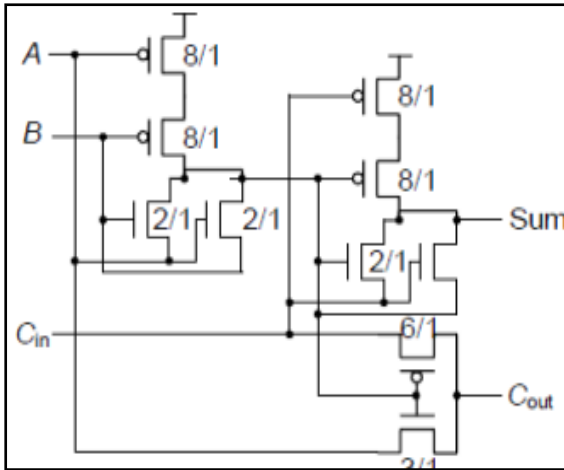


Fig 1(c). SERF Full Adder Cell

The weak driver is formed by the series transistors in the output stage. Therefore, at the last stage additional buffers are required to provide the necessary driving power to the cascaded cells. The Complementary CMOS logic style had the advantage of its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage and arbitrary transistor sizes. The straightforward and area-efficient layout of complementary CMOS circuit is due to the complementary transistor pairs and smaller number of interconnecting wires, which makes the design style more favourable. Another adder shown in Fig. 1(b) is the Complementary Pass Transistor Logic (CPL) with swing restoration, which uses 32 transistors. Fig 1(c) represents Full adder cells based on Sense energy recovery full adder (SERF).

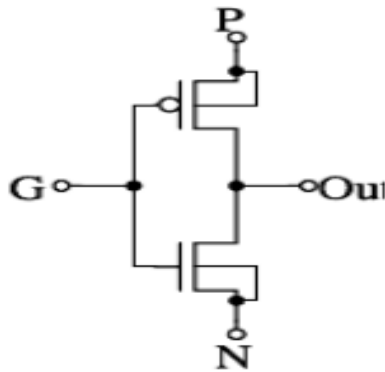


Fig. 2 Gate Diffusion Input basic cell used in 1-bit full adder circuit

The technique on Gate-Diffusion Input (GDI) was proposed by Morgenshtein, which is a wizard design and very flexible for digital circuits. The GDI technique is power efficient without much increase of transistor unit count. GDI cell requires twin-well CMOS or silicon on insulator (SOI) process to actualize which is the main problem of this technique. The Gate-Diffusion-Input technique is based on the use of a simple cell as shown in Fig. 2. The GDI cell contains three inputs: G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). The NMOS and PMOS both the bodies are connected to N or P respectively.

### 3. PROPOSED 1-BIT FULL ADDER DESIGN

A 1-bit CMOS full adder has been designed in this work. There are various ways to realize full adder function, in this work, a full adder is designed using 22 transistors. Firstly working of full adder is designed using multiplexers (MUX) then each multiplexer is implemented using GDI technique as shown in Fig.3 and Fig. 4.

In GDI technique as shown in Fig. 4 a pair of NMOS and PMOS is used and drain of PMOS and NMOS are connected together to give the output of a MUX. Gates of PMOS and NMOS are also connected together and used as a select input of MUX whereas the other inputs of MUX applied to the sources of NMOS and PMOS pair.

For carry output three GDI pairs are used. In first two NMOS and PMOS pair b input is connected to the gate as a select input and Cin is used as input of a MUX. In third pair an input is connected with gates as a selection line and output of previous two with the sources as MUX input. For sum output two inverters and two GDI pairs are used. In first NMOS and PMOS pair c input and invert of c input are connected to the sources and b input to the gates. Output of first NMOS and PMOS pair gives the sum of b and c inputs. Then this output and invert of output are connected to the sources of second NMOS and PMOS pair and gates of GDI pair are connected with a input.

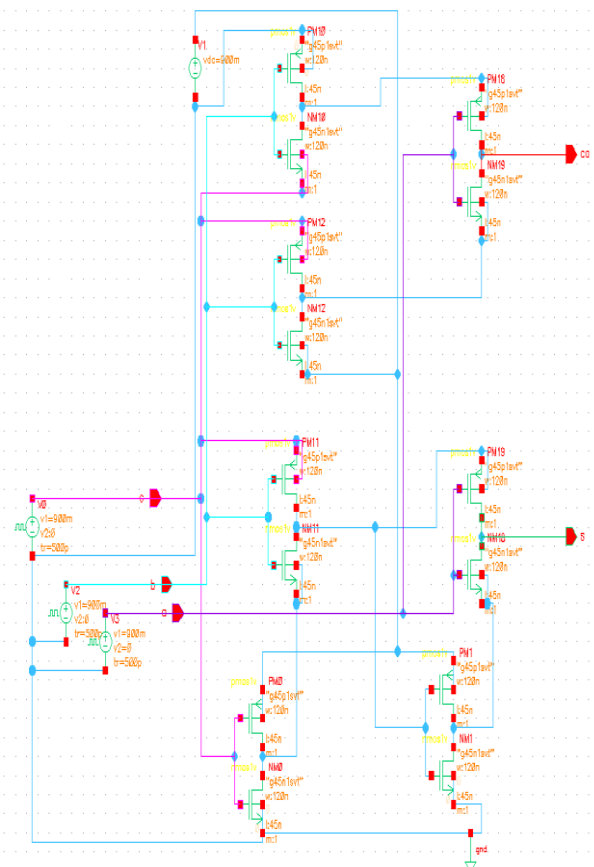


Fig. 3 CMOS 1-bit full adder schematic without buffer

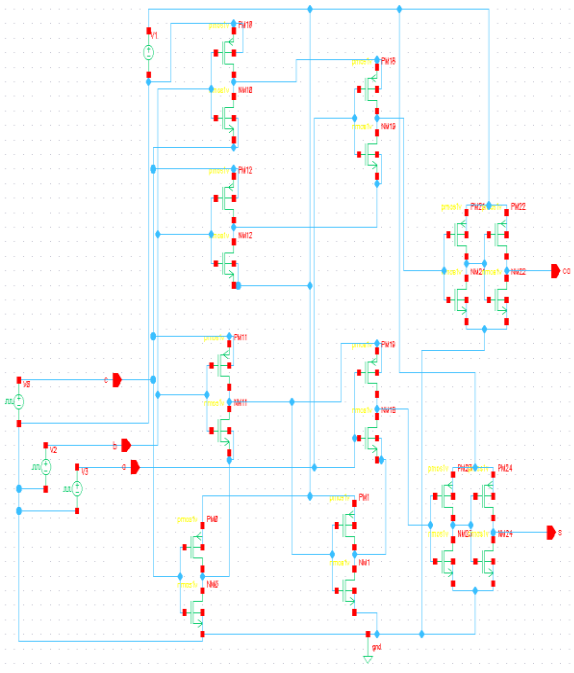


Fig 4. CMOS 1-bit full adder schematic with buffer

Output of this second pair gives the sum of a,b and c inputs. Buffers are used to improve the driving capabilities and waveforms of full adder. The test circuit used for simulation is shown in Fig.5

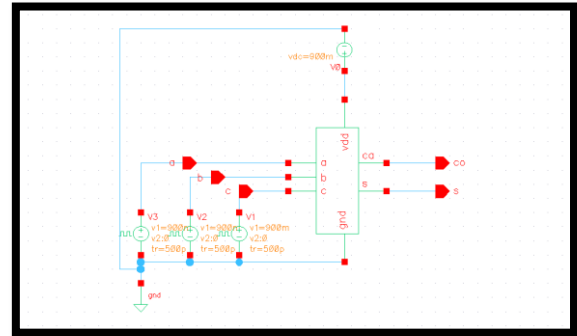


Fig 5. CMOS 1-bit full adder test circuit

#### 4. SIMULATION RESULTS

Simulation results are performed by SPECTRE in Virtuoso, Cadence at 45nm CMOS process with the 0.9 V and 0.7V supply voltage. After verifying the functionality, various performance parameters i.e Power, Delay and Power Delay Product (PDP) of the design are summarised in the Table I for different voltages and loads at a fixed input rise and fall time

Table I Performance Comparison of proposed 1-bit full adder with conventional one at a Rise Time and Fall Time = 500ps with different loads

Parameter Name	V = 0.9 Volts		V = 0.7 Volts		V = 0.9 Volts			
	Conventional CMOS Full Adder	Proposed 1-bit full adder	Conventional CMOS Full Adder	Proposed 1-bit full adder	No load	1fF	10fF	20fF
Total Power (nW)	344.27	139.8	193.13	63.67	139.8	139.8	193.13	63.67
Static Power (nW)	171.27	13.08	95.13	0.559	13.08	13.08	13.08	13.08
Active Power (nW)	173.0	126.7	98.0	63.11	126.7	126.7	98.0	63.11
Leakage Current (nA)	190.0	23.28	136.0	0.798	23.28	23.28	23.28	23.28
Delay (ns)	0.323	0.201	0.737	0.254	0.201	0.223	0.401	0.598
PDP(fJ)	0.111	0.027	0.142	0.016	0.027	0.027	0.142	0.016

Comparison between conventional and designed 1-bit CMOS full adder is shown in Table I. It represents that low power and high speed 1-bit CMOS full adder is achieved and shows less active and leakage power along with total power. The resulted less delay which enhances the speed of operation and leads to less PDP (Power Delay Product). Full adder with buffer at 20fF capacitive load is shown below and Table III shows the effect of various loads on power, delay and PDP at 0.9V.

#### 5. CONCLUSION

Design and simulation of optimized low power 1-bit CMOS full adder has been done at 45nm Technology. Different

parameters at different scenario is calculated and compared with conventional full adder. the simulation result signify that the optimized low power full adder circuit delay is reduced to 0.254ns and power dissipation is reduced to 63.11nW and leakage current is reduced to .798nA for 0.7V at 45nm Technology. Comparison shows that the implementation of the circuit would be better for 0.7V rather than 0.9V.

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