Vedic Mathematics for Digital Signal Processing Operations: A Review

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ABSTRACT
Speed improvement in Digital signal processing is considered to be challenging. High speed multipliers and adders are prime requirement for digital filters and for FFT operations.

Vedic mathematics is an ancient scheme based on 16 formulas (sutras). These are simple and easy methods which can be directly applied for DSP computations. Many researchers have worked on multiplier designs using Vedic operators. Present paper deals with exhaustive review of literature based on Vedic mathematics. It shows that Vedic mathematics can be used for fast signal processing. Multipliers based on Vedic mathematics can be used for speed improvement, reduction in power consumption, complexity, area etc. Vedic mathematical algorithms can be proved efficient over traditional (existing) methods in FIR and IIR filters for providing effective results in de-noising of biomedical Signal.

General Terms
Fast computations**,** Vedic mathematics in signal processing, FIR-IIR filters

Keywords
Vedic Mathematics, Multiplier, DSP, Filter Design

1. INTRODUCTION
Vedic mathematics deals with calculations based on 16 Vedic mathematical formulae known as *sutras* which were used in ancient time by Indian scholars. The present algorithms based on modern mathematics can be simplified and optimized by the use of Vedic Sutras. The methods presented here are direct and easy to implement. Digital signal processing is fastest growing area with large number of challenges in front of engineering community. Faster addition, multiplication, convolution, DFT implementation are very important. Core computing process is a multiplication process and there is a need to find out new faster algorithms and hardware implementation routines. Digital filters when implemented on FPGA obtain fast speed, low chip area and low power consumption over traditional approaches like using DSP chips. This work attempts to review applications of Vedic mathematics in digital FIR and IIR filters. The work proposes use of Vedic mathematical algorithms over traditional (existing) methods in FIR and IIR filters to obtain the above objectives.

It has been proved that MAC, adder, multiplier etc. can be efficiently implemented by use of Vedic mathematical algorithms. The extensive literature review shows that different algorithms are suggested and used for FIR and IIR filter implementation on FPGA. It seems that very less work may have carried out in implementation of FIR and IIR filters by using Vedic mathematics. Hence there is huge scope to work under this area for research.

This article presents a review of the work done in digital signal processing by using Vedic mathematical approach by various researchers.

2. LITERATURE REVIEW
This section discusses the work done by researchers on applications of Vedic mathematics in Signal processing.

The comparison between conventional and Vedic mathematics implemented in VLSI for RSA algorithm, ALU, curve encryption etc. with respect to efficiency analysis and complexity has been presented in [1]. It shows that Vedic mathematical approach is fast and simple. 'Urdhva Tiryagbhyam Sutra' and ‘Nikhilam Sutra' multiplication techniques are proposed in [2]. 16 X 16 multiplier using ‘Urdhva Tiryagbhyam Sutra‘ is presented and extended by using 'Nikhilam Sutra' 16X16 multiplier modules uses two 8x8 modules , one 16 bit carry save adder and two 17 bit full adder stages are implemented here. The carry save adder increases the speed of addition of partial products. The multiplier is implemented in SPARTAN 2 FPGA Device XC2S30-5pq208. The presented method shows speed improvements in [3]. The ‘Urdhva Tiryagbhyam Sutra' and 'Nikhilam Sutra' multiplication techniques are found to be speedy when magnitude of both operands are more than half of their maximum values. A floating point multiplier with 24X24 bit integer multiplication operation is presented using ‘Urdhva Tiryagbhyam Sutra' algorithm, improvement in speed , efficiency and power has been obtained by this sutra. In this the 24 X 24 multiplication architecture is fragmented to four 12 X 12 bit multiplication modules. The 12 X 12 modules are implemented by 4X4 bit multiplier modules. The proposed method shows advantages like power saving, configurability, self-reparability etc. The technique can be extended for DFT [4]. A low power Multiplier is presented in [5] . The implemented multiplier is based on the

ancient Vedic Multiplication Technique. Here the 'Urdhva tiryakbhyam sutra‘ and 'Nikhilam sutras‘ are used for multiplication. The multiplier based on this technique is compared with the modern multiplier to highlight the power and speed advantages in the Vedic Multipliers. To test the Vedic multiplier BIST (Built In Self Test) is implemented and it is found Fault free. The results are compared with the Booth's Multiplier in terms of parameters like power and time delay. The multiplier is implemented using VHDL and Spartan 2G FPGA. The simulation results are presented based on power and time delay. A new architecture for fast polynomial division based on Indian Vedic mathematics is proposed in [6] for LFSR. The synthesis results for Vedic mathematics showed lower hardware requirement. A block convolution process using multiplier based on Vedic mathematics is proposed in [7] using vertical and cross over algorithm, which is the embedded in OLA algorithm to reduce calculations. Coding is done on VHDL for FPGA. The results

shows that linear convolution of finite sequences is easy to compute and better performance can be obtained. Matrix multiplication is very complex in image processing for spatial and frequency filtering. It can be designed effectively and efficiently by using Vedic mathematics. A systolic matrix multipliers using array, Wallace and Vedic multiplication units were simulated and synthesized here. The systolic matrix multiplier with Vedic mathematics was proven to be best. A high speed and low power can be obtained by the proposed method [8]. Reference [9] presents a squarer based high performance multiplier for which Vedic multipliers and two variable constant coefficient multipliers are used. Results are stored in ROM which increases power consumption. The scheme proposed in [10] obtains increased speed and reduced area as compared to array multipliers. According to authors its only disadvantage is increment in dynamic power. According to [11] multiplier is very important part of any processor and needs more hardware resources and processing time than subtractors and adders. Reference [11] states that 8.72 percentage of instructions of any processor are multiplication based and considerable amount of time is spent on this operation by any CPU [12]. A comparative study of different multipliers with respect to low power requirement and high speed is presented in [13] by using 'Urdhva tiryakbhyam'algorithm , it also suggest to use 'Nikhilam sutras' for minimum iterations. Array multiplier, Wallace multiplier and Booth multiplier are compared and Vedic mathematical operations are used in all. The results showed that Booth multiplier is superior in factors like speed, delay, area, complexity and power consumption. Array Multiplier requires more power consumption and gives optimum number of components; the delay for this multiplier is greater than Wallace Tree Multiplier. 'Nikhilam sutras'requires less number of iterations to carry out multiplication. 'Nikhilam sutras' found to be less complex as compared with 'Urdhva tiryakbhyam' algoriothm. Further work can be carried out to minimize delay and to improve the speed. The efficiency comparison between Karatsuba multiplier using polynomial multiplication with multiplier implementing 'Nikhilam Sutras' have been presented in [14] which states that Karatsuba multiplier shows speed improvement as compared to Vedic multiplier. A modified 'Urdhva tiryakbhyam' algoriothm has been implemented on new multiplier for low power, high speed applications. The new algorithm generates concurrent carry for next stage which is based on generation and addition of concurrent partial sums produced within matrix architecture [15].

A MAC unit based on 'Urdhva tiryakbhyam' algoriothm has been implemented on FPGA in [16]. In this the multiply accumulate unit computes product of two numbers and adds the product to accumulator. MAC unit consists of multiplier, adder and accumulator register to store the result. According to authors the 16X16 and 32X32 bit MAC modules show improved speed which may be used in DSP applications.

From ref. [1]-[16] it can be understood that FFT is an algorithm which calculates N point DFT, FFT implementation needs large number of multiplications which are very complex and time consuming. Such issues can be solved by implementing multipliers by using Vedic mathematical operations. From ref.[1]-[16] Urdhva tiryakbhyam' algoriothm is considered to be the best approach for speedy multiplication. According to ref.[17] Vedic FFT is superior in aspects like speed, simplicity, delay, area, power consumption etc. But for large numbers it suffers from high carry propagation delay. Ref. [18] presents a reconfigurable FFT design using Vedic multiplier with high speed and small area. 'Urdhava Triyakbhyam' algorithm of ancient Indian Vedic Mathematics is utilized to improve its efficiency. It consists of 4x4 bit multiplication operation which is fragmented in reconfigurable FFT modules. Here the 4x4 multiplication operation units are implemented using small 2x2 bit multipliers. Re-configurability at real time has been provided for power saving. The re-configurable FFT has been designed and implemented on an FPGA based system which shows high speed and small area as compared to the conventional FFT. FFT is very useful in Digital Signal Processing which is considered to be difficult to implement [19]. Vedic mathematics is a technique based on 16 sutras which reduces complexity, execution time, area, power etc. By using Urdhava Triyakbhyam'algorithm reconfigurable FFT design is proposed here.

A set of algorithms for performing Variable Long Precision Arithmetic (VLPA) and their implementation on a reconfigurable hardware is presented in [20]. These algorithms are characterized by parallelism, scalability and similarity. Therefore a reconfigurable target provides reduced design time, easy scalability and cost performance trade off. VLPA finds application in cryptography, computational algebra and geometry. High speed digital telecommunication systems such as OFDM and DSL need real-time high-speed computation of the Fast Fourier Transform. Thus there is a need to find new algorithms to improve the speed [21]. This paper proposes Vedic algorithm for the implementation of multipliers to be used in the FFT. According to authors the conventional multiplication method requires more time & area on silicon than Vedic algorithms which helps to speed up the signal processing task. Ref. [22] presents an efficient technique for multiplying two binary numbers using limited power and time. The work focuses on speed improvement of multiplication operation of multipliers, by reducing the number of bits using Vedic mathematics. The proposed algorithm is modeled using Verilog. It was found that for 3.3 V supply voltage, the 4 bit multiplier dissipates a power of 47.35 mW. The propagation delay of the architecture was found to be 6.63 ns which showed improvement in power dissipation and speed.

In ref. [23] to increase the ability of the processors and to handle complex processes large number of processor cores is implemented on chip. This creates load over processors which can be reduced by assigning tasks to coprocessors. According to authors ALU speed depends upon multipliers, if multipliers are implemented using Vedic mathematical *sutras* then much of the complexity, speed, area on chip of circuitry can be minimized.

Ref. [24] presents design of NxN multipliers, by using Vedic Mathematic algorithms. Various Vedic multiplication techniques were tested for arithmetic multiplications and it is found that Urdhva Tiryagbhyam Sutra is efficient Sutra , giving minimum delay for multiplication . Using Urdhva Tiryagbhyam, various NxN multipliers have been designed.

The paper [25] presents comparison between implementation of normal multiplication and Vedic multiplication using 'Urdhva Tiryakbhyam Sutra' on hardware. It required same number of multiplication and addition operations. All multipliers have been tested for 16 X 16 multiplications for comparison. Test vectors have been given through a text file. Designed multipliers were implemented on Xilinx FPGA platform and Virtex XCV 300-6PQ240. Various multiplier implementations have been tested and compared for optimum area and speed. It shows that the methods adopted by using Vedic mathematics is very powerful regarding speed, low

power dissipation , area on silicon etc. The paper [26] investigated new multiplier and square architecture based on algorithm of ancient Indian Vedic Mathematics, applicable for low power and high speed applications. It generates all partial products and their sums in one step. Results show that the proposed Vedic multiplier and squarer are faster than array multiplier and Booth multiplier. The paper [27] presents novel Integrated Vedic multiplier architecture, which selects the appropriate multiplication sutra based on the inputs. Depending on applied inputs, the faster sutra is selected by the proposed integrated Vedic multiplier architecture. The simulation results shows that, Urdhva Tiryakbhyam Sutra performs faster for small inputs and Nikhilam Sutra is good for large inputs .

Reference [28] highlight the use of multiplication process based on Vedic algorithms and its implementations on 8085 and 8086 microprocessors, this results in considerable savings in processing time. The implementation of Vedic algorithms in the DSP domain may prove to be extremely advantageous. The implementation of Vedic multiplication on 8085/8086 microprocessors and comparing it with conventional mathematical methods clearly indicates the computational advantages offered by Vedic methods. Fast multiplication is very important in DSPs for operations like convolution and Fourier transforms. A fast method for multiplication based on ancient Indian Vedic mathematics is proposed in paper [29]. Among the various methods of multiplications in Vedic mathematics, 'Urdhva tiryakbhyam sutra' is demonstrated in detail. Urdhva tiryakbhyam is applicable to all cases of multiplication. This is a flexible design in which smaller blocks can be used to build higher blocks.

A simple digital multiplier based on 'Urdhva tiryakbhyam' is presented in ref. [30], which was used in ancient India for multiplication of numbers. The sutra is applied to binary system to make it useful in hardware implementation. All advantages as discussed above are obtained in the same implementation.

Raised cosine filter implementation is discussed in paper [31], it is a set of FIR filters which is utilized to shape the rectangular pulses to sine waves. The paper [32] presents reconfigurable FFT design by using Vedic mathematics with high speed and less area. 'Urdhva tiryakbhyam' algorithm is used to efficiency improvement. Here the 4X4 multiplication operation is fragmented into FFT modules. The 4X4 modules are implemented using 2x2 bit multipliers. As compared to conventional FFT, the Vedic FFT provides many advantages.

Efficient multiplier architecture based on 'Urdhva tiryakbhyam' algorithm is presented in [33] which performs fast multiplication and is used in FFT implementation by using system C language.

FFT architecture needs multipliers to be implemented [34], if multipliers are made faster enough, the processing speed of FFTs can also be increased which means many applications in digital signal processing can be processed with high speed. By using ancient Vedic mathematical formulae (sutras) this can be done.

The reconfigurable FFT design and implementation is proposed in [35] which states that use of Vedic mathematical sutras will reduce time delay, increase speed, reduce surface area and complexity in FFT.

The core computing unit of any DSP processor is ALU which is based on multiplication operation is time consuming and complex. The speed can be increased and complexity can be reduced by use of Vedic mathematics in implementation of multiplication operation. The operations like increment, decrement are based on 'Ekadhikina Purvena' and 'Ekanyunena Purvena' Sutras [36].

Ref. [37] describes implementation of digital filters on FPGA. The structures implemented are MAC unit, FIR filter and IIR filter on FPGA. It states that advantages FPGA implementation ha more advantages over DSP chips like higher sampling rates, lower costs than an ASIC and flexibility than other alternate approaches. Paper shows that FIR and IIR filter implementation on FPGA is flexible and provides good performance as compared to traditional approaches.

An efficient architecture for FIR filters has been described in [38], which shows reduced complexity by use of sparse powers of two coefficients. FIR filter is implemented here by using two full adders and two latches which are implemented on FPGA. High sampling rate can be obtained in this architecture.

In ref. [39] FIR filter is simulated on MATLAB and is implemented in FPGA. A fourth order, hamming window based FIR filter is implemented whose sampling frequency and cut off frequency is 48KHz and 10.8 KHz respectively.

A FIR filter implementation without multipliers and using adders and shifters have been presented in [40]. Modified common sub expression elimination algorithm has been used to reduce number of adders. 50 % reduction in number of slices and 75% reduction in number of LUTs is observed. 50 % reduction in total dynamic power is also seen here.

A cascade connection of several low order filters is presented in [41], the attenuation in pass band is kept very low and stop band attenuation is increased. Multiplier less technique is used here, which utilizes binary shifters and adders to reduce FPGA chip area.

A new algorithm synthesizing multiplier blocks with low hardware requirement is presented in [42]. The structure is implemented on ASIC and the performance has been tested on FPGA hardware. An IIR filter is implemented on FPGA board which considers derivative kick, integral saturation, bump less transfer from manual to automatic mode [43]. The performance comparison between the conventional PID control and the 2-Degree of Freedom PID control for a second order process is presented.

The implementation of FIR and IIR filters on FPGA is carried out in [44] and results showed that pipelined filters shows advantages over non pipelined filters in terms of speed and area on FPGA.

A Distributed Arithmetic (DA) based IIR filter implementation is proposed in [45] which reduces complexity, increases maximum sampling period. An accumulator has been designed which feed backs first two bits serially before complete result is obtained.

IIR filter implementation on FPGA for ECG recording is presented in [46] where MATLAB and Modelsim based simulation results is presented. The results show that fast processing speed is obtained on FPGA. In [47] IIR filter implemented with multiplier is presented, the presented high speed multiplier saves nearly 57% power as compared with traditional multipliers. It reduces number of partial products by 2. The multiplier is designed by the SPST (Spurious Power Suppression Technique) approach. The result shows that

power consumed by SPST technique is less as compared with power consumed by tree multiplier.

Implementation of adaptive IIR filter based on particle swarm optimization (PSO) is presented in [48]. PSO performs randomized search of unknown parameter space by manipulating a population of parameter estimates to converge on a suitable solution. This technique is independent of the adaptive filter structure .Computation cost can be reduced by use of recursive filters in optimal edge detectors [49]. Here anew organization of the filter is proposed at the 2D and 1D levels which reduce the memory size and the computation cost by a factor of two.

3. CONCLUSION

It is found that the Vedic mathematics reduces complications appearing in conventional mathematics. Vedic formulae are based on the fundamentals. It can be used for many applications in Engineering and Technology. This interesting field presents some effective algorithms which can be applied to design of Digital filters. The potential of this field can be used efficiently to solve the real world problems. With use of Vedic multiplier it is possible to reduce area, increase speed, decrease power consumption and to reduce complexity of digital FIR and IIR filters. It is possible to carry out research work on uses of Vedic mathematical algorithms over traditional (existing) methods in FIR and IIR filters that will provide effective results for de-noising of biomedical Signals. FIR and IIR filtering consists of operations like multiplication, addition. By using Vedic *sutras* fundamental entities of FIR and IIR filters can be implemented to achieve merits like reduced area, fast speed etc.

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