Transmission Gate base Programmable Binary Incrementer Decrementer

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ABSTRACT
We can use a high-speed parallel adder in incrementer / decrementer to improve the operating speed which can count up or count down from the loaded value by one step in one clock cycle. For this, design of a faster and highly reliable adder is of major importance. Thus, much effort has been invested in the research that has led to faster and more efficient ways to perform this operation. To prove the efficiency of the proposed method, the circuit is simulated in pass transistor CMOS 50nm technology and some simulation parameters are calcultes in the layout of the circuit. The binary decrementer reduces the stored binary data in memopry or register by '1'. This can be done by using 2's complement method by using XOR gates which convert binary data in 1's complement and then by addition of binary '1' it can be converted to 2's complement form. It is made by cascading 'n' full adders for 'n' number of bits i.e. the storage capacity of the register to be decremented. Hence, a 4-bit binary decrementer requires 4 cascaded half adder circuits. This paper presents the eight bit CMOS base incrementer and decrementer logic design using eight bit adder and subtractor. The parametric simulation is done on MICROWIND layout editor tool. The any conventional static CMOS adder with pullup and pulldown logic requires 32 MOSFET whereas our design adder requires 30 MOSFETs. Our design methodology is based on static CMOS logic and transmission gate logic to achieve smaller delays, reduce power dissipation and optimized area.

Keywords
Incrementer/ decremnter, Layout design, Transmission gate.

1. INTRODUCTION
The INC/DEC circuits are use to counts upwards or counts downwords at every clock cycle. These circuits are widely used in digital systems, such as the program counter and frequency divider. A cound value is preloaded in circuit , this is called it as programmable incrementer decrementer logic. A pre-loadable up/down counter along tith adder is used as an INC/DEC. However, in parallel adders, there occurs a speed limitation in the process of generating the carry bit. This is due to the up/down counter is designed using the process of conventional addition operation. We design a Incrementer decrementer architecture using a data-out XOR array and a decision block but the latency remains high due to the generation of select bit.

This paper presents the eight bit CMOS base incrementer and decrementer logic design using eight bit adder and subtractor. The parametric simulation is done on MICROWIND layout editor tool. The any conventional static CMOS adder with pullup and pulldown logic requires 32 MOSFET whereas our design adder requires 30 MOSFETs. Our design methodology is based on static CMOS logic and transmission gate logic to achieve smaller delays, reduce power dissipation and optimized area. We can use a high-speed parallel adder in incrementer / decrementer to improve the operating speed which can count up or count down from the loaded value by one step in one clock cycle.

2. METHODOLOGY
In this paper we design a programmable incrementer decrementer design by using pass transistor logic circuit technique. The proposed circuit is a eight bit pass transistor base incrementer decrementer, which increments or decrements the loaded value of which each next count state represents the next counter value in sequence. The counter frequency to a great extent improved by sinking the gate count on all timing paths to two gates using pass transistor circuit design techniques. The circuits consist of toggle latch and full adder logic circuits.

The major drawback of the parallel adder is its slow speed due to the time it takes to propagate the carry. Thus to overcome this grawback we propose a transmission gate base adder cell. In our work the use of transmission gate reduces the number of transistors which overcomes the area trade offs. The major limitation of the parallel adder is that the delay increases linearly with the bit length. The circuit consists of a t-gate based multiplexer and a non-inverting buffer (built as a cascade of two inverters). One additional inverter is used to generate the inverse of the clock input signal, required to control the transmission-gates. If both the clock signal and the inverted clock signal are available from external circuitry, this inverter can be removed. The major limitation of the parallel adder is that the delay raises linearly with the bit length. Each full adder has to wait for the carry out of the previous stage to output steady-state result. The result is a reduced carry propagation time. The basic building blocks in this adder is the PG generator, carry generator and sum gernerator.

3. TRANSMISSION GATES
The source and drain end of NMOS and PMOS are connected together to for a logic gate. These are known as transmission gates. The nMOS transistors passes weak at conducting high signal and are good at conducting low signals whereas the pMOS transistors are good at conducting high signals but weak at conducting low signals, so transmission gates are often made from a pair of complementary transistors. When the control signal S is high, the transmission gate conducts logic signals of either sense in either direction. A special symbol is used for the CMOS transmission gate:

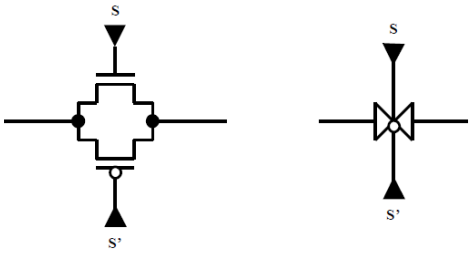

Fig 1 Symbol of transmission gate

4. ADDER MODULE

The half adder is design using two transmission gates and one inverter which requires total 6 transistors. Using two half adders and one OR gate, the full adder circuit is design which consumes 14 transistors. Thus the number of transistors requires to design the full adder are reduce to 14 instead of 32 requires in conventional full adder circuits. In conventional incrementer decrementer circuit the parral ripple carry adder is use which has the speed limtationdue to the carry propagation time. Also for eight bit parallel adder it requires 368 transistors for its design. In our propose transmission gate base logic this circuit requires 240 transistor and reduces the carry propagation path length. It improves the speed with reduce number of transistors.

5. TIMING SIMULATION

Timing simulation of our design is done on MICRWIND layout editor tool. All the possible input patterns are applied on the design and its output responces are analyze. For simulation all eight possible combinations of values of input signals for a FA cell, i.e., 000, 001, 010,.., 111 are use. By using three bit inputs of full adder cell it is possible to use total sixty four transissions of all possible eight combination of inputs are applied on simulator. In the process of time delay measuring the previous values of the input signals should be considered together with the current signal values. This is due to the fact that there exist cases when the values of input signals remain unchanged implying that the outputs remain unchanged as well, and, therefore, no time delay should be measured.

6. IMPLEMENTATION

The address generation for data read and write memory data, branching and storage functions in Microprocessors, microcontrollers and application-specific processors Incrementer Decrementer logic is use. The circuit can be design by using low power high speed adders and a toggle flipflop base asynchronous counter logic circuit. The output of counter is connected to the one of the bit of adder unit and the second input of adder unit is connected through a chain of XOR logic to get 2's complement number to add or subtract the counter output. The second input can be act as a load value for the circuit. The input given on second input is consider as a load value and the circuit either increment or decrement from this load value depends on the direction signal 'INCDec' from the logic circuit.

7. RESULTS

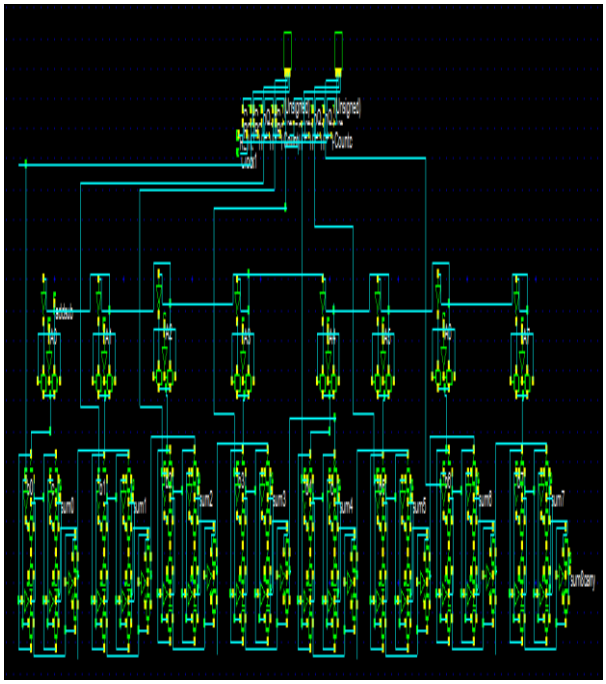

Fig 2 Schematic circuit for Incrementer Decrementer logic

The CMOS layout is shown in above figure 2 is the schematc circuit for incremeter decementer logic. It cincludes the chain of XOR logic gates which is use to transfer counter output directly in case of increnet operation andit transfer its 2's complement in case of decrement operation. The loaded value from which increment or decrement operation is done is pass through this XOR chain. Depends on the IncDec signal the counder output is added or subtracted from this loaded value.

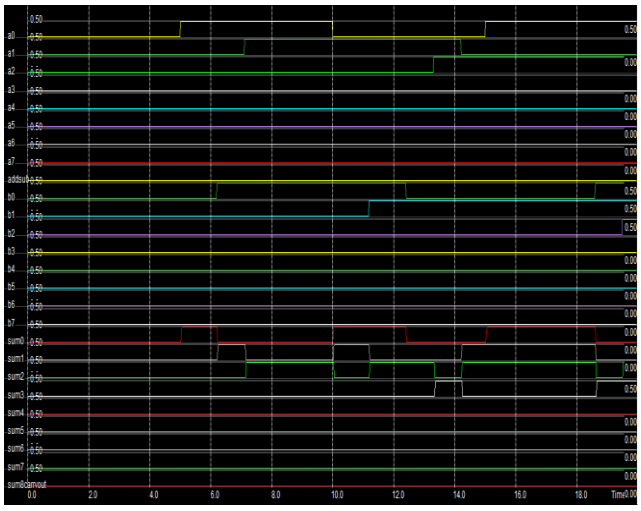

Fig 3 Timing simulation of addition operation when IncDec signal is at '0'.

The fig 3 shows the incremented operation of adder module when the IncDec signal is at logic '0'. This logic '0' is transmitted the data of the loaded value and thus this value gets added from the counter output value.

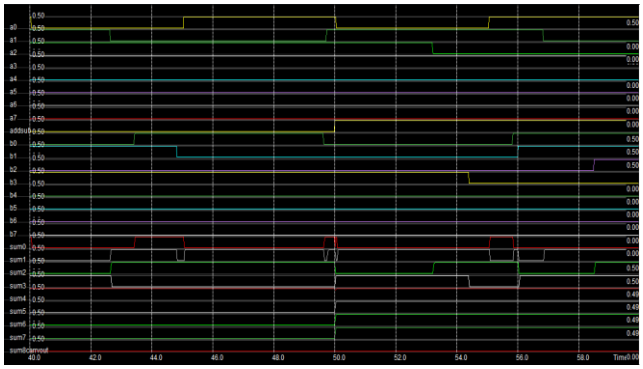

Fig 4 Timing simulation of subtraction operation when IncDec signal is at '1'

The fig 4 shows the decremented operation of adder module when the IncDec signal is at logic '1'. This logic '1' is transmitted the 2's complement of the loaded value and thus this value gets subtracted from the counter output value.

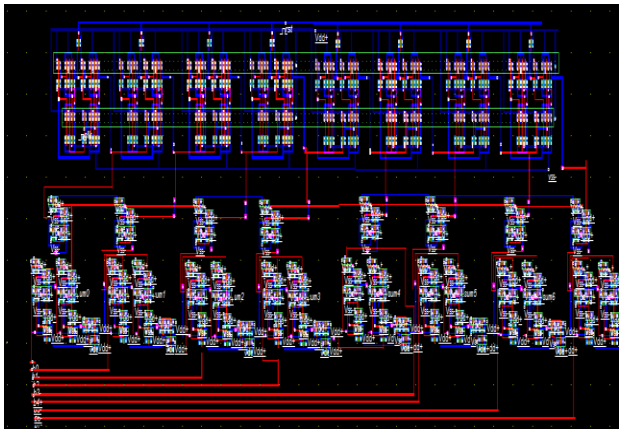

Fig 5 Layout design for 8 bit Incrementer/ Decrementer Logic from predefine state act as timer.

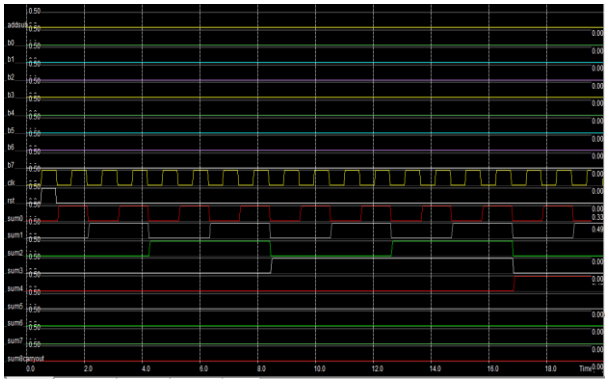

Fig 6 timing simulation of 8 bit Incrementer/ Decrementer Logic start from state '0'.

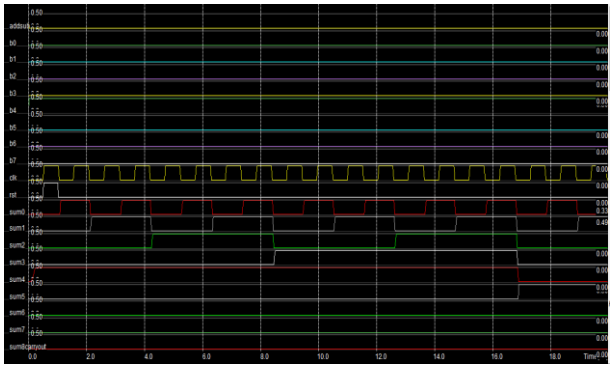

Fig 7 timing simulation of 8 bit Incrementer / Decrementer Logic start from state '16'.

The timing simulation of our Incrementer/Decrementer logic circuit is mainly depends on the value of IncDec signal, when IncDec= 0 it will increment the corresponding sequence and vice versa. This logic can be use as a timer, when the load value is inserted in the circuit then it will increment or decrement from that loadedvalue depends on the IncDeec signal.

Table 1 Comparative analysis with base paper

Node Point	Base Paper [1]				Our Work				Base paper [2]	Our work
	Delay	Tphl (ps)	Tplh (ps)	Power dissipation	Delay	Tphl	Tplh	Power dissipation	Prop Delay	Prop Delay
s3	1.44	38.873	50.402	5.2072mW	0.055	26 to 37ps	20 to 24ps	2uW	0.215ns	0.148ns
s2	1.422	34.914	46.509	5.2072mW	0.041	26ps	41ps	2uW		
s1	9866	37.793	46.45	5.2072mW	0.927	22 to 37ps	20 to 41ps	2uW		
s0	1.599	41.121	188.87	5.2072mW	1.75	23 to 35 ps	21 to 39ps	2uW		
Avarage Power	5.2072mW				1.2 to 1.5uW				43%	40%
Number of Transistor	362				152				Increase	Decrease

8. CONCLUSION

The above circuits are simulated in microwind 3.1 using 90nm CMOS technology. The delay measured in the range of 55 ps to 175ps and power consumed in the range of 2 microwatt from the supply voltage to the output nodes of sum0, sum1, sum2, and sum3. The adder module is design with reduced 152 number of transistor as compare to 362 number of transistor requires in base paper work. The average power dissipation of the adder circuit at simulation is 1.2 to 1.5uW. The propose incrementer decrementer logic is design using transmission gate uses 280 NMOS and 272 PMOS type transistor. We design the basic building blocks of adder subtractor by using transmission gate. Transmission Gate has is a high-quality switch with low resistance and capacitance. Sizing is also not necessary in general, as the resistance and capacitance decrease and increase respectively as the gate W=L ratio is increased. TG is commonly used to implement designs with the minimum number of transistors.

9. REFERENCE

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