Nano Scale Low Power Chopper Amplifier using Cascode and Miller Compensation Nutrilization in 45 nm CMOS

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ABSTRACT
In this paper, reduced power consumption, low-noise CMOS amplifier using chopper technique is designed, chopper-equalized amplifier had been used as a front end of a voltage-to-frequency converter instrument which performs pretty well, and they were meeting just about every specification, but they had a problem with undesired and unpleasant little offset shifts and jumps. Trying to solve this problem of the jumpy offset, Chopping technique proved to be an efficient approach to decrease the low-frequency offset and 1/f noise of amplifiers. The chopper amplifier consist of combination of two-stage amplifier .The first stage is by the introduction of cascade amplifier produces high output impedance to the amplifier and the equivalent Miller capacitance of the second stage amplifier constitute to reduce the modulating noise by introduction of low pass filter in a attainable objective to gain the required Performa, so the chopper amplifier need low-pass filter, which can decrease the power consumption. The circuit of the proposed chopper amplifier is designed and simulated with cadence 45nm CMOS process and at a supply voltage 0.7V. Simulation results shows that the equivalent input noise is 23nV/ Hz at 100 Hz and the power consumption is 102 Watt.

Keywords
Chopper amplifier, low-noise, equivalent input noise, low-pass filter.

1. INTRODUCTION
A chopper is a static device that converts fixed dc input to a variable dc output voltage directly. An amplifier using chopper technique may be described as an ac transformer since they behave in an identical pattern. Essentially, a chopper is an electronic switch that is used to interrupt one signal under the control of another. Amplifier Choppers may be categorized on several bases. One classical implementation of chopper circuit can be in chopper amplifiers. They can be classified as direct Current amplifiers. Signals that required amplification can be so weak that an increasingly high gain is desired, but very high gain Direct Current amplifiers are much difficult to be designed with low offset value and 1/f noise ratio and having reasonable stability and bandwidth. An Alternate Current Amplifier circuit is very much easy task to design so in case of chopper amplifier circuit it is used to divide the input signal so that it can counter handle as if it is an Alternate Current signal, then integrated back to a Direct Current signal at the output terminal. As a result extremely small DC signals can be amplified. This approach is more often used in electronic instrumentation techniques where accuracy and stability are important factors of consideration.

The offset voltage produced at the input of amplifiers becomes very important when posing to amplify small signals with very high gain factor, as this technique results in a voltage amplifier having negligible input offset, and because this input offset voltage does not fluctuate much with time and temperature, this techniques is also called "Zero-Drift" amplifiers. Related techniques that also give these Zero-drift advantages are Auto-zero and Chopper-stabilized Amplifier. Auto-zero amplifiers use a secondary auxiliary amplifier to correct the input offset voltage of a main amplifier. Stabilized Chopper amplifiers uses an integrated approach combination of auto-zero and chopper techniques to give out some excellent DC precision specifications [1]. Advanced bipolar amplifiers offer 0.1 μV/ºC drift and offset voltages of 25 μV also offset voltages less than 5 μV with practicably no measurable offset drift is gained with choppers. A basic chopper amplifier circuit is shown in Figure below.

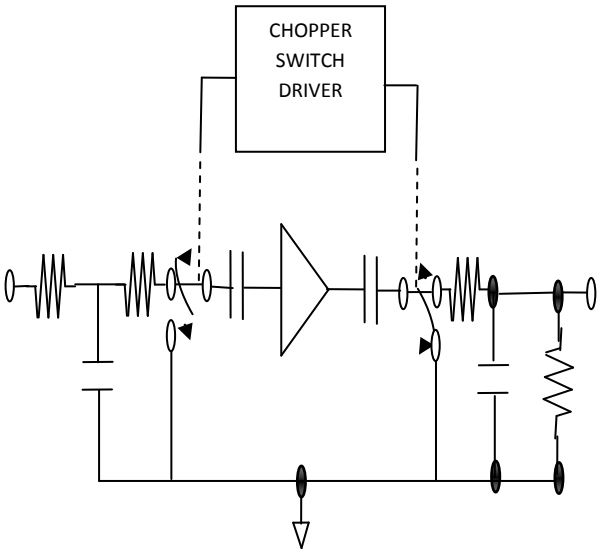


Figure 1 Basic Chopper Amplifier

2. WORKING
The basic working of the amplifier comprises of switching the terminal switches at the "Z" (auto-zero) position, the input capacitors C2 and C3 are charged due to amplifier input and output offset voltage, respectively. Terminating the switches in the "S" or the sample position, VIN which is input voltage is connected to VOUT i.e. voltage at the output terminals through the path composed of R1, R2, C1, C3, and R3. The frequency gained by the chopper amplifier is more often between a few hundred Hertz and several kilohertz, and it is noticeable factor because this is a sampling system in which the input frequency should of the

order of one-half the chopping frequency in order to prevent errors due to further matching. The R1-C1 combination provides an anti-matching filter. It is also supposed that after a static condition is reached, there is only a negligible amount of charge being transferred during the substitutive cycles. The capacitor C4 output, and the load RL, must be so selected such that there is negligible Vout drop during the auto-zero cycle low power consumption amplifier and a low-noise and is one of the key circuits for detecting the small level signals in the biomedical information sensing system [1-2]. An amplifier implemented in CMOS technology is attractive due to its low consumption capability, dense integration, and lower cost. However, in CMOS technology, 1/f noise becomes a serious problem, which limits the minimum detectable signal in amplifier at low frequency [3-4]. The chopping technique is widely used in amplifier for low noise. It is a modulation technique that can be employed to reduce the effects of op-amp imperfections including noise and input referred dc offset voltage [5-6].

3. PRINCIPLE OF CHOPPER AMPLIFIER

The principle of chopper amplifier is illustrated in adjoining figure. The signal at the input is first modulated by the chopping frequency fchop and chopping signal i.e. m (t) with and shifted to odd harmonics of the chopping frequency. Whereas Vos and Vn denote the dc offset and noise of the amplifier, respectively. Resultant amplified signal is modulated which then demodulated to the even harmonics, noise and DC offset before the amplifier is just modulated once and shifted to the odd harmonics of the chopping frequency. Through a post low-pass filter, the noise and dc offset are filter out, leaving base-band input signal without any distortion. To prevent attenuation of input signal which is converted to fchop, the cut off frequency of chopper amplifiers should be higher than the chopping frequency, and a post low-pass filter is need to filter modulated noise. Thus the conventional chopper Amplifier consumes large power and comprises of complicated circuitry. A low-noise and low power consumption amplifier has been a vital for detecting the signals with small values. It is mostly used in biomedical information systems. EEG (electroencephalogram) and ECG (electrocardiogram) have characteristics of low amplitude and low frequency [1-2]. The bandwidth of the signal is from 3Hz to 100Hz and amplitude less than 100 μV and in case of EEG signals bandwidth is from 1Hz to 150 Hz and amplitude less than 5mV. These signals require precise designing of the acquisition and recording units for capturing and storing these signals. So the low noise, low power and the low offset amplifier are the key circuit for detecting the small signal levels in the information system of biomedical stream, 45nm CMOS technology is implemented due to its low power consumption capability, dense integration and low cost. Moreover in technology implementing CMOS processes 1/f noise becomes a serious problem. It limits the minimum detectable signal at low frequency. So as an associated approach to design a high precision amplifier, chopping technique is widely used, it has an advantage of having low noise and low offset characteristics.

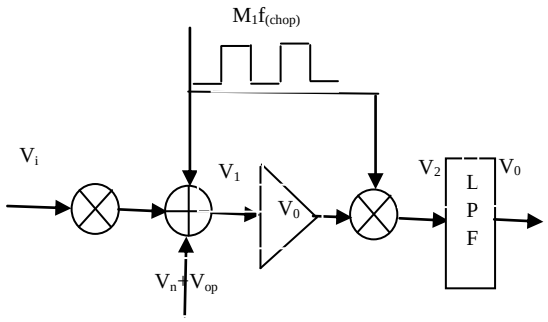


Figure 2 Schematics of Chopper Technique

4. SCHEDULED CHOPPER AMPLIFIER

The conventional chopper amplifier had disadvantage of having higher cut off frequency than fchop or chopping frequency and a post low-pass filter also it consume large power. Op-amp imperfections such as noise input referred DC voltage can be reduced by chopping technique which makes use of Modulation process. It implements modulation technique which can be used to decrease Op-amp imperfections. A post low pass filter is also needed to filter out modulation noise, which consumes power too. Conventional chopper amplifier is very complex and consumes large power. In order to reduce the power exhaust and streamline the circuitry of chopper amplifiers, a chopper amplifier is designed and verified in this paper. The schematic circuit of the proposed amplifier is shown below.

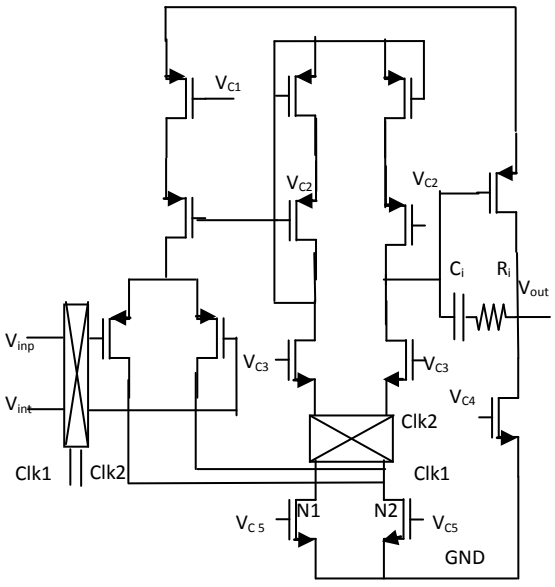


Figure 3 Schematics of Proposed Chopper Amplifier

It is a two-stage amplifier, the first stage is a folded cascode op-amp and the second stage is a common source amplifier with Miller compensation, Cascode amplifier is basically a differential amplifier. It comprises of series of amplifier stage interconnected with one another amplifier stage [10]. Cascode amplifier offers low output gain but requires low supply voltage the cascode approach reduces the gate-drain capacitance of the Amplifier. The cascade amplifier is presented in the figure below

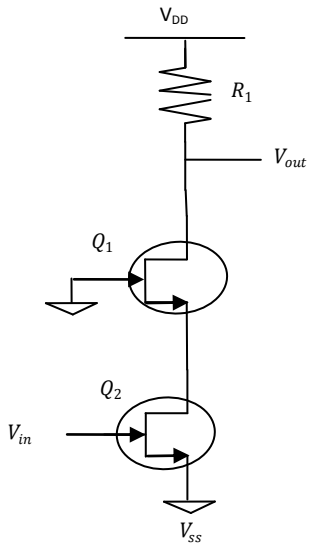


Figure 4 Schematics of cascade Amplifier

Miller multiplication effects and provides added isolation between the input and output ports and also improving amplifier stability without using feedback. In the design of two-stage amplifiers, it is common practice to employ the Miller compensation technique since it allows the use of a relatively low-valued compensation capacitor and increases the achievable bandwidth thanks to the well-known pole-splitting feature. It is also known that the stability of Miller-compensated amplifiers is deteriorated by a right-half-plane zero which must be eliminated in CMOS amplifiers especially in low-power applications, due to the low trans-conductance of MOS transistors. Miller compensation can also be applied to multistage amplifiers [5-12], and in this context three main possible arrangements have been recognized [4]. The nested Miller (NM) compensation is one of these, and can be profitably used when only the final gain stage is voltage-inverting. Several of the NM compensated amplifiers considered in the literature are implemented in bipolar technology or have high-drive capability and are not designed for low-power CMOS applications [2-10]. Here, the main effort of researchers has been to improve the nature. This design approach also improves the gain compared to the single transistor stage. Miller compensation can provide large output voltage range assuming that the DC gain of the second stage op-amp is A, an equivalent capacitance of (A+1)Cc can be obtained at the output node of the first stage op-amp according to Miller's theorem, where Cc is the Miller capacitance. Before compensation, the poles of the two-stage cascade are given as,

$$P_1 = \frac{1}{R_1 C_1} \quad \text{- (1)}$$

$$P_2 = \frac{1}{R_2 C_2} \quad \text{- (2)}$$

Where RK & CK are the Resistance and Capacitances at respective nodes, k= 1, 2, 3....

In order to achieve dominant pole stabilization of the op-amp, Miller compensation is employed to achieve pole splitting. In this technique, the compensation capacitor (Cc) is connected between the output of the first and second stages. The compensation capacitor splits the input and output poles apart thus obtaining the dominant and non-dominant poles which are spaced far away from each other [1-6]. However, Miller compensation also introduces a right-half-plane (RHP) zero due to the feed-forward current from the output of the first stage to the op-amp's output. Figure 2-2 shows the small signal model for two stage op-amp used for nodal analysis the resistances and capacitances respectively at nodes.

Small signal transfer function for miller compensation of two stage op-amp is:-

$$\frac{V_{out}}{V_s} = g_{m1} R_1 g_{m2} R_2 \frac{(1-\frac{s}{Z_1})}{(1-\frac{s}{p_1})(1-\frac{s}{p_2})} \quad \text{- (3)}$$

The right-half-plane zero is located at

$$Z_1 = \frac{g_{m2}}{C_c} \quad \text{- (4)}$$

Hence, the dominant pole is located at

$$P_1 = \frac{1}{g_{m2} R_2 R_1 C_c} \quad \text{- (5)}$$

And the non-dominant pole is located at

$$P_2 = \frac{g_{m2} C_c}{C_c C_1 + C_1 C_2 + C_c C_2} = \frac{g_{m2}}{C_1 + C_2} \quad \text{- (6)}$$

The open loop gain of op-amp is given as

$$A_v = g_{m1} R_1 g_{m2} R_2 \quad \text{- (7)}$$

While the unity-gain frequency is given as

$$f_{un} = \frac{g_{m1}}{2\Pi C_c} \quad \text{- (8)}$$

In addition, the cascade transistors of the first stage op-amp provide large output impedance, which can build a low-pass filter with the equivalent capacitance of (A+1) Cc. So the presented chopper amplifier does not need a post low pass filter and its dissipation can be drastically reduced.

5. SIMULATION RESULTS

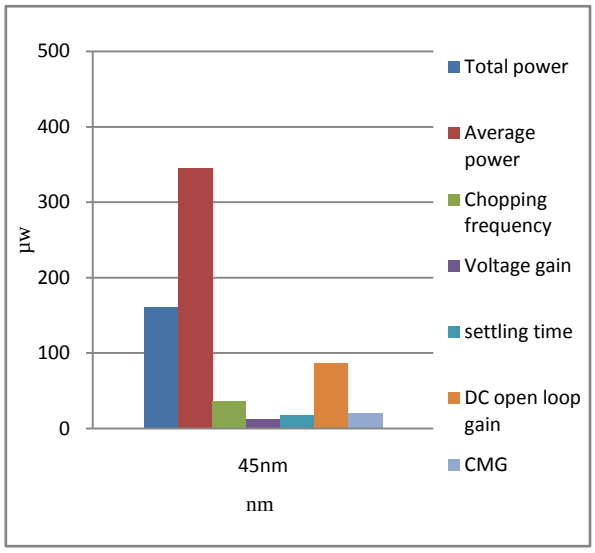
The circuit of the presented chopper amplifier is designed using 45nm CMOS. The whole amplifier consumes 117_W of power at a supply voltage 0.7V. The chopping frequency is set to 10KHz. Fig.3 shows the periodic small signal analysis results. The DC open loop gain of the chopper amplifier is 100dB with phase margin of 55. Simulation results show that the equivalent input noise is 129nV/Hz at 1Hz and is 20 nV/Hz at 100Hz Figure 6 shows the transient response of the chopper amplifier in closed loop configuration with a gain of 500. The input signal is a 500 Volt sinusoidal waveform with frequency of 50Hz.

The input referred noise power spectral density of the chopper amplifier with and without chopping, here without chopping means the CLK1 is set to 0.7V and CLK2 is set to ground is shown in Fig. 2. From the results, we can see that input referred noise power spectral density of the amplifier with chopping is smaller than that without chopping

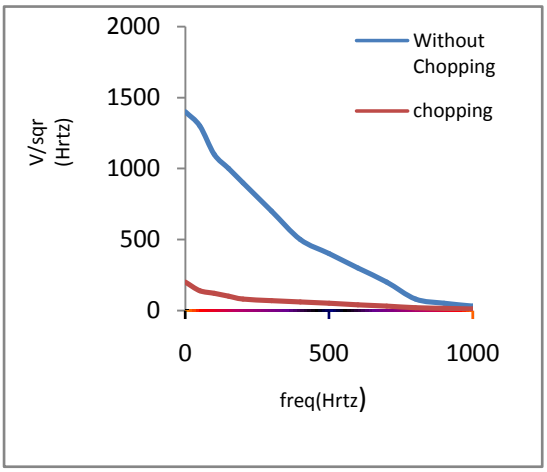
Table1 Observed output parameters at the given input

S.no	Parameters	Technology Used	Input Supply	Output
1	Total Power(µw)	45nm	0.7V	161.0
2	Average	45nm	0.7V	346

	power(µw)			
3	Chopping frequency (kHz)	45nm	0.7V	10
4	Voltage gain(V)	45nm	0.7V	2.90
5	Settling Time(ns)	45nm	0.7V	10
6	DC open loop gain(dB)	45nm	0.7V	87
7	Common mode gain	45nm	0.7V	5



Output Response of Chopper Amplifier Simulated at 45nm technology



Waveform of Proposed Amplifier

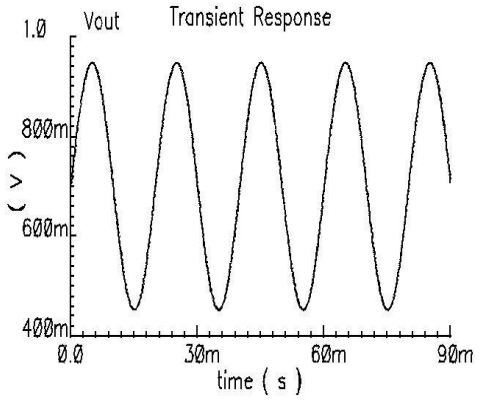


Figure 5 Transient Response

6. CONCLUSION

A low-power and low-noise chopper amplifier without post low-pass filter is presented. The two-stage amplifier configuration is adopted, in which the high output impedance of the first stage and the equivalent Miller capacitance of the second stage amplifier constitute together a low pass filter to filter out the modulation noise. The circuit of the presented chopper amplifier is designed in 0.18_m CMOS process. The whole amplifier consumes 102 Watt of power at a supply voltage .7V, and the equivalent input noise is 23nV/Hz at 100Hz

7. ACKNOWLEDGEMENT

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