CMOS Design of Area and Power Efficient Multiplexer using Tree Topology

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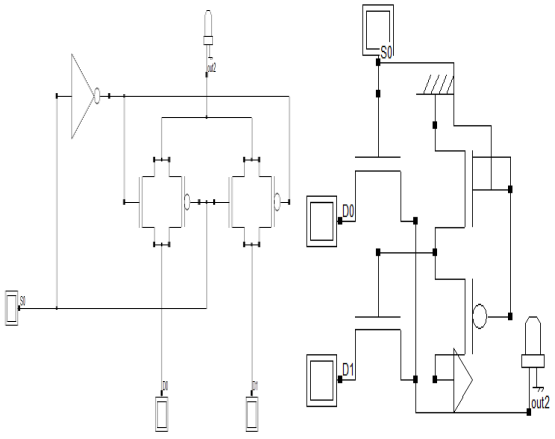
ABSTRACT
In this paper a design of 16:1 tree type multiplexer has been presented using GDI and PTL technique. The proposed design consists of 31 NMOS and 15 PMOS. The proposed multiplexer is designed and simulated using DSCH 3.1 and MICROWIND 3.1 on 180nm technology. Performance comparison of proposed multiplexer with CMOS, Pass transistor and transmission gate logic design techniques is also presented. The different logics are compared with respect to Area and Power. A power comparison with respect to supply voltage has been performed using 180nm technology. At 1.2 V power supply the proposed MUX design consumes 56.046 μW power on BSIM-4 and 56.043 μW power on LEVEL-3. The proposed design has shown reduction in power consumption by 90%, 55% and 53% as compared to CMOS, TG and PTL techniques respectively on BSIM-4 simulation model. So the proposed multiplexer design has been proven power efficient in comparison with other logic designs.

Keywords
CMOS, Gate Diffusion Input, Multiplexer, Pass Transistor Logic, Transmission Gate, tree type.

1. INTRODUCTION
With rapid development of portable digital applications, the demand for increasing speed, compact implementation and low power dissipation triggers numerous research efforts [1]. The idea to enhance the performance of logic circuits results in the development of many logic design techniques during the last two decades. Multiplexer abbreviated as MUX can be analogue circuits using MOSFETs and transistors or they can be of digital type circuits made from logic gates. MUX are used in a number of applications which includes digital signal processing, telephone network, communication system and telephone memory etc. Transmission gate type of MUX structure implemented using very less number of transistors compared to CMOS based logic design. Pass transistor logic is used to improve the performance of arithmetic and logic circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors and it also uses less number of transistors, runs faster, and requires less power than the same function implemented with the same transistors in CMOS logic.

GDI (Gate Diffusion Input technique) - a new low power design technique approach allows implementation of a wide range of complex logic functions using only two transistors [1]. GDI technique is suitable for design of fast, low power circuits, using reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving power characteristics [1]. Area of the chip reduces with the reduction in number of transistors and also we can decrease the number of layout elements. A tree-type multiplexer is composed of multiple 2-to-1 MUX cells which are organized in a tree type structure. A multiplexer tree is a network topology where the output of one multiplexer is used as the input to another multiplexer and so on. To construct 16:1 MUX number of 2:1 MUX required are 15 which is given by N-1 and in this case N=16.

2. MULTIPLEXER
A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer with 2^n inputs has n select lines. Multiplexer tree is a network topology where the output of one multiplexer is used as the input to another multiplexer. n:1 multiplexer is generally implemented by decomposition into smaller multiplexers. It can be obtained by cascading two or more multiplexers with lesser number of inputs. Number of 2:1 Multiplexers required to make n:1 MUX, where n is an integer greater than or equal to 2 , is n-1. So number of 2:1 MUX required to make 16:1 MUX is 16-1=15.Here MUX circuits are classified into CMOS circuit , PTL, transmission gate and GDI MUX composition. A 2:1 MUX can be designed with the help of different logics. Different 2:1 multiplexer circuits are shown here from previous papers which are implemented using different techniques. Figure 1(a) shows transmission gate MUX circuit which is basically a switch that connects two points. Figure 1(b) shows PTL MUX Figure 1(c) is implemented using CMOS logic which has the advantage that the output signal swings the full voltage between the low and high transitions. Figure 1(d) uses GDI based logic to implement 2:1 MUX whose function is based on the use of a simple cell. The GDI method enables the implementation of a wide range of complex logic functions using only two transistors therefore consumes very less area. Figure 1(e) and 1(f) are composed of logic gates as circuits. A logic gate is a basic building block of digital circuits. So the different 2:1 MUX designs has been shown in the figure 1 using different logics.



(a) (b)

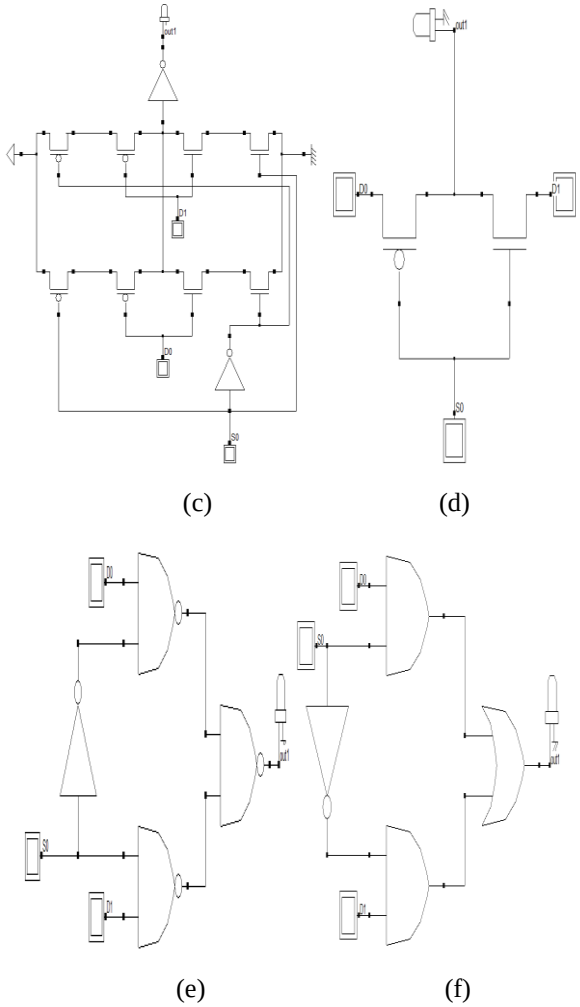


Fig 1. 2:1 MUX (a) Transmission gate MUX[8] (b) PTL MUX (c) CMOS MUX[8] (d) GDI MUX (e) NAND based MUX[8] (f) AND based MUX[8]

The comparison of different 2:1 MUX designs has been shown in the table 1 as shown below:-

Table 1. 2:1 MUX's COMPARISON

2:1 MUX design	PTL	CMOS	TG	GDI
NMOS	3	6	3	1
PMOS	1	6	3	1
Area (μm^2)	215.3	584.1	318.3	98.3
Power(µW)	5.186	48.643	21.414	1.394

3. LOGIC BLOCK DIAGRAM OF PROPOSED MUX

The logic diagram of proposed 16:1 GDI PTL MUX consists of 8 2:1 PTL MUXs which has inputs D0 to D15 and S0 as a select input. Then the output of each 2:1 PTL MUX produces one output signal which acts as a inputs to next stage 2:1 GDI MUXs having select line as S1 and so on. In this manner a tree topology based design is presented of proposed multiplexer. The logic diagram is shown in figure 2 as:

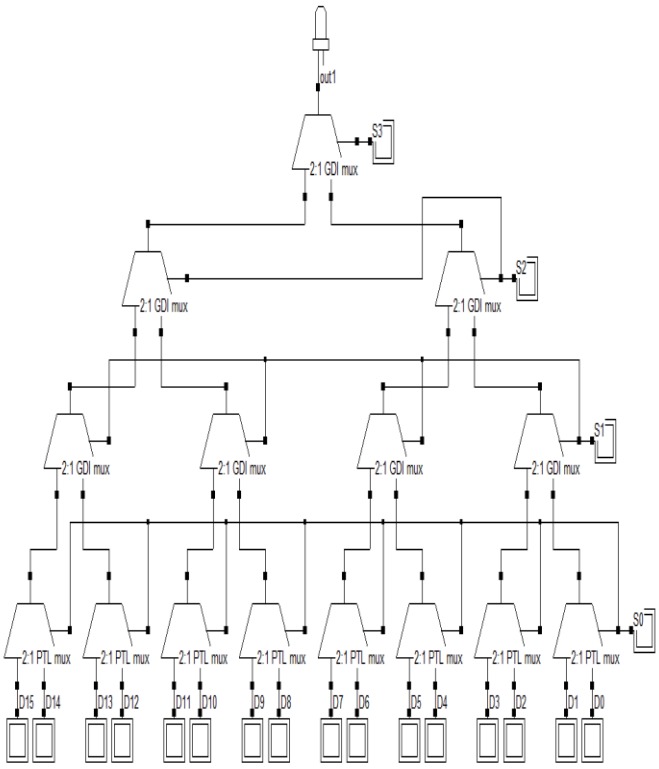


Fig 2. Logic Diagram of proposed MUX

4. PROPOSED SCHEMATIC DESIGN SIMULATION

The design of proposed 16-to-1 multiplexer has been implemented by using only 46 transistors (15 PMOS & 31 NMOS). In this design, Gate Diffusion input with Pass transistor logic kind of MUX structure is composed with less number of transistors compared to the CMOS and transmission gate based design. So, in the proposed design power consumption is reduced with minimum space as shown in figure 3(a). The other design schematics for 16:1 MUX are also shown in figure 3(b) and 3(c):-

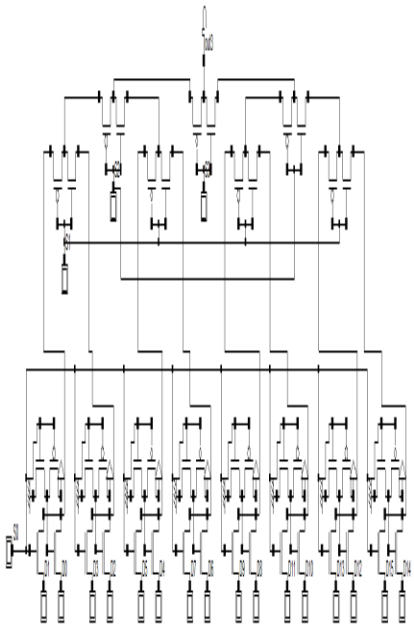


Fig 3. (a) Proposed 16:1 MUX design

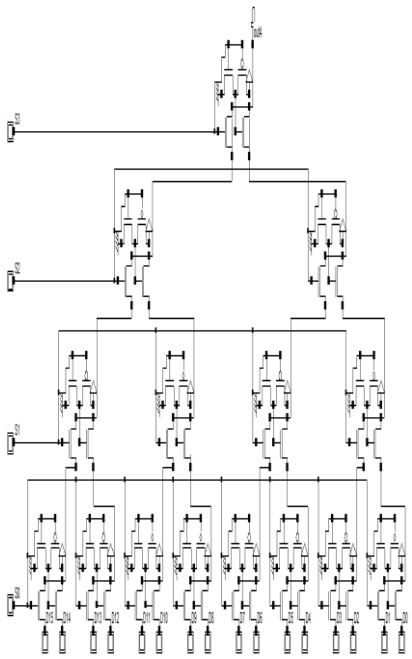


Fig 3. (b) 16:1 PTL MUX design

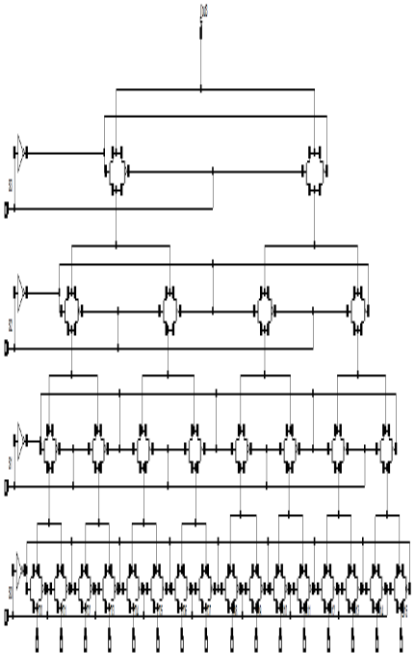


Fig 3. (c) 16:1 TG MUX design

Fig 3. 16:1 MUX designs

The timing simulation of proposed 16:1 MUX is shown in figure 4 as:

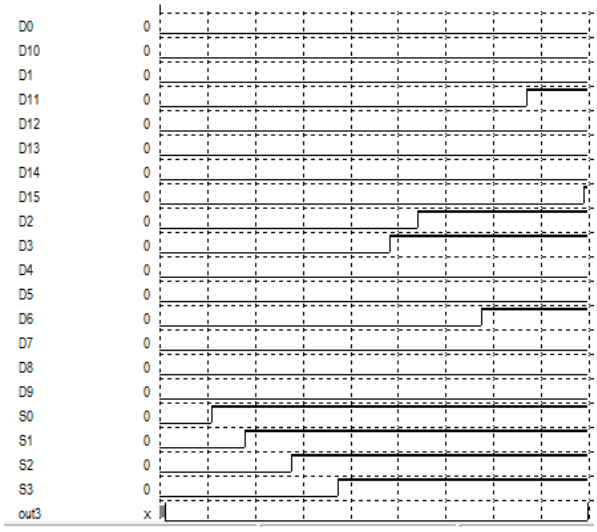


Fig 4. Timing Simulation of 16:1 MUX

Before the actual layout design of 16:1 MUX it is necessary to validate the schematic of logic circuit. To overcome this problem DSCH and MICROWIND designing tools works parallel. DSCH is basically a logic editor and simulator which is used to simulate the logic design to understand the proper functioning of the circuit and after that the layout of that circuit is implemented in MICROWIND. The proposed 16:1 MUX has been compared with other 16:1 MUX designs of CMOS, PTL and transmission gate logic in terms of area and power in MICROWIND 3.1 designing tool on 180nm technology.

5. LAYOUT RESULT ANALYSIS

In complex VLSI design manual layout designing for a very complex circuit will become very difficult. So as compared to manual layout designing an automatic layout generation approach is preferred. In DSCH designing tool the schematic diagram has been firstly designed and validated at logic level on DSCH designing tool. DSCH 3.1 has feature to analyze timing simulation and power consumption at logic level but accurate layout information is missing. DSCH 3.1 tool is used to generate the VERILOG file of schematic which is compiled by the MICROWIND3.1. The layout of proposed MUX is shown as:

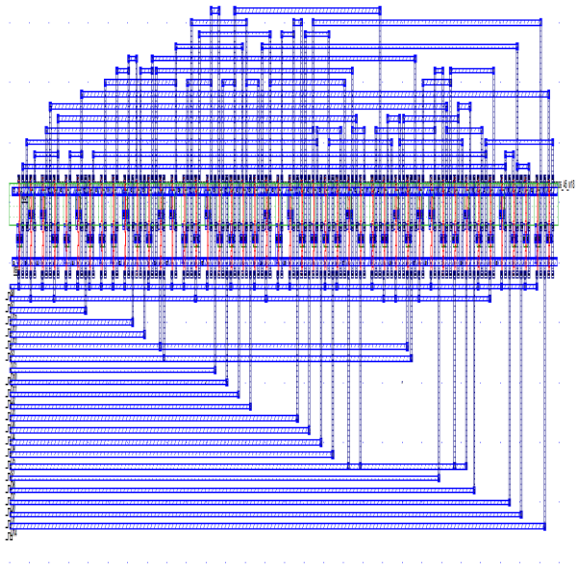


Fig 5. Layout of proposed 16:1 Multiplexer

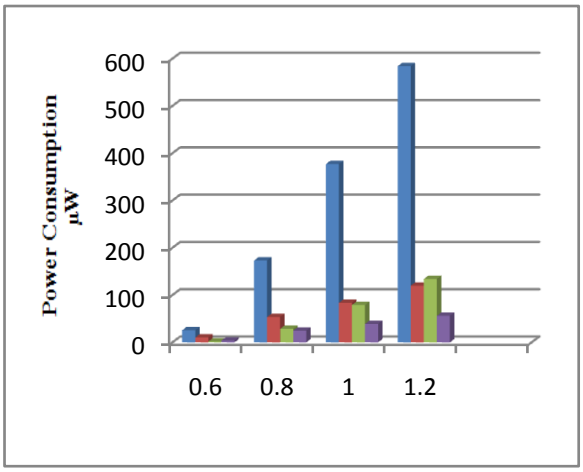
The following table shows the comparison of 16:1 MUX by different logics in terms of area and power and it is clear from the table that the proposed MUXs performance is better in terms of both area and power with transistor count of only 46 as compared to 60, 68 and 172 for PTL, TG and CMOS designs respectively.

Table 2. Comparative Analysis of proposed 16:1 MUX in terms of area and power with other 16:1 MUX design by different logics on 180nm technology

16:1 MUX design	Proposed MUX design	PTL	CMOS	TG
NMOS	31	45	86	34
PMOS	15	15	86	34
Area (μm^2)	5675.9	8471.9	20602.9	8654.9
Power (µW)	56.046	120	584	125

6. SIMULATION RESULTS

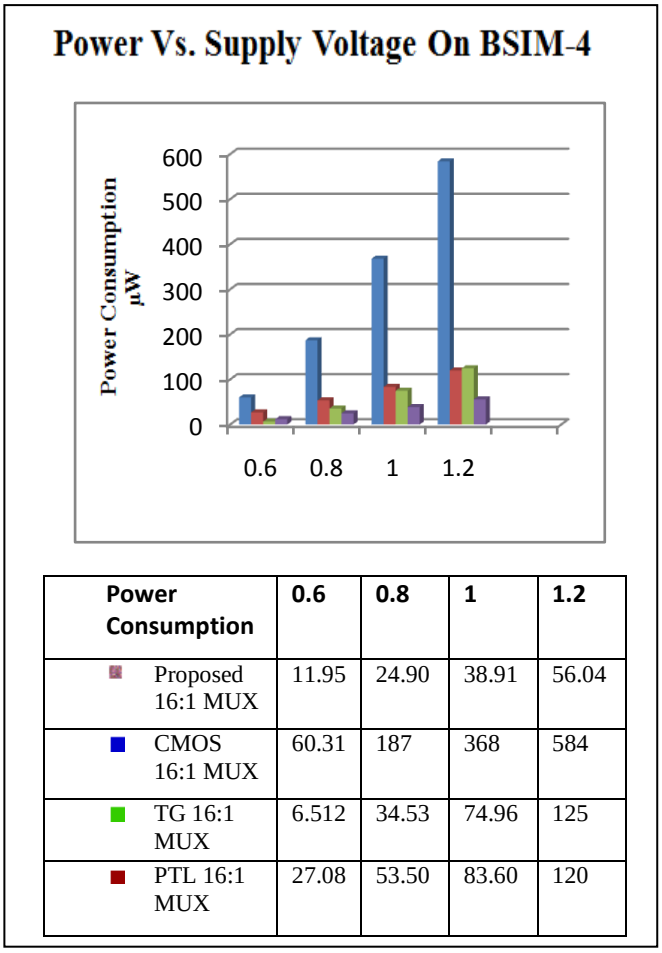
The performance of proposed 16:1 MUX design has been evaluated in terms of area and power on 180nm technology. Simulation has been performed using MICROWIND 3.1. Results are measured in terms of power variation with respect to the variation in voltage on BSIM-4 and LEVEL-3. By using MICROWIND 3.1, the analog simulation has been carried out to know the power consumption at different voltages. Analog simulation is carried out for proposed 16:1 MUX on 180nm technology. For 180nm VDD is fixed to 1.2V and VSS to 0V. In MICROWIND 3.1, simulation can be done by four ways as:-Voltage vs. Time, Voltage and current vs. time, Voltage vs. Voltage and Frequency vs. Time. Voltage vs. Time simulation for proposed 16:1 MUX has been done on 180 nm as:-



Power Consumption	0.6	0.8	1	1.2
Proposed 16:1 MUX	3.87	24.90	38.91	56.04
CMOS 16:1 MUX	25.59	173	377	584
TG 16:1 MUX	1.84	28.60	79.14	134
PTL 16:1 MUX	10.24	53.49	83.58	120

Fig 6. Comparison of Power Consumption on BSIM-4

Simulation results have been shown in Figure 6 and 7. From Figure 7 it is clear that power dissipation increases with the increase in the power supply.



Power Consumption	0.6	0.8	1	1.2
Proposed 16:1 MUX	11.95	24.90	38.91	56.04
CMOS 16:1 MUX	60.31	187	368	584
TG 16:1 MUX	6.512	34.53	74.96	125
PTL 16:1 MUX	27.08	53.50	83.60	120

Fig 7. Comparison of Power Consumption on LEVEL 3

7. CONCLUSION

Proposed 16:1 MUX has been realized in 180-nm CMOS technology which consists only 46 transistors. Proposed 16:1 MUX design has been implemented by using 31 NMOS and 15 PMOS transistors. Area and power simulation of proposed 16:1 MUX design has been shown on 180nm. The simulation results for area and power parameters have been shown on LEVEL-3 and BSIM-4 models. Proposed 16:1 MUX using 46 transistors consumes power and area respectively 56.046 µW and 5675.9 $\mu m^{2.}$ at BSIM-4 model and consumes power and area respectively 56.043 µW and 5675.9 $\mu m^{2.}$ at LEVEL-3. All the results are carried out using MICROWIND 3.1. The results presented in this research work have a future scope that will encourage the upcoming research on the GDI and PTL techniques. GDI circuits can also be implemented along with other low power logic based designs from which more area and power efficient designs are expected.

8. REFERENCES

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