Launch and Capture Power Reduction using Data Encoding and Precomputation Technique

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ABSTRACT
Testing of VLSI circuits aims for high quality screening of circuits by targeting performance related faults. The main objective of testing is to generate compact test set which is used to detect multiple faults present in the circuit, which results in increase of switching activity hence the pattern should be optimized without losses in performance of the circuit. Design for Testability mechanism is used for launch-off shift and launch-off capture testing and it supports design partitioning approach in which one region is tested at a time results in launch and capture power reduction in a design flow compatible manner. Data encoding scheme is used to reduce the power dissipation by the means of reducing the switching activity which involves comparison of two bits at a time. By using precomputation technique which involves comparison of single bit at a time starting from its MSB to LSB, the power dissipation is reduced up to 20% compared to data encoding technique.

Keywords
Design partitioning, Launch-off capture (LOC), Launch-off shift (LOS), Peak power reduction, Test power reduction.

1. INTRODUCTION
Testing of VLSI circuits aims for detecting the fault present in the circuit. Scan based at speed testing performs load, launch, and capture operation for every test pattern [6]. Load operation is performed by scan/shift operation by means filling up all the scan chains with the pattern. The main drawback of this method it takes more time the pattern need to check whether transitions launched from scan cells can arrive at their destinations within functional clock period[1][2]. There are two different methods for launching transitions off the serially loaded pattern. In launch-off-capture test, a functional capture operation launches transition from the locations with respect to the input. In launch-off-shift, a single cycle shift operation launches transitions from the locations where the serially loaded pattern differ from its one bit shifted version.

In at-speed testing schemes yield losses. Excessive switching activity during the Launch cycle may result in elevated peak supply current leading to IR drop that increases the signal propagation delays in the combinational logic. Test pattern generation while accounting for the functional clock gating logic in order to produce patterns that disable parts of the design during launch and capture to reduce peak power at the expense of pattern count inflation. Another approach that elevates pattern count while reducing peak launch power has been in the form of generating patterns under the constraint that only one chain launches transitions while all chains capture them. Another similar scan-segmented solution partitions the scan cells into three regions where only two out of three regions launch and capture any test pattern [5]. A partitioning approach where power wise costly patterns are further analyzed via fault simulation to identify the location of the care bits, which dictate the partitioning of the design during capture; with few problematic patterns, such an approach can deliver power savings. X-fill approaches have also been proposed where pattern count inflation is the side effect [7]. Partitioning the design and testing one partition at a time used to reduce launch and capture power in built-in self-test (BIST) in LOS and in LOC testing schemes, In this method newly generated patterns targeting one partition at a time end up loading the interface registers of other partitions as well, incurring test time and data volume penalty. Finally, low-power automatic test pattern generation (ATPG) solutions have been proposed, design partitioning technique that can reduce power dissipation during launch and capture operations in at-speed testing.

2. EXISTING METHOD
Single region testing is performed by a given set of test pattern. Loading the pattern into scan cells launch and capture operation is performed. Design can be partitioned into strongly connected components (SCC) [2].Interface register of a region are those that feed the register of other region trough path. By the means of shifting operation load and capture power can be reduced. A set of patterns optimized for cost and quality can be utilized in a low power manner. Goal is to enable a single-region-at-a-time testing of a design by utilizing any given set of test patterns. Upon the completion of the loading of a pattern into the scan cells, launch and capture operations will be done in every region, one at a time, resulting in as many pairs of launch and capture pulses as the number of regions. A pattern may launch transition(s) from a set of flip-flops which may possibly span multiple regions and capture these transitions in the region(s) being tested. The challenge is that any test pattern may be testing any set of regions by launching transitions from any other set of regions. Testing one region at a time in at-speed testing requires launching and capturing transitions within one region at a time, delivering savings in launch and capture power. Power savings during launch and capture in LOS and LOC testing via partitioning can be attained while being able to apply the patterns of a power-unaware ATPG tool. In which a cyclically formed regions are tested in an order opposite to the data flow, region interface registers can be restored back to their load state upon launch and capture [5].

To identify the design regions, and thus the scan cell groups properly, the s-graph of the design can be partitioned into strongly connected components (SCCs). An SCC is a group of nodes where each node within the SCC is reachable from any other in the SCC [2]. It is guaranteed that an s-graph partitioned into SCCs contains no cycles, delivering the acyclicity needed. Multiple SCCs can form a region. Interface

registers of a region are those that feed the registers of other regions through combinational paths. Launching and capturing only the interface registers of a region in testing another region enables a more cost-effective scheme.

3. DATA ENCODING SCHEME

A data encoding scheme is used to reduce power dissipation by the means of reducing the switching activity. The transactions from 0 to 1 number are counted and if it is larger than half of the link with the inversion will be performed. In this technique encoding and decoding is done at every node [10].

3.1 Types

Minimization the power dissipation is done by minimizing the coupling transition activities. Coupling transitions is mainly classified into four types.

- Type I
- Type II
- Type III
- Type IV

Type I

It occurs when one of the input switches and the other one remain constant.

T-1 00, 11

T 10, 01

Type II

It occurs when one of the inputs switches from low to high and the other one switch from high to low.

T-1 01, 10

T 10, 01

Type III:

It occurs when both input switches simultaneously.

T-1 00, 11

T 11, 00

Type IV:

It occurs when both current and previous input does not change.

T-1 00, 11

T 00, 11

3.2 Encoding Architecture

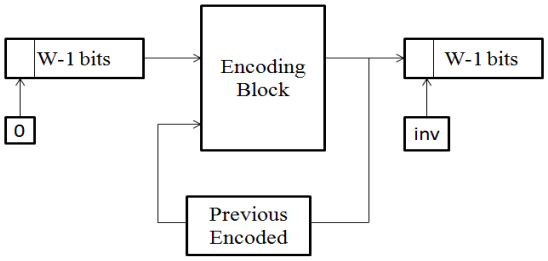

Fig 1: Block diagram of encoding scheme

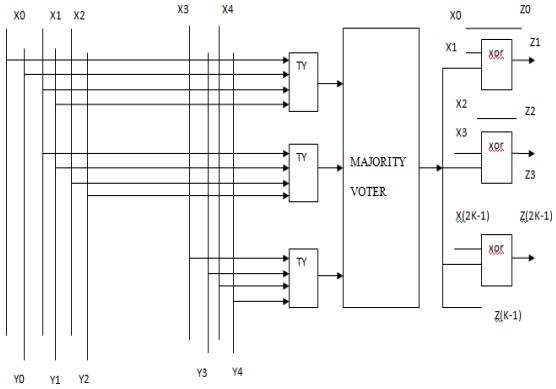

Fig 2: Internal view of encoding block

The proposed encoding architecture is based on the odd invert condition. Consider a link width of w bits. If no encoding is used, the body flits are grouped in w bits by the network interface and are transmitted via the link. In this approach, one bit of the link is used for the inversion bit, which indicates if the flit traversing the link has been inverted or not. More specifically, the network interface packs the body flits in w − 1 bits. The encoding logic E, which is integrated into the NI, is responsible for deciding if the inversion should take place and performing the inversion if needed. To make the decision, the previously encoded flit is compared with the current flit being transmitted. This latter, whose w bits are the concatenation of w – 1 bit and a "0" bit, represents the first input of the encoder, while the previous encoded flit represents the second input of the encoder [10]. The w − 1 bits of the incoming (previous encoded) body flit are indicated by Xi (Yi), I = 0, 1. . . W − 2. The width bit of the previously encoded body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0). In the encoding logic, each Ty block takes the two adjacent bits of the input flits (e.g., X1X2Y1Y2, X2X3Y2Y3, X3X4Y3Y4, etc.) and sets its output to "1" if any of the transition types of Ty is detected. This means that the odd inverting for this pair of bits leads to the reduction of the link power dissipation. The Ty block may be implemented using a simple circuit. The second stage of the encoder, which is a majority voter block, determines if the condition given in is satisfied (a higher number of 1s in the input of the block compared to 0s)[9]. If this condition is satisfied, in the last stage, the inversion is performed on odd bits. The decoder circuit simply inverts the received flit when the inversion bit is high.

3.3 Precomputation Technique

Precomputation is a logic optimization technique which selectively compares the input bits and it inverts the bit in data encoding technique thereby reducing switching activity and power dissipation up to 20% reductions in switching activity and power dissipations are possible using this scheme.

4. RESULTS

The proposed precomputation and data encoding schemes are designed in Xilinx 13.2 using VHDL coding and the results are being simulated.

4.1 Data Encoding

Minimization of power dissipation is done by minimizing the switching activity by comparison of all bits which results in launch and capture power reduction.

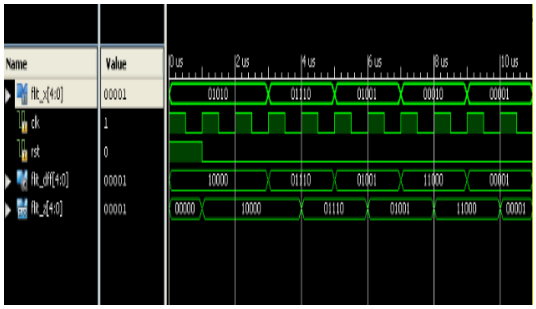

Fig 3: Output waveform of data encoding scheme

4.1.1 Power Analysis Report

In the power analysis report of data encoding technique Junction temperature, Leakage power, Dynamic power, quiescent power and total power can be determined.

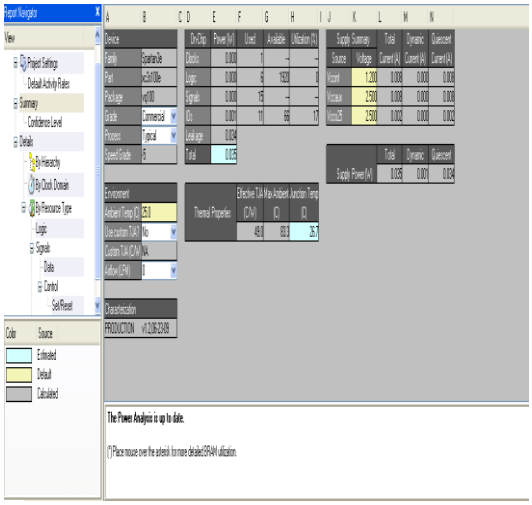

Fig 4: Power analysis report of data encoding technique

4.2 Precomputation Technique

It compares using bit by bit operations, from MSB to LSB.Switching activity is reduced compared to data encoding technique.

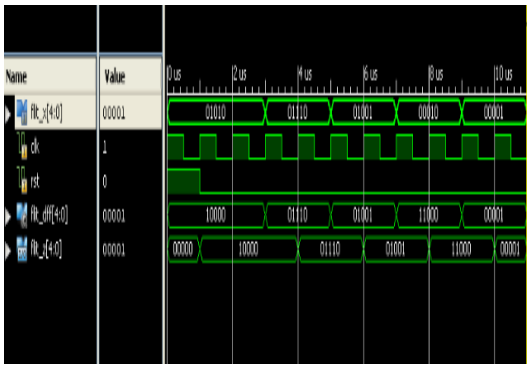

Fig 5: Output waveform of Precomputation technique

4.2.1 Power analysis report

In power analysis report of precomputation technique Junction temperature, Leakage power, Dynamic power, quiescent power and Total power can be determined. It is found that the power is reduced up to 20% compared to data encoding scheme.

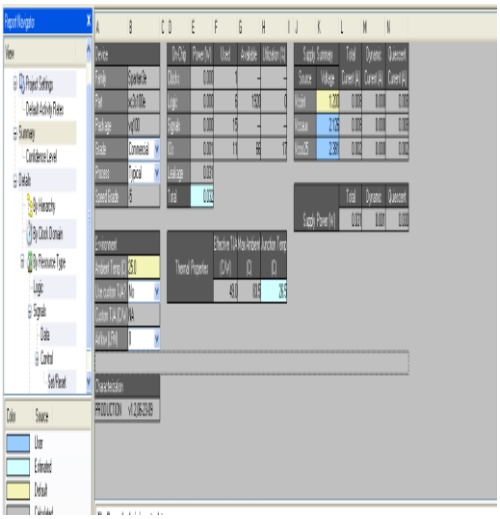

Fig 6: Power analysis report of precomputation technique

4.3 Power dissipation

Table 1: Comparison of power dissipation by data encoding and precomputation technique

Parameter	Data Encoding Scheme	Precomputation Technique
Junction temperature	26.7	24
Leakage power	0.035mw	0.031mw
Dynamic power	0.007mw	0.001mw
Quiescent power	0.034mw	0.021mw`
Total power	0.035mw	0.022mw

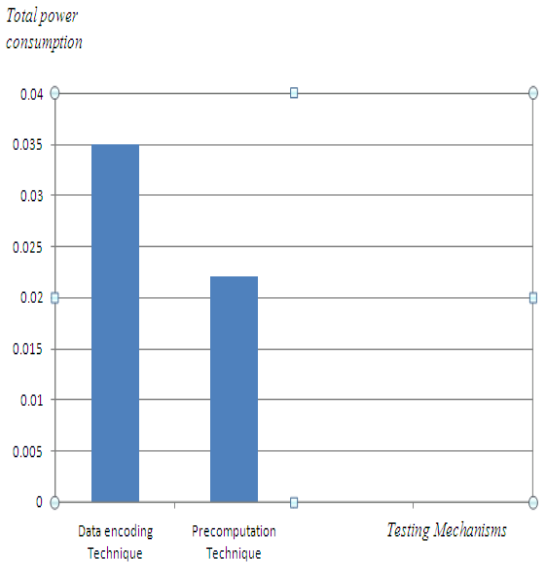

Fig 7: Comparison of power dissipation by data encoding and precomputation technique

It is evident from the table 1 and fig.7 that by using pre computation technique the power dissipation can be reduced up to 20% when compared to data encoding scheme.

5. CONCLUSION

Data encoding scheme is used to reduce the power dissipation by means of reducing the switching activity up to 30% compared to Design for Testability mechanism [1]. By using pre-computation technique in which it involves bit by bit operations from MSB to LSB, the switching activity is reduced up to 20% compared to data encoding technique and 50% compared to Design for Testability mechanism. When it finds first variation starting from its MSB then inversion operation is performed which reduces the power dissipation up to 20%. Multiply and accumulate unit (MAC) can also be used in which the power dissipation reduced to a larger amount compared to data encoding technique and pre-computation technique.

6. REFERENCE

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