Analysis of THD and Output Voltage for Seven Level Asymmetrical Cascaded H-Bridge Multilevel Inverter using LSCPWM Technique

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ABSTRACT
In this paper, a seven level asymmetrical cascaded H-Bridge multilevel inverter in three phase configuration using different level-shifted carrier-based pulse width modulation techniques is discussed. Multilevel inverters have become more popular due to high voltage and high power output applications. Comparable to traditional PWM inverters, multilevel inverters are able to reduced switching losses, low harmonic distortion and high-voltage capability with low costs. This paper presents ACMLI using fixed frequency level-shifted carrier-based PWM technique for three phase squirrel cage induction motor as a load. In this topology, two H-Bridges with 8-IGBT switches are used for getting seven level output voltage for each phase leg. Simulation using MATLAB-SIMULINK is done to verify the performance of the ACMLI using LSCPWM techniques. Simulation results for this proposed scheme are shown in this paper.

General Terms
Multilevel Inverter (MLI), Symmetrical Cascaded H-Bridge Multilevel Inverter (SCMLI), Asymmetrical Cascaded H-Bridge Multilevel Inverter (ACMLI).

Keywords
Level shifted carrier-based PWM techniques (LSCPWM), MATLAB SIMULINK, Total Harmonic Distortion (THD).

1. INTRODUCTION
The increasing demand for electrical energy, depleting fossil energy reserves and the increase in energy prices have necessitated to use the current energy resources more efficiently. Power electronic converters as the essential equipment to convert and control of electrical power in the wide range of milliwatts to gigawatts with the help of semiconductor devices are finding increased attention. Controlled ac drives are usually connected to the medium-voltage network (2.3 KV-13.8 KV) cover a power range of 0.2 MW to 40 MW. Today, it is hard to connect a single power semiconductor switch directly to medium-voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a multilevel inverters has emerged as the solution for working with higher voltage levels.

Multilevel inverters include an array of power semiconductors and capacitor voltage sources with a single dc source or multiple dc sources without capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig 1: shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions.

Multilevel Inverter (MLI) offers a number of advantages when compared to the conventional two-level inverters in terms of improved D.C. link utilization and harmonic spectrum. The stepped approximation of the sinusoidal output waveform with higher levels reduces the harmonic distortion of the output waveform and the stresses across the semiconductor devices and also allows higher voltage/current and power ratings. The reduced switching frequency of each individual switch of the inverter also reduces the switching losses and improves the efficiency of the inverter.

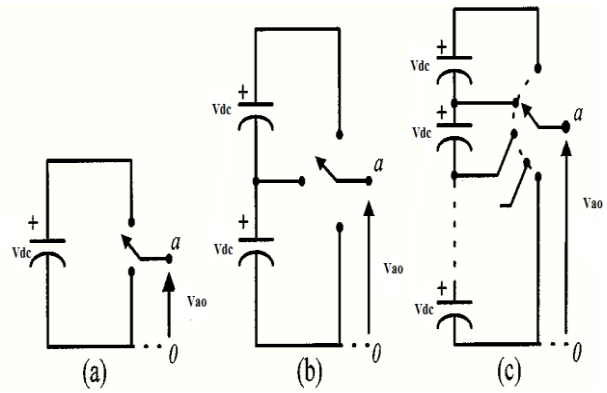

Fig 1: One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels

The different types of MLI are diode clamped, flying capacitor, cascaded MLI. Diode clamped requires more no of diodes and flying capacitor has capacitor balancing problem. The cascaded H-bridge inverters having more no of advantages such as modular structure compare to other topologies and less no of components. It is one of the topologies proposed for drive applications which meet the requirements such as high power rating with reduced THD and switching losses. The asymmetrical cascaded H-Bridge MLI reduces the number of input DC sources required for getting the same number of levels in the output as in the symmetrical cascaded H-Bridge MLI. In this paper, level shifted carrier based PWM techniques are used for reducing the THD and the carriers used are the triangular waves with same amplitude and frequency.

2. ASYMMETRICAL CASCADED H-BRIDGE MLI

Cascaded H-Bridge multilevel inverter (CMLI) removes the excessively large number of bulky transformers demanded by conventional multipulse inverters, the clamping diodes demanded by diode clamped multilevel inverters and the flying capacitors demanded by flying capacitor multilevel inverters. It consists of a series connection of multiple H-Bridge inverters. Each H-Bridge has the same architecture as a typical single phase full bridge inverter. CMLI introduces the concept of using separate DC sources to produce a staircase ac voltage waveform. Each H-Bridge inverter has its own DC source. By cascading the output voltage of each H-Bridge inverter, a stepped voltage waveform is produced. If the no. of H-Bridges is N, then the output voltage is obtained by adding the output voltage of each H-Bridges as shown in equation (1).

$$V_0(t) = V_{01}(t) + V_{02}(t) + ...V_{0N} \quad \text{..... (1)}$$

There are two types of CMLI as follows:

1. Symmetrical cascaded H-Bridge multilevel inverter (SCMLI).
2. Asymmetrical cascaded H-Bridge multilevel inverter (ACMLI).

A symmetrical cascaded H-Bridge multilevel inverter having same value of DC voltage sources for all H-Bridges whereas asymmetrical cascaded H-Bridge multilevel inverter having different value of DC voltage sources for all H-Bridges. The advantage of ACMLI over SCMLI that ACMLI allows more levels to be created in the output voltage using same no. of H-Bridges as SCMLI and thus reduces the THD with less H-Bridge cells required.

The proposed three phase 7-level ACMLI consists of two H-Bridges for each phase leg as shown in Fig 2. The first H-Bridge H_1 required a separate DC voltage source V_{dc}, whereas the second H-Bridge H_2 required a separate DC voltage source $V_{dc}/2$. Let the output of H_1 be denoted as $V_1(t)$ and the output voltage of H_2 be denoted as $V_2(t)$. Hence the output voltage is given by $V(t) = V_1(t) + V_2(t)$. By alternatively opening and closing the switches of H_1, the output voltage of $V_1(t)$ can be made equal to $+V_{dc}, 0, -V_{dc}$. Similarly the output voltage of H_2 can be made equal to $+V_{dc}/2, 0, -V_{dc}/2$. Hence $V(t)$ take values $-1.5V_{dc}, -V_{dc}, -0.5V_{dc}, 0, 0.5V_{dc}, V_{dc}$ & $1.5V_{dc}$.

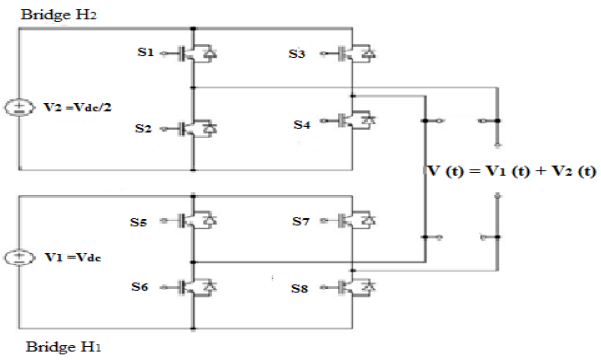

Fig 2: Topology of seven level ACMLI

The switching states of seven level asymmetrical CMLI output voltage is given in the Table 1.

Table 1. Switching States of Seven Level Asymmetrical Cascaded Multilevel Inverter

S1	S2	S3	S4	S5	S6	S7	S8	Output
1	0	0	1	1	0	0	1	$1.5V_{dc}$
0	1	0	1	1	0	0	1	V_{dc}
1	0	0	1	1	0	1	0	$0.5V_{dc}$
0	1	0	1	1	0	1	0	0
0	1	1	0	1	0	1	0	$-0.5V_{dc}$
0	1	0	1	0	1	1	0	$-V_{dc}$
0	1	1	0	0	1	1	0	$-1.5V_{dc}$

3. LEVEL SHIFTED CARRIER BASED PWM TECHNIQUE

This modulation technique is based on the comparison of a sinusoidal reference signal with carrier signals (having same frequency) which are usually selected triangular pulses. Due to its simplicity and popularity of this technique, we would be analyzed in this paper in details and would be used as the modulator of this multilevel inverter.

The carrier-based PWM techniques can be classified into two types: phase shifted and level shifted modulations. Both modulation schemes can be applied to the ACMLI but the THD of phase shifted is much higher than level shifted modulation. Therefore we had considered level shifted modulation schemes.

An m-level proposed multilevel inverter using level shifted multicarrier modulation schemes requires $(m-1)$ triangular carriers, all having the same frequency f_c and amplitude A_c. The $(m-1)$ triangular carriers are vertically disposed such that the bands they occupy are adjacent to each other. The reference waveform has amplitude of A_m and frequency of f_m and it is placed in the middle of the six carriers. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the device switches off.

The frequency modulation index is given by:

$$m_f = f_c / f_m \quad \text{.....} \quad (2)$$

Whereas the amplitude modulation index is defined as:

$$m_a = A_m / A_c(m-1) \quad \text{..... (3)}$$

In this paper the simulated waveforms for seven level ACMLI operating under the conditions of $m = 7, A_m = 3, A_c = 0.5, m_a = 1, V_{dc} = 210V, f_c = 2850Hz$ & $f_m = 50Hz$. There are three types of level shifted carrier-based PWM techniques as follows:

3.1 Phase Disposition Technique (PD)

The vertical offset of carriers for 7-level ACMLI with PD technique is illustrated in Fig 3. It can be seen that all six carriers are adjacent to each other with same phase and the reference sine wave is placed in the middle of the six carriers.

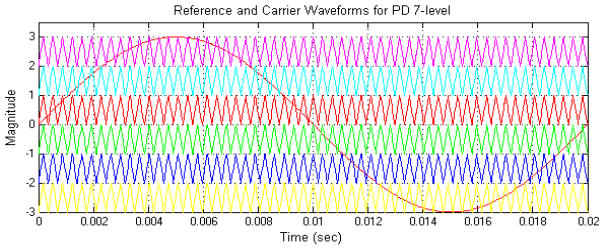

Fig 3: Reference and Carrier Waveforms for PD 7-Level

3.2 Phase Opposition Disposition Technique (POD)

The vertical offset of carriers for 7-level ACMLI with POD technique is illustrated in Fig 4. It can be seen that they are divided equally into two groups according to the positive / negative average levels. In this type the two groups are opposite in phase with each other while keeping in phase within the group. The reference sine wave is placed in the middle of the six carriers.

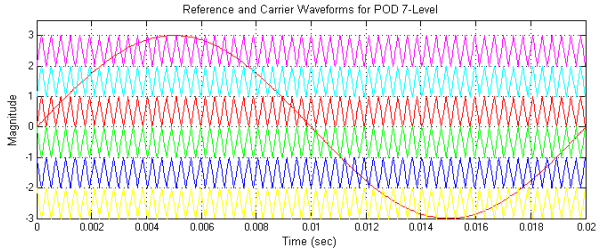

Fig 4: Reference and Carrier Waveforms for POD 7-Level

3.3 Alternative Phase Opposition Disposition (APOD) Technique

The vertical offset of carriers for 7-level ACMLI with APOD technique is illustrated in Fig 5. In this technique, all carriers are opposite in phase with each other and the reference sine wave is placed in the middle of the six carriers.

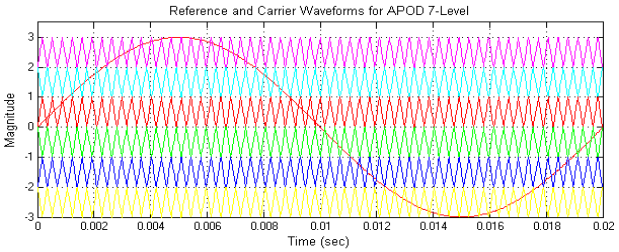

Fig 5: Reference and Carrier Waveforms for APOD 7-Level

4. STUDY CASE IMPLEMENTED IN MATLAB

The simulation of three phase seven level asymmetrical cascaded H-Bridge multilevel inverter is carried out using MATLAB/SIMULINK as shown in Fig 6. Here the subsystem for pulse generator is modeled where one reference wave (sine wave) and six carrier signals (triangular wave) are taken. First three triangular wave is applied across the positive half cycle of the sine wave and the second three triangular wave is applied across the negative half cycle of the sine wave.

Based on the concepts explained in modulation techniques, eight pulses are generated. These pulses are given to the switches in one phase leg of a seven level ACMLI. Similarly the pulses are generated for remaining two phases, just by changing phase shifting angle of modulating signal by 120 degrees. Fig 7: represents the one phase leg of a 7-level ACMLI and Fig 8: represents the logic circuit of a 7-level ACMLI.

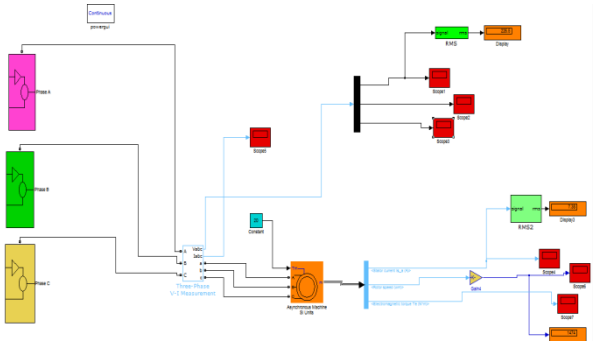

Fig 6: Simulation model of a three phase 7-level ACMLI

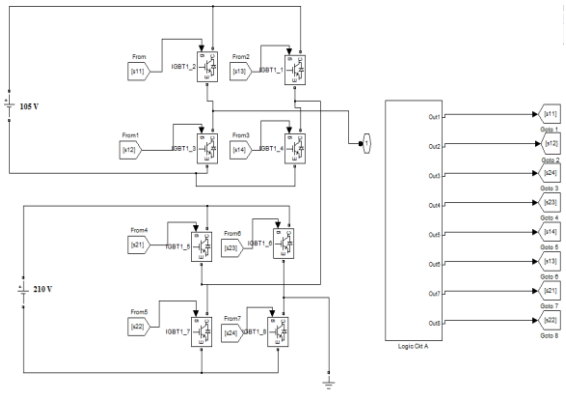

Fig 7: One phase leg of a 7-level ACMLI

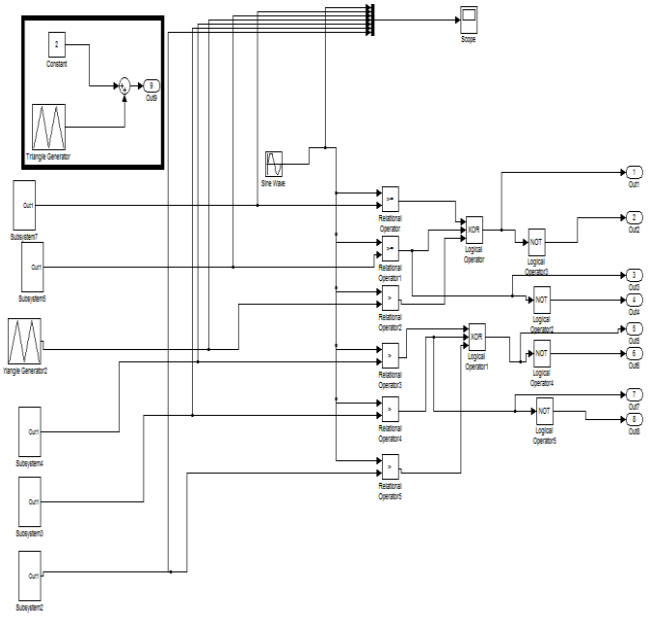

Fig 8: Logic circuit of a 7-level ACMLI

5. SIMULATION RESULTS

The topology presented in this paper employs six carriers level shifted by particular amplitude. The performance analysis has been carried using a three phase squirrel cage induction motor and an asymmetrical cascaded H-Bridge multilevel inverter has been used for the analysis. The parameters of the motor are specified in Table 2.

Table 2. Ratings of Three Phase Induction Motor

Voltage (L-L) V_{L-L}	400 V
Frequency f	50 Hz
Nominal Power of Motor P_o	10 HP (7.5KW)
Rated Speed N_r	1440 rpm
Rated Current I	10.825 Amp
Load Torque T_l	20 N-m
No. of Poles P	4

The output voltage waveform for phase A of seven level asymmetrical cascaded H-Bridge multilevel inverter with three phase squirrel cage induction motor as a load using PD-LSCPWM technique is shown in Fig 9: and its FFT analysis is shown in Fig 10. The same voltage waveform using POD-LSCPWM is shown in Fig 11: and its FFT analysis is shown in Fig 12. And using APOD-LSCPWM is shown in Fig 13: and its FFT analysis is shown in Fig 14.

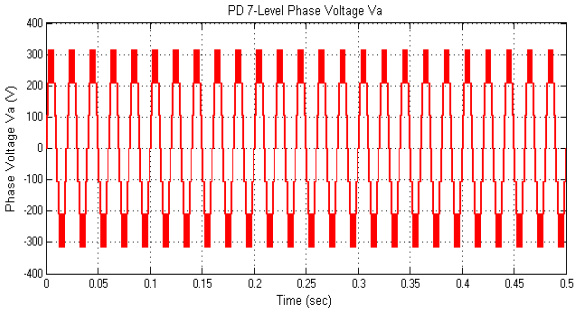

Fig 9: PD 7-Level Phase Voltage V_a

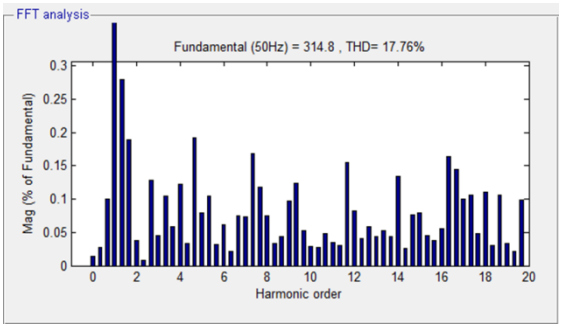

Fig 10: Harmonic Spectrum of 7-level phase voltage ACMLI using PD LSPWM

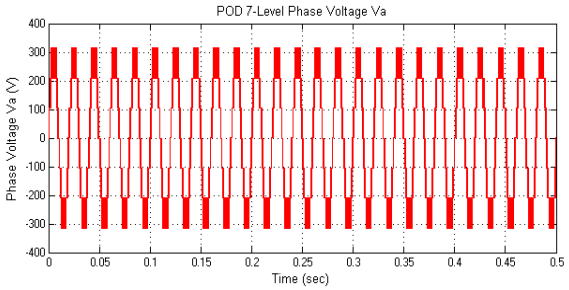

Fig 11: POD 7-Level Phase Voltage V_a

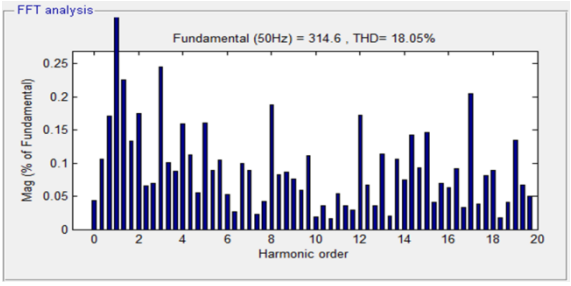

Fig 12: Harmonic Spectrum of 7-level phase voltage ACMLI using POD LSPWM

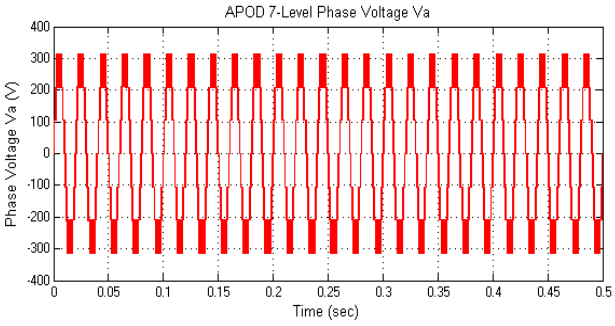

Fig 13: APOD 7-Level Phase Voltage V_a

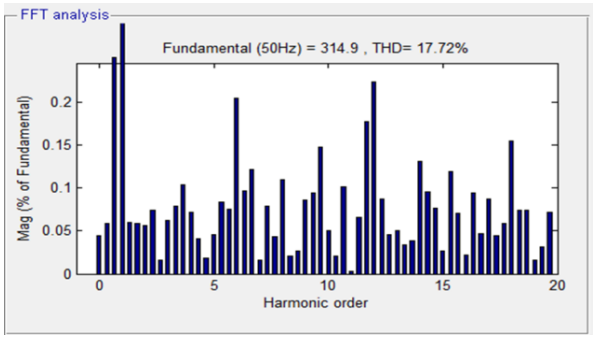

Fig 14: Harmonic Spectrum of 7-level phase voltage ACMLI using APOD LSPWM

The speed, stator winding current and the torque of the induction motor are observed and are shown below. The speed, three phase stator winding current and torque of the induction motor for 0.5 sec are shown in Fig 15, Fig 16, Fig 17 and Fig 18.

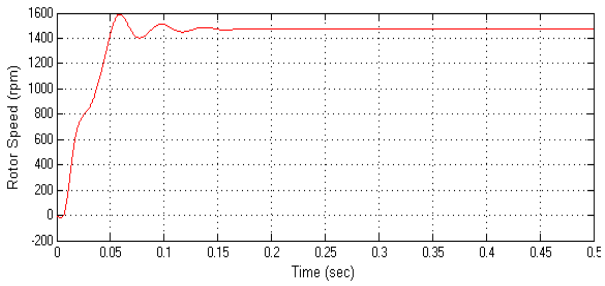

Fig 15: Rotor speed

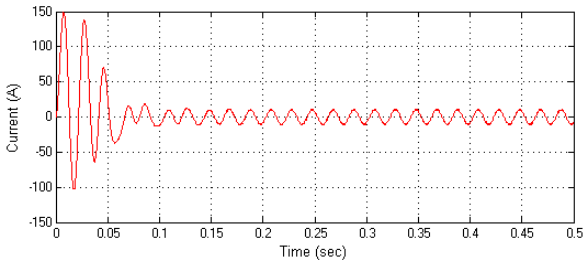

Fig 16: Phase A stator current I_a

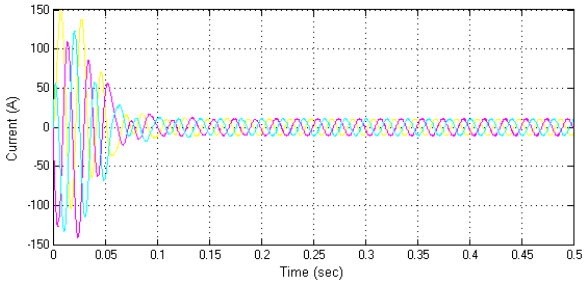

Fig 17: Three phase stator current

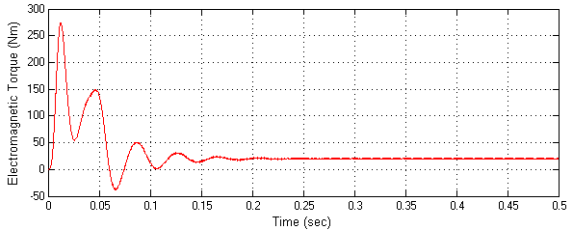

Fig 18: Electromagnetic Torque

The THD of the phase voltage V_a of an asymmetrical CMLI is compared for all the three LSCPWM technique i.e. PD, POD, APOD is shown in Table 3.

Table 3. Comparison of LSCPWM

LSCPWM	PD	POD	APOD
THD%	17.76	18.05	17.72

6. CONCLUSIONS

In an asymmetrical topology, seven level output voltage is generated by using only 2 H-Bridges (8 switches) whereas in symmetrical topology 3 H-Bridges (12 switches) needed to generate the same no. of levels, therefore the number of switches are reduced in asymmetrical topology compared to symmetrical topology for the same no. of levels. The THD of the phase voltage of an asymmetrical CMLI is studied under different modulation techniques such as PD, APOD, and POD and the less THD is observed for APOD technique i.e. 17.72%. If the number of H-Bridges is boundless, the output voltage levels are infinite, which is similar to the analogue one. However a large number of H-Bridges can be a cause of cost increase, controlling and manufacturing problems. Therefore, it should be selected considering the amplitude of input voltage, the THD of output voltage, and the system price.

7. ACKNOWLEDGEMENTS

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