Charge Conservation Technique to Reduce Dynamic Power of Class AB Amplifier for LCD using LTSpice

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ABSTRACT
A complementary differential amplifier which has RAIL TO RAIL feature with offset cancellation technique to enhance high color depth and high-resolution liquid crystal display (LCD) drivers, is proposed. The dual complementary differential pairs are used to obtain RAIL TO RAIL input-output swing and an offset canceling capability. Both offset voltage and injection-induced error, due to mismatch of device and charge injection, are greatly reduced. The offset cancellation and charge conservation, which is used to reduce the dynamic power consumption, are operated during the same time slot so that the driving period does not need to increase. It is implemented using LTSPICE simulation.

General Terms
Liquid crystal Display, Low power design, Charge sharing, Offset voltage cancellation, Buffer Amplifier.

Keywords
CMOS, Class AB amplifiers, Rail-to-Rail, Push-pull stage, Complementary differential pair, transconductance amplifiers.

1. INTRODUCTION
WITH the progressive progression of Liquid Crystal Drivers, there is an expansive interest for creating high-determination and high shade profundity driver ICs [1]–[8]. LCD boards made for multimedia products have ended up bigger with higher definition, and their color quality requires more sharpness. For LCD-TV applications, the drivers must change over 10-bit computerized info codes to simple levels, at which point the implicit cradle enhancers drive the highly capacitive information lines [9]–[11].

The cradle amplifiers focus the pace, determination, voltage swing, and force scattering of the LCD drivers [3]–[7]. In an amazing presentation module, the amplifier has to have a higher resolution, and it ought to offer a practically rail-to-rail voltage driving to suit the increasing resolution of DACs . The settling time of the buffer amplifier ought to be shorter than the even filtering time for better stability of the system. Likewise, the balance voltage ought to be extraordinarily decreased to accomplish high color profundity. Enhancers for LCD applications have been proposed and exhibited in late work.

Case in point, P.C.Yu et al [4] proposed a class b output buffer for flat panel column driver. Two low power area efficient complementary push pull buffer amplifiers provide sufficient dyanamic range with low bias currents using a bias control mechanism. Ito et al. [12] proposed a rail-to-rail class-AB amplifier for LCD drivers, in which the quantity of current required by the circuit path is reduced and the phase compesation is suitable for rapid operation of data drivers. D. Marano et al [13] proposed a reduced, low-power, and rail-to-rail class-B buffer amplifier for driving the expansive segment line capacitance of LCDs, in which a nonlinear component in the input path is changed from the current-mirror amplifier so as to acquire region and force points of interest. Lu et al [6] proposed a rapid driving plan and a minimal high velocity low-power rail-to-rail class-B cradle enhancer, which is suitable for both little and expansive size LCD applications. It incorporated an inversion controller which was attached to the column driver for rail-to-rail operation. The buffer amplifier employs a single comparator to sense transients of the input. This increases the speed without increasing static power consumption.

Itakura et al [18] proposed a low balance high output voltage swing rail-to-rail support enhancer for LCD driver, in which the nonlinearity of the yield voltage is decreased. Crisscross of the gadgets causes a balance voltage, which constrains the high-determination for LCD driver application. A few strategies are proposed to diminish the counterbalance voltage.For instance, "yield balance stockpiling" and "data counterbalance stockpiling" strategies measure the counterbalance voltage and store the result on capacitors in arrangement with the yield/information. Nonetheless, these two procedures present capacitors in the indicator way, an important and genuine issue in op-amps and input framework.

For the determination of the above issues, a counter balance abrogation plan is introduced, which can confine the indicator way from the balance stockpiling capacitors through the utilization of a helper enhancer, as was proposed previously [16]. A push-pull stage is frequently utilized in buffer design as a part of CMOS support amplifiers. The push-pull stage comprises of two corresponding basic source transistors, permitting rail-to-rail yield output voltage swing.

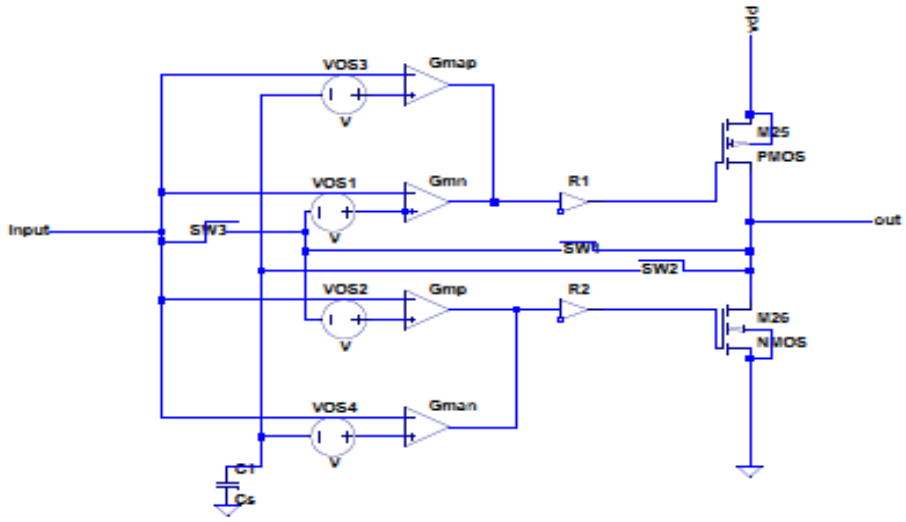

Figure 1: Architecture of proposed amplifier with offset cancellation

In this work the single ended differential amplifiers are to drive the output stage to achieve offset cancellation. Under class AB operation no extra path for current is needed. The two single ended differential amplifiers act as a complementary differential pair at the input stage to obtain the full swing and also act as offset cancellation network with the help of switch capacitor. The offset voltage is caused due to mismatch and process variation. By proper design of a differential amplifier we reduced the injection- induced error of switch capacitor amplifier. The offset and charge conservation are greatly reduced the dynamic power consumption as both are operated in same time slot in driving. In charge conservation firstly the output buffer is isolated from output then the output of buffer is connected with the charge storage capacitor which is holed with the previous phase charge. When input is applied this charge is also provided to output of buffer using negative feedback to cancel the offset. During charge conservation no static current will flow at output stage so power dissipation is minimized.

2. PROPOSED AMPLIFIER WITH OFFSET CANCELLATION

The structure of the proposed buffer amplifier is shown in fig 1 is divided into two stages. In first stage four trans-conductance amplifiers G_{map}, G_{mn}, G_{mp}, and G_{map}; and the trans-conductance amplifiers R1 and R2 are used in the second stage as a pair of complementary common source amplifiers. We further divide the first stage into main and auxiliary trans-conductance amplifiers, G_{mn}, G_{mp}, are our main trans-conductance amplifier, G_{man}, G_{map} are auxiliary transconductance amplifier, G_{map}, G_{mp} are the PMOS input differential pair similarly G_{man}, G_{mn} are the NMOS input differential pair, the output complementary common source amplifiers are used to drive the LCD panel and the second stage as to achieve push-pull and RAIL TO RAIL differential oputput we use the single ended amplifiers to drive the output device, PMOS and NMOS main and auxiliary transconductance amplifiers are combined to make dual complementary differential pair , thus when the input is near the voltage VDD G_{map}, G_{mp} are cut off but G_{man}, G_{mn} amplify the input signal to output stage through two transconductance impedance amplifiers R1 & R2 . The use of transimpedance amplifiers is to combine the current from the main and auxiliary transconductance amplifiers. The auxiliary transconductance amplifiers are used to extend the input string. We use three switches and a charge storage capacitor at the input stage of auxiliary transconductance amplifiers as shown in the above figure 1 called as offset storage capacitor. As the input stage contains both PMOS and NMOS differential amplifiers, the offset voltage varies with input voltage regularly and we can drive the LCD pixel for high color resolution. This offset reduction technique makes a large difference, so the auxiliary transconductance amplifiers are used with the help of offset storage capacitor to remove offset voltages.

The whole operation is conducted in two phase offset cancellation phase and driving output phase. In offset cancellation phase SW2 & SW3 are on and SW3 is off. When offset is completed, the process is reversed to drive the load capacitance. A negative feedback loop is formed by auxiliary transconductance amplifiers and two main transconductance amplifiers, and the output push-pull transistors. During transition phase input voltage is applied to all auxiliary and primary transconductance amplifiers at input terminal as shown in the figure 1 were Vos1, Vos2,Vos3,Vos4 are the referred offset voltage

$$\begin{aligned}\{[\pm V_{OS1}g_{mn} + (V_{out} - V_{in} \pm V_{OS3})g_{map}\,]R_1 g_{m25} \\ + [\pm V_{OS2}g_{mp} \\ + (V_{out} - V_{in} \\ \pm V_{OS4})g_{man}\,]R_2 g_{m26}\}R_{out} \\ = V_{out}\end{aligned} \quad (1)$$

$$V_{out} = \frac{\begin{bmatrix} V_{in}(g_{map}\,g_{m25}R_1 + g_{man}\,g_{m26}R_2) \pm \\ (V_{OS1}g_{mn} + V_{OS3}g_{map})g_{m25}R_1 \pm \\ (V_{OS2}g_{mp} + V_{OS4}g_{man})g_{m26}R_2 \end{bmatrix} R_{out}}{(g_{map}\,g_{m25}R_1 + g_{man}\,g_{m26}R_2)R_{out} - 1} \quad (2)$$

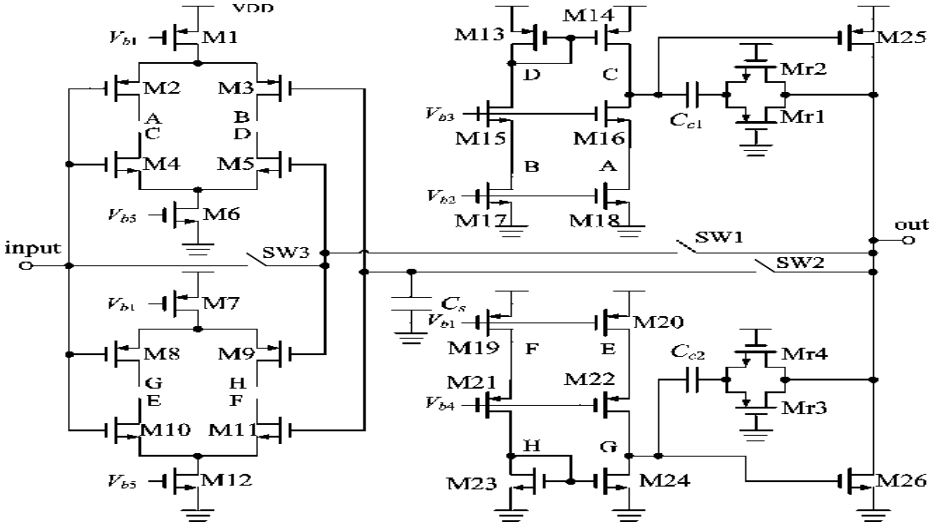

Figure 2: Schematic of the proposed amplifier with offset cancellation

g_{m25} & g_{m26} are the transconductance of M25 & M26 and R_{out} is the output resistance of the amplifier.Assume g_{m25} = g_{m26} and $R_1 = R_2$ then V_{out} is,

$$\cong V_{in} \pm V_{OS1} g_{mn} g_{m25} R_1 \pm V_{OS2} g_{mp} g_{m26} R_2 + \frac{\pm V_{OS3} g_{map} g_{m25} g_{man} g_{m26} R_2}{g_{map} g_{m25} R_1 + g_{man} g_{m26} R_2} \quad (3)$$

assume g_{m25} = g_{m26} and $R_1 = R_2$ then

$$V_{out} \cong V_{in} + \frac{\pm V_{OS1} g_{mn} \pm V_{OS2} g_{mp}}{\pm V_{OS3} g_{map} \pm V_{OS4} g_{man}} \quad (4)$$

When SW2 andSW3 were off and SW1 is on, the output voltage is stored at the capacitance called as output offset voltage which is,

$$V_{out} - V_{in} \cong \frac{\pm V_{OS1} g_{mn} \pm V_{OS2} g_{mp}}{\pm V_{OS3} g_{map} \pm V_{OS4} g_{man}} \quad (5)$$

The total output of the voltage referred to the input is given as

$$V_{OS,tot} = \frac{V_{out} - V_{in}}{A_{dc}} = \frac{\pm V_{OS1} g_{mn} \pm V_{OS2} g_{mp}}{(g_{map} + g_{man}) A_{dc}} \quad (6)$$

Where A_{DC} is the DCgain of the amplifier,it is the order of 80 dB. Equation 1 shows output from the buffer, with offset considered at primary and auxiliary amplifier and equation 5 shows the total offset at output of buffer, the switch SW2 will introduce injection induced error. Input referred offset voltage expressed as;

$$V_{OS,inj} = \left(\frac{g_{map} + g_{man}}{g_{mn} + g_{mp}}\right) \Delta V \quad (7)$$

Where ΔV is the injection induced error on the storage capacitor. To reduce the center the transconductance the transconductance of main transconductance amplifier is designed to be higher than auxiliary transconductance amplifier. Figure 2 shows schematic diagram of proposed buffer. In this methodology charge conservation technology is used to reduce the power consumption as shown in Fig 3

In this process the data line are divided into three phase. In the first phase all data lines are isolated from the output of the buffers. In second phase they are shorted with external capacitor, this two phases are used to conserve charge on data line. In the last phase all data lines are connected with output buffer to drive the data line to their final values. This charge conservation technique eliminates the need of additional phase consideration for the buffer amplifier which means the driving time does not need to be elongated.

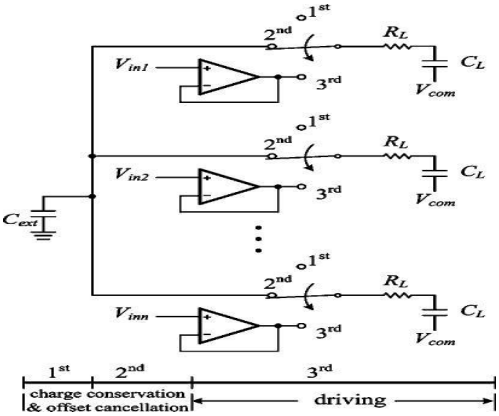

Figure3: Generalized diagram of charge observation technology

3. 3. SIMULATION AND RESULTS

The buffer is implemented in .35µm CMOS technology using LTSPICE simulation tool, the circuit draws 4µA static current for voltage supply of 5V under 3.4 kΩ resistance and 140pF load capacitance. The obtained value of offset voltage is .3mV.As can be inspected, the output voltage basically follows the input voltage for a full dynamic range.

Slew-rate values obtained are 12V/µs and 14V/µs for the rising and falling edges respectively, whereas positive and negative settling time values are within 100% of the final output voltage. They are 3µs and 3.7µs, respectively. As can be observed, the output waveform follows the input waveform.

A. Using LTSPICE

Fig 4 shows schematic of buffer without offset cancellation scheme, fig 5 show schematic with offset cancellation scheme which is implemented by using 3 switches and a storage offset voltage capacitor, fig 6 shows value of offset voltage value without offset cancellation which is 9mV, Fig 7 shows value of offset after offset cancellation which is 0.3µV.

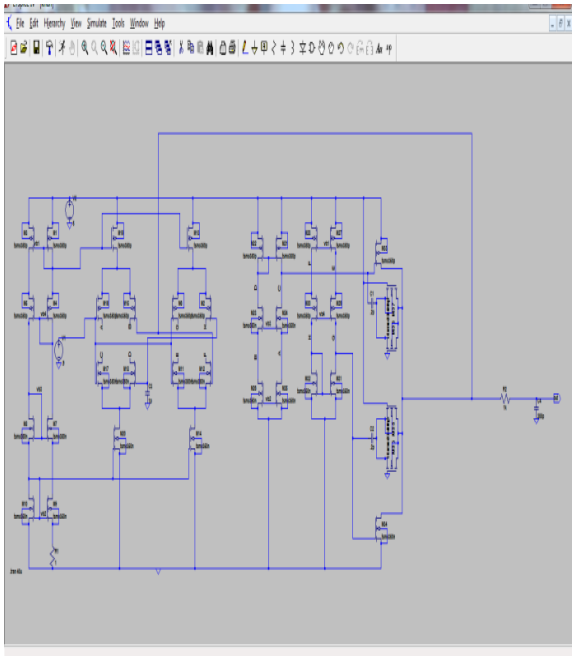

Figure 4: Schematic of proposed buffer without offset cancellation

Figure 8 and 9 shows transient output response of the buffer with rectangular and triangular wave having 50 kHz signal frequency. Simulation is implemented using LTSpice for with and without offset voltage cancelation respectively, Figure 10 presents the AC response of the signal ant it shows that with applied input frequency the phase and gain is constant and it shows the stability with the applied signal frequency.

The major performance parameters of the analyzed buffer are summarized and compared to other conventional topologies in Table 6.1, which shows a remarkable improvement of the proposed amplifier over other previously reported buffer interims in tems of offset voltage which is .3 µV, area, settling time,DC gain,phase margin, unity gain frequency.

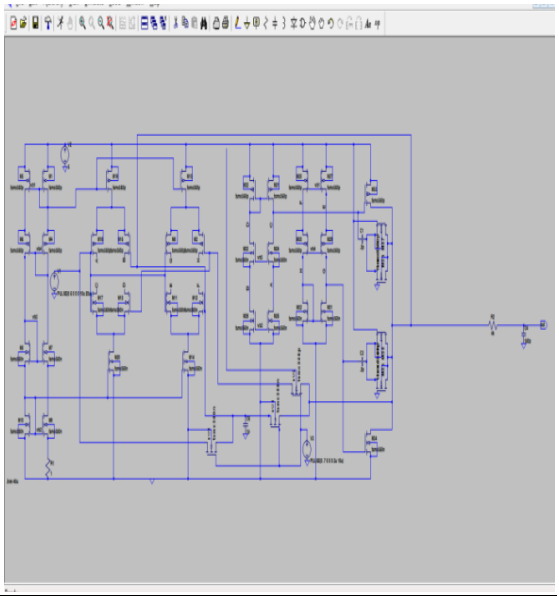

Figure 5: Schematic of proposed buffer with offset cancellation

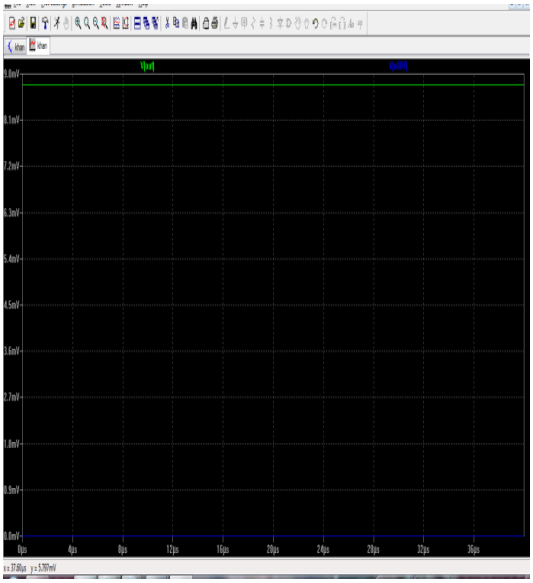

Figure 6: Offset of proposed buffer without offset cancellation is 9mV

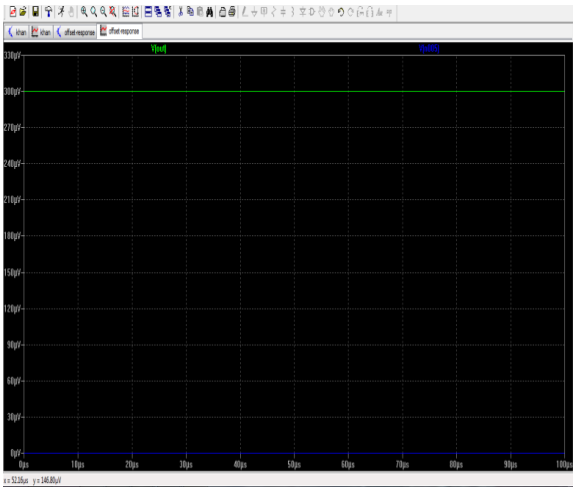

Figure 7: Offset of proposed buffer with offset cancellation is 0.3µV

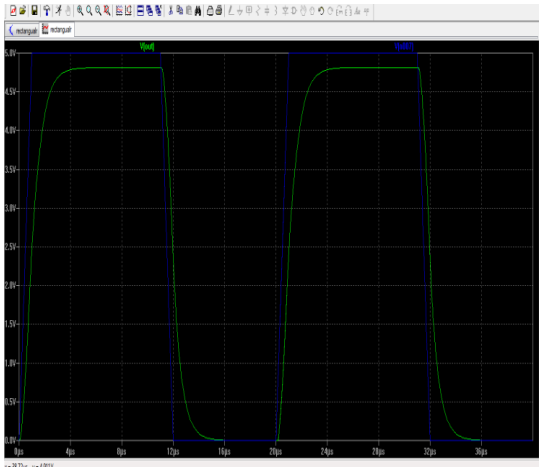

Figure 8: Output response to square pulse of 20u to proposed buffer with offset cancellation at output load of 140pf

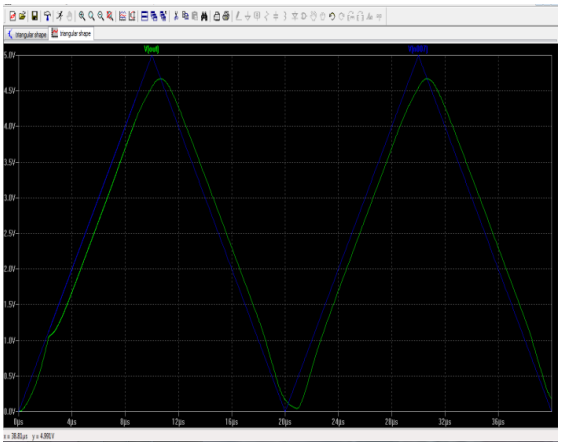

Figure 9: Output response to triangular pulse of 20u to proposed buffer with offset cancellation at output load of 140pF

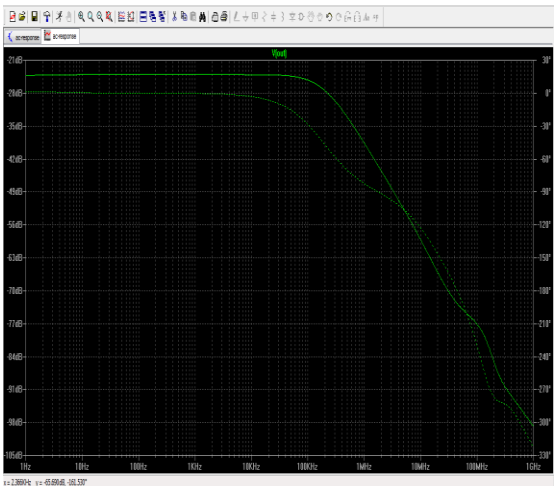

Figure 10: AC response of the proposed buffer with offset cancellation (frequency-phase plot)

Table 1 Comparision table

Parameter	**[12] IQ Ito's amplifier**	**[13] Weng's amplifier**	**Hong's [14] amplifier**	**This work**
Process technology	.35 µm CMOS	.35 µm CMOS	.35 µm CMOS	.35 µm CMOS
VDD	5 V	3.3 V	5 V	5 V
Input-output ranges	0.5-4.5 V	.05-3.25 V	0-5 V	0-5V (100% VDD)
Quiescent current	2 µA	7.4 µA	NA	7 µA
DC gain	NA	65db	NA	88db
Unity gain frequency	NA	750KHz	NA	3.5 MHz
Phase margin	NA	50^0	45^0	109^0
Settling time	1.95 µs(24 Pf Load)	8µs(600pF Load)	.95µs(400Pf Load)	3µs(140pF Load)
Offset voltage	NA	NA	NA	.3 mV
Act ive area	100* 46µ m²	100*100 µm²	86*74 µm²	100*50 µm²

4. CONCLUSION

It is limpidly visually perceived in the results that the output waveform follows the input waveform. Withal the comparison table depicts a remarkable amelioration of the proposed amplifier over other intecedently reported buffers. Hence the high speed self inequitable low power rail-to-rail class-AB low offset buffer amplifier is implemented prosperously. Since the dissertation topic implements a very compact, high speed rail-to-rail buffer for LCD drivers, it can be utilized as a boon in many future applications where die area is a matter of concern, additionally where slew rates is a matter of concern. Since power consumption is low, it has a great future in getting utilized in applications like "ultra low power ADCs", utilized in "image exhibit contrivances, flat panel exhibits etc. Due to rail-to-rail input and output cognations, it is utilized in buffered analog clocks .Above are just few examples, but this buffer is having excellent usability in many other areas also.

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6. REFERENCES

[1] T. Itaku, H. Minamizaki, T. Satio, and T. Kuroda, "A 402-output TFT-LCD driver IC with power control based on the number of colors selected," IEEE J. Solid-State Circuits, vol. 38, no. 3, pp. 503–510, Mar. 2003.

[2] J.-S. Kim, D.-K. Jeong, and G. Kim, "A multi -level multi-phase charge-recycling method for low-power AMLCD column drivers," IEEE J. Solid-State Circuits, vol. 35, no. 1, pp. 74–84, Jan. 2000.

[3] Y.-S. Son, J.-H. Kim, H.-H. Cho, J.-P. Hong, J.-H. Na, D.-S. Kim, D.-K. Han, J.-C. Hong, Y.-J. Jeon, and G.-H. Cho, "A column driver with low-power area-efficient push-pull buffer amplifiers for active-matrix LCDs," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 2007, pp. 142–143.

[4] P.-C. Yu and J.-Wu, "A class-b output buffer for flat-panel-display column driver," IEEE J. Solid-State Circuits, vol. 34, no. 1, pp. 116–119, Jan. 1999.

[5] T. Itakura and H. Minamizaki, "A two-gain-stage amplifier without an on-chip miller capacitor in an LCD driver IC," IEICE Trans. Fundamentals, vol. E85-A, no. 8, pp. 1913–1920, Aug. 2002.

[6] C.-W. Lu and K. J. Hsu, "A high-speed low-power rail-to-rail column driver for AMLCD application," IEEE J. Solid-State Circuits, vol. 39, no. 8, pp. 1313–1320, Aug. 2004.

[7] C.-W. Lu and C. L. Lee, "A low power high speed class-AB buffer amplifier for flat panel display application,"

IEEE Trans. VLSI Syst., vol. 10, no. 2, pp. 163–168, Apr. 2002.

[8] Gordon and F. Dingwall, "Matrix addressed LCD display having LCD age indication, and autocalibrated amplification driver, and a cascaded column driver with capacitor-DAC operating on split groups of data bits," U.S. Patent 5,739,805, Apr. 14, 1998.

[9] M. J. Bell, "An LCD column driver using a switch capacitor DAC," IEEE J. Solid-State Circuits, vol. 40, no. 12, Dec. 2005.

[10] M. J. Bell, "An LCD column driver using a switch capacitor DAC," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers., Feb. 2005, pp. 556–557.

[11] J.-S. Kang, J.-H. Kim, S.-Y. Kim, J.-Y. Song,O.-K. Kwon, Y.-J. Lee, B.-H. Kim, C.-W. Park, K.-S. Kwon, W.-T. Choi, S.-K. Yun, I.-J. Yeo, K.-B. Han, T.-S. Kim, and S.-I. Park, "A 10b driver IC for a spatial optical modulator for full HDTV applications," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers., Feb. 2007, pp. 138–592.

[12] R. Ito, T. Itakura, and H. Minamizaki, "A class AB amplifier for LCD driver," in 2007 Symp. VLSI Circuits Dig. Tech. Papers, Jun. 2007, pp. 148–149.

[13] A New Compact Low-Power High-Speed Rail-to-Rail Class-B Buffer for LCD Applications Davide Marano, Gaetano Palumbo, Fellow, IEEE, and Salvatore Pennisi, Senior Member, IEEE JOURNAL OF DISPLAY TECHNOLOGY, VOL. 6, NO. 5, MAY 2010

[14] D. J. R. Cristaldi, S. Pennisi, and F. Pulvirenti, Liquid Crystal Display Dr Techniques and Circuits. New York: Springer, Mar. 2009.

[15] S. Di Fazio, S. Pennisi, F. Pulvirenti, and T. Signorelli, "670-nACMOS OTA for AMLCD column driver," J. Circuits, Syst., Comput., vol. 18, no. 2, pp. 339–350, Apr. 2009.

[16] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," IEEE J. Solid-State Circuits, vol. 29, no. 12, pp. 1505–1513, Dec. 1994.

[17] T. Itakura, "A high slew-rate operational amplifier for an LCD driver IC," IEICE Trans. Fundamentals, vol. E78-A, no. 2, pp. 191–195, Feb. 1995.

[18] T. Itakura and H. Minamizaki, "10- µAquiescent current opamp design for LCD driver ICs," IEICE Trans. Fundamentals, vol. E81-A, no. 2, Feb. 1998

[19] C.-W. Lu, "Low-power high-speed class-AB buffer amplifiers for liquid crystal display signal driver application," J. Circuits, Syst., Comput., vol. 11, no. 4, pp. 427–444, Aug. 2002.