Reduction of Leakage Power in Half- Subtractor using AVL Technique based on 45nm CMOS Technology

Anand Singh Narwariya
M.Tech (VLSI design) Student
ITM Gwalior, India

Shyam Akashe
EC Department Professor, EC Department
ITM University, Gwalior, India

ABSTRACT
The analytical paper of arithmetic circuits plays an important role in designing of any VLSI system. Subtractor is one of them. Half Subtractor is being designed using Adaptive Voltage Level (AVL) techniques. This design consumed less power as compare to conventional design. We can reduce the value of total power dissipation by applying the AVLG (adaptive voltage level at ground) technology in which the ground potential is raised and AVLS (adaptive voltage level at supply) in which supply potential is increased. This paper represents how to control power using AVL techniques. The AVL technique based Half Subtractor compared to conventional design that based on power consumption, propagation delay, speed and layout area is more preferred. Power consumption of the projected cell is measured and compared. The result shows that there is a significant reduction in power consumption for this proposed cell with the AVL technique. This styal is much useful in designing the system that consumed less power. The circuit is simulated on Cadence tools in 45 nanometer CMOS technology.

Keywords
Half–Subtractor, AVLG techniques, AVLS techniques, Low Power and High Speed

1. INTRODUCTION
In very large scale integration the increasing demand for low power can be addressed at different logic levels, such as circuit, architectural and layout. At circuit design level considerable amount of power can be saved by means of proper choice of a logic design. The proper choice of a logic design is important because all important parameters governing power dissipation- switching capacitance, transition activity, and short circuit currents are strongly influenced by the chosen logic design [1]. The increasing eminence of portable systems and the need to limit power consumption in very high density ULSI chips have led to rapid and very interesting developments in low-power design in recent years [2]. A one such combinational circuit that performs the subtraction of two bits is called a Half Subtractor. The digit from which another digit is subtracted is called the minuend and the digit which is to be subtracted is called the subtrahend. There are a number of logic designs by which a circuit can be implemented some of them used in this paper are CMOS, AVL technique. CMOS logic designs are robust against voltage scaling and transistor sizing and thus provide a reliable operation at low voltages and arbitrary transistor sizes [3]. In CMOS design input signals are connected to transistor gates only, which facilitate the usage and characterization of logic cells. Due to the complementary transistor pairs the layout of CMOS gates is not much complicated and is power efficient. The large number of PMOS transistors used in complementary CMOS logic design is one of its major disadvantages and it results in high input loads [4]. The transmission gate is simply the combination of two complementary transistors. These gates are more often used internally in larger scale CMOS devices because of its simplicity and low propagation delay. The advantage of pass transistor logic is that it uses smaller number of transistors and smaller input loads, especially when NMOS transistors are used. Thus in this paper the use of AVL technique has been made for the reduction of power dissipation. Power dissipation in any Half Subtractor circuit depends on both static and dynamic power dissipation [5]. The static power dissipation is the product of the leakage current and supply voltage. The leakage current is described by the equation

$$I_o = I_s\,(e^{qV/kT} - 1) \qquad (1)$$

Where, I_s = reverse saturation current, V= diode voltage, q= electronic charge, k= Boltzmann's constant, T= temperature.

The static power dissipation is the product of the leakage current and supply voltage. The total static power dissipation P_s is given by

$$P_s = \sum_1^n I_{leakage} \times V_{dd} \qquad (2)$$

Where n = no of devices

2. HALF SUBTRACTOR
The Conventional Half Subtractor may be a combined circuit which can be used to perform subtraction of two binary digits. It has two inputs A (minuend) and B (subtrahend) and two outputs D (difference) Y (borrow). Functionally, the Half Subtractor uses the gate level circuit. The Symbol of Half Subtractor using with XOR gate, AND gate and Inverter are implemented shows with in the Half Subtractor [6].

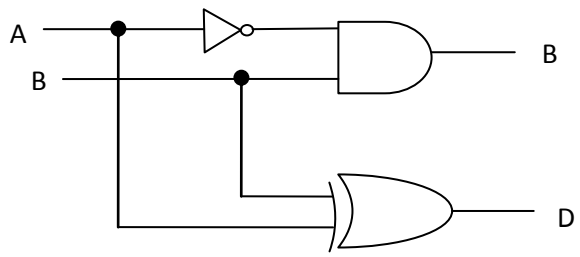

Fig.1 Gate Level Design of Half Subtractor

The Truth Table below shows the operation of Half Subtractor:

Table (1) Truth Table of Half Subtractor

A	B	Bout	Diff
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$\text{Diff} = A'B + AB' \qquad (3)$$

$$Y(\text{borrow}) = A'B \quad (4)$$

In conventional Half-Subtractor [7], a simple transistor level circuit is designed. Where, all N-MOS are connected to ground terminal and all P-MOS are connected to Source terminal. The circuit is designed using CMOS Circuit. Leakage current [8] also place a vital role in designing of any system. It should be as low as possible. Power consumption is also an important parameter in system design.

3. HALF SUBTRACTOR USING AVL TECHNIQUE

An adaptive voltage level technique [9] [10], can be used to control circuits and it can be used either at the upper end of the cell to bring down the supply voltage value, called AVLS technique. By this technique reduction of power dissipation is occurred. The power dissipation is reduced less than conventional design cell. The complete effect of these techniques on the power consumption is described as follows. In the literature [11] [12], the half subtractor is implemented with two different techniques called the AVLG and AVLS techniques. Fig. 2 and 3 shows the half subtractor using AVLG and AVLS technique on 45nm.

3.1 Half Subtractor using AVLG

In AVLG technique, a combination of 1-N-MOS & 2-P-MOS are connected in parallel. So that a input clock pulse is applied at the N-MOS of circuit of AVLG and rest of all P-MOS are connected to ground. This AVLG circuit is connected at the ground terminal of conventional one by removing ground. This ground terminal is connected to the AVLG circuit. Fig. 2 shows the Half Subtractor designed using AVLG technique.

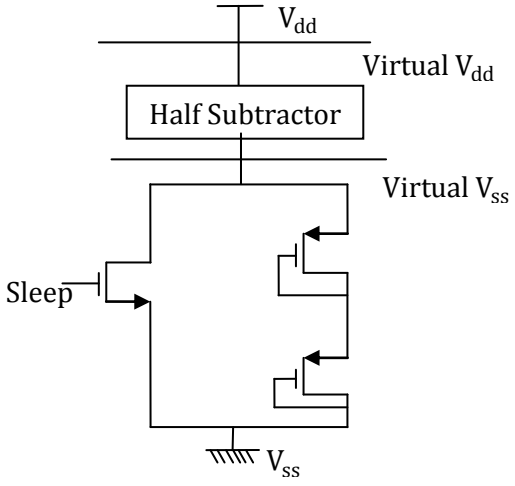

Fig. 2 AVLG Technique of Half Subtractor

Table 2 shows the truth table of Half Subtractor using AVLG technique. Depending upon the clock and inputs, variation in output is varied. In AVLG technique shown in Fig. 4 which the supply voltage is reduced and AVLG (Adaptive Voltage Level at Ground) in which the ground potential is increased are used. In AVLG Technique the adaptive voltage level control circuit is used at the lower end of the cell to lift the potential of the ground node. The use of AVLG Technique decreases the power consumption through an Half Subtractor. Therefore, this approach is useful in lowering the final value of the power consumption [13]. This technique makes use of supply voltage. At V_{dd} = 0.7 V, Power consumes 1.21µW power.

The Truth Table below shows the operation of Half Subtractor:

Table (2) Truth Table of Half Subtractor

A	B	Bout	D
0	0	X	X
0	1	1	1
1	0	X	X
1	1	0	0

Layout of Half Subtractor with AVLG Technique

In fig. 3 shows the Layout of Half Subtractor with Adaptive Voltage Level at Ground (AVLG) Technique in which used an extra circuitry for controlling the leakage current. The AVLG is connected to ground source.

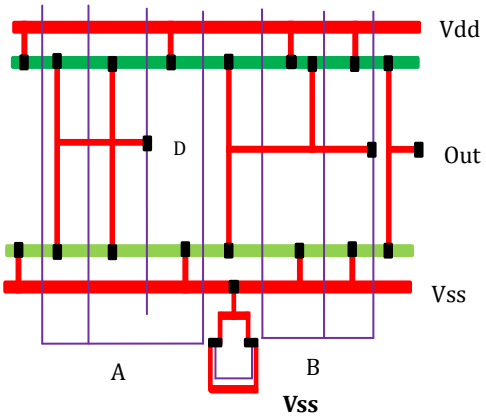

Fig. 3 Layout of Half Subtractor with AVLG Technique

3.2 Half Subtractor using AVLS

In AVLS technique, a combination of 2- N-MOS & 1-P-MOS are connected in parallel. So that a input clock pulse is applied at the P-MOS of circuit of AVLS and rest of all N-MOS are connected to drain terminal. This AVLS circuit is connected at the voltage supply source terminal of conventional one by removing voltage supply source. A very small leakage current is flowing in designing using AVLS technique [14]. Also power dissipation is very less here [15]. Figure 3 shows the of Half Subtractor designed using AVLS.

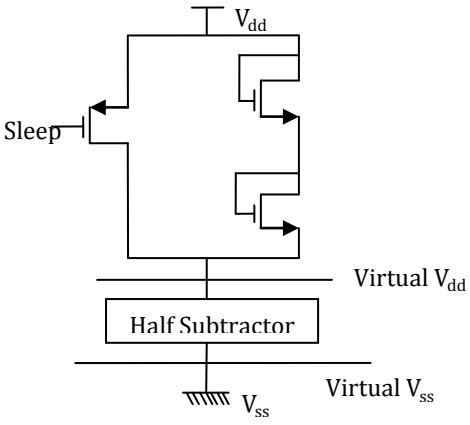

Fig. 4 AVLS Technique of Half Subtractor

Table 3 shows the truth table of Half Subtractor designed using AVLS technique. Fig 3 shows the variation of power Vs supply voltage of Half Subtractor design using AVLS technique. In AVLS Technique the adaptive voltage level control circuit is used either at the upper end of the cell to bring down the supply voltage value. In comparison to the AVLG approach this approach is more successful in lowering the value of the total power usage [16]. This technique also consists of produces a power of 2.25nW.

The truth table below shows the operation of Half Subtractor:

Table (3) Truth Table of Half Subtractor

A	B	Bout	D
0	0	0	0
0	1	X	X
1	0	1	0
1	1	0	0

Layout of Half Subtractor with AVLS Technique

In fig. 5 shows the Layout of Half Subtractor with Adaptive Voltage Level at Supply (AVLS) Technique in which used an extra circuitry for controlling the leakage current. The AVLS is connected to ground source.

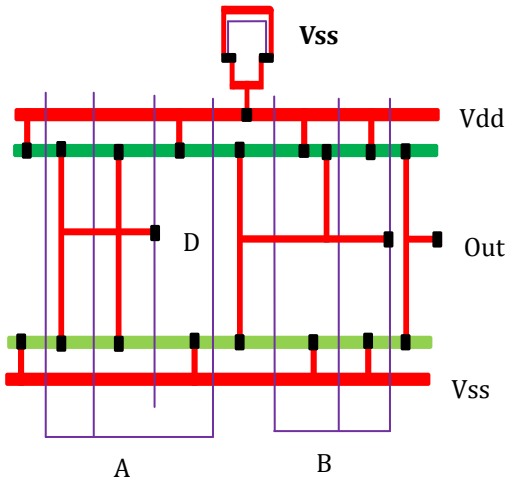

Fig. 5 Layout of Half Subtractor with AVLS Technique

4. SIMULATION RESULTS

The circuit simulated in cadence for 45nm technology, from the result table, we are getting effective and average reduction result in delay, leakage power and Leakage Current with AVL technique compare to AVLS and AVLG technique.

4.1 Leakage Power

In Half Subtractor either the transistors are in off mode or in ON mode due to the early switching of opposite level leakage is introduced. The power consumption in Half Subtractor consume a power off 1.66nW, with AVLG and with AVLS technique power consumes is 2.16nW then, we finally getting the average result of Half Subtractor with AVL(AVLG & AVLS) technique 0.45pW. This shows more power reduction in comparison to AVLG & AVLS at 45nm technology, so from this we analyses a power reduction of 24% using AVL technique [18]. It can also be observed through varied supply voltage as shown in comparison table below;

$$P_{leakage} = I_{leakage} \times V_{dd} \quad (5)$$

Where, $I_{leakage}$ = leakage current and V_{dd} = power supply.

The leakage power is calculated by this formula and AVL technique with supply voltage V_{dd} = 0.7V

Table (4) Shown the Leakage Power

Voltage	Leakage Power of Half Subtractor	Leakage Power with AVLG Tech.	Leakage Power with AVLS Tech.
0.7V	0.68	0.47	0.65
0.8V	1.58	1.24	1.64
0.9V	2.79	2.15	2.92
1.0V	3.45	3.05	4.25

Simulation results have been shown in Fig.6 & it is clear that Leakage power increases with the power supply. Figure also shows that the power dissipation is less at compared to Level-3 at 0.7V to 1.0v input supply.

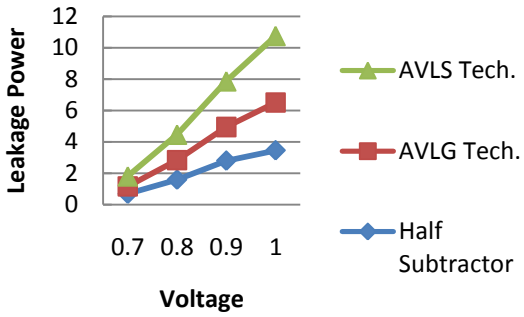

Fig. 6 Shows the Graph of Leakage power analysis

4.2 Leakage Current

Consists varied parts of this. Like the sub threshold leakage current, gate leakage current, reverse biased junction leakage current and gate evoked drain leakage current are the sub-threshold leakage current and also the gate leakage current square measure dominant within the circuit

Table (5) Shown the Leakage Current

Voltage	Leakage Current of Half Subtractor	Leakage Current with AVLG Tech.	Leakage Current with AVLS Tech.
0.7V	57.13	3.05	25.65
0.8V	111.81	13.67	34.15
0.9V	171.61	42.61	73.04
1.0V	232.42	85.04	101.25

Simulation results have been shown in Fig.7 & it is clear that Leakage Current increases with the power supply. Figure also shows that the power dissipation is less at compared to Level-3 at 0.7V to 1.0v input supply.

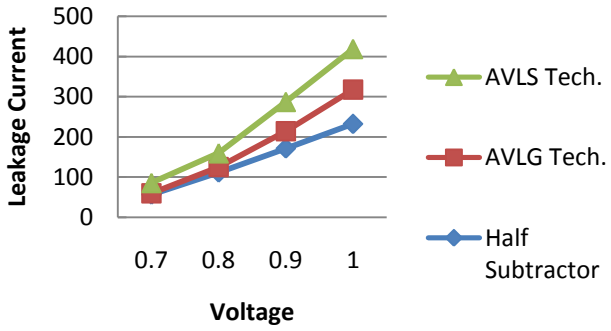

Fig. 7 Shows the Graph of Leakage Current analysis

4.3 Delay

The time difference between the input increasing the reference voltage and output changing the logic state is known as the propagation delay, propagation delay time of Half Subtractor input a larger input will result in a smaller delay time. Delay time of the circuit is measured as the average of response time of gate for positive. The comparative analysis of various circuit delay time is shown below.

Table (6) Shown the Delay

Voltage	Delay of Half Subtractor	Delay with AVLG Tech.	Leakage Power with AVLS Tech.
0.7V	3.85	21.39	21.34
0.8V	4.95	25.24	34.15
0.9V	6.21	42.61	73.04
1.0V	8.02	85.04	101.25

Simulation results have been shown in Fig.8 & it is clear that Delay increases with the power supply. Fig. 8 also shows that the power dissipation is less at compared to Level-3 at 0.7V to 1.0v input supply.

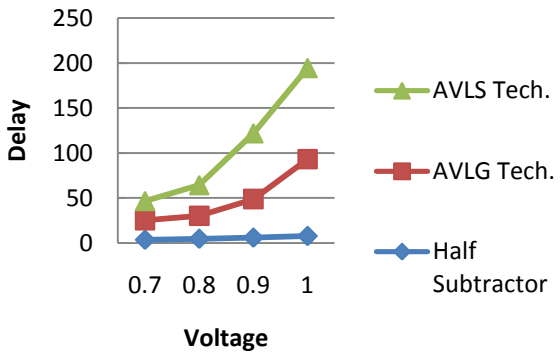

Fig. 8 Shows the Graph of Delay analysis

5. CONCLUSION

The Half Subtractor is an important gate level diagram Inverter, AND gate, OR gate and XOR gate. During this experiment, completely different techniques were gained and applied in an exceedingly basic half. So, we will be able to design implement and analyze, with success, the characteristics of a Half Subtractor circuit. The completion of most of the tasks was satisfactory since the theoretical expectations matched our experimental results. The performance of the Half Subtractor was assessed in terms of area, speed; Leakage Current and power consumption in used the AVLG and AVLS technique. Also quality of the output signals was ensured by comparing the timing measurements of every circuit by means of propagation delays. The PMOS connect V_{dd} supply voltage at 0.7v and NMOS connect V_{ss} supply ground. The circuit has been used for the design of low power and high speed. On designing AVL technique based Half Subtractor using 45 nm technologies; we obtain a very low power consumption circuit, less propagation delay, leakage current and also with lesser number.

6. ACKNOWLEDGEMENT

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