High EMI Resistivity CMOS Operational Amplifier

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ABSTRACT
In this paper a high resistant EMI interference CMOS operational amplifier has been designed and simulated. It is designed by implementing easy modification of the differential pair with active current load. The power amplifier seems to be leading the output voltage power with respect to the input supply given, the two stage power amplifier was designed in this current technology and results are noted below. CMOS power amplifier is a type of power amplifier designed by using CMOS transistors connected together and get the output gain of amplifier .The desired input stage can be produce using standard CMOS technologies, and it also does not requires extra levels of masking process, such as triple well, nor external components are required. Analysis and results have been provided for very large interferences, which arise from the input pin and result produced are noted precisely.

Index Terms:
-CMOS, Resistivity to electromagnetic interferences (EMIs), ICs, operational amplifier (Op Amp).

1. INTRODUCTION
Due to the increasing adaptation of microelectronic and electronic circuitry applications, electromagnetic interferences (EMI's) the resistivity has become an important constraint for IC designers. The effects of EMI, indeed, may involve a wide class of circuits. Furthermore, the level of electromagnetic environmental pollution has been increasing during the past years because of the wider and wider diffusion of wireless LANs (WLAN's). The amplitude of EMI, which is collected by wires and printed circuit board (PCB's) traces, has consequently increased and may be quite larger than the amplitude of nominal signals, leading to failures on the ICs exposed to EMI [1-3]. As a consequence, IC designers have to consider EMI during design phase: a posterior layout adjustments, filters, change in the operating frequency, shielding are, indeed, seldom viable and often complex and expensive. Therefore, in recent years, EMIs were carefully investigated [3], both theoretically and experimentally, in an objective to find possible preventing methods; in particular in high-performance ICs implementing analog-digital transfer characteristics that comprises distinctly various operational amplifiers (Op Amps). The most sensitive circuits to EMI are, indeed, the analog ones and, among them, the Op Amps [3]. In literature, it has been demonstrated that a successful approach to reduce the EMI susceptibility of the Op Amp is the adoption of symmetrical topologies [4-5]; unfortunately, the high EMI resistance architectures presented in previous works are unsuitable for the low voltage supply of the current ICs, due to the cascode connections. Therefore, recently, other solutions were proposed to intrinsically improve the resistivity of the amplifiers. For example, in [6], a double differential pair along with an RC high-pass filter has been designed to have a good EMI resistivity, while in [8], a simple RC filter on the Op Amp input stage has been proposed. In what follows, a CMOS amplifier is presented, suitable for low voltage applications, which exhibits a high resistivity to very large EMI's arising from the input pin at low to medium and out-of-band frequencies. The proposed Op Amp comprises of most simple and efficient adjustment of the Miller Op Amp input stage, still preserving high gain and large gain-bandwidth (GBW) product. The proposed adjustment can be formulated by standard CMOS technology, and it neither requires extra levels of masking, such as triple well, nor external components. Furthermore, it can be easily adapted on other Op-Amp topologies, improving their resistivity to EMI.

2. DESIGN STAGES
In order to easily investigate the EMI effects on a generic amplifier, the interfering signals are represented by a sinusoidal waveform generated with zero dc mean value and superimposed on the pins connected to long wires (long wires, indeed, act as antennas for EMI). This assumption represents a worst-case condition, because the interfering signal often decays with time. Furthermore, the amplifier is in the voltage-follower configuration, as reported in [3] and [4], as it is a worst-case condition [3] as well. The undesirable effects concerning about interferences is the shift of the output dc mean value (offset) that may asymptotically force the amplifier to saturation, as depicted in Fig. 1; this unexpected behaviour of the Op-Amp transient response is mainly due to the parasitic capacitances and to the asymmetry of signal paths during the positive and the negative period of the sinusoidal waveform. Concerning the Electromagnetic Interface superimposition to the power pins, filtering can prevent the dangerous dc offset to be formed, while the interfering signals conveyed on the input pins of the Op-Amp are rather difficult to prevent. This is due to the fact that the adoption of external filters may modify the original input signals, often very weak so it should be neglected.
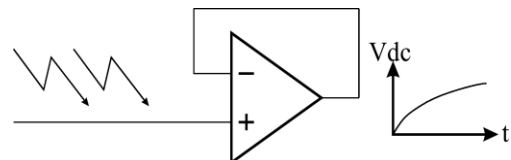

Figure 1 Electromagnetic Interference Effect on Input.

Recently, some solutions have been proposed to intrinsically improve the resistivity of the amplifiers to EMI signals arising from the input pins. For example, in [6], the design of an input stage is reported, based on a double cross-connected differential pair along with a simple high-pass filter. The cross-connected differential pair becomes active only in the pass band of the RC high-pass filter. However, as demonstrated later, this approach may modify the response of the amplifier, critically reducing the GBW product. Another solution has been proposed in [7], based on a double differential pair: in this architecture, the nominal differential pair is bootstrapped using bulk biasing. In the design example shown in [7], the bootstrapped differential pair exhibits an EMI resistivity that is two orders of magnitude larger than the classic differential pair. Nevertheless, following this approach, only a p-type differential input stage can be fabricated in a standard CMOS technology: the n-type stage requires, indeed, a triple-well technology due to the bulk biasing. More recently, in [8], a comparison between the architecture proposed in [6] and a simple differential pair with an RC low-pass filter has been illustrated. To have a fair comparison, the cut off frequency of both the high- and the low-pass filter has been chosen to be 800 kHz, but another value can be used, provided that the filter cut

off frequency is below the minimum frequency of the interfering signals: the RC filter, indeed, must be effective at the frequencies of interferences. All the solutions, briefly described above, except the one proposed in [7], which does not require a standard CMOS technology, are now verified and compared, using a standard Miller Op-Amp. More precisely, the standard Miller Op-Amp has been designed, choosing the optimal aspect ratio of the transistors, and simulated. Then, it has been modified following the approach given in [6] and [8], and the results of the comparison are now discussed. The Miller amplifier has been designed in the standard Austria Micro Systems (AMS) 0.35 μm CMOS process, which has a 1.8-V voltage supply and exhibits the following main characteristics: the gain is 70 dB, the GBW product is 60 MHz, and the phase margin is 80◦. The size of the transistors is chosen to fit the required performances and to accomplish the issues of the analog layout; therefore, there are no minimum length devices and large W/L aspect ratios were preferred for the transistors to be matched with each other. The frequency compensation, which is necessary for a two-stage Op-Amp, is performed by means of a simple RC filter, with values of 5 kΩ and 2 pF, respectively, while the capacitive load is 10 pF. The simulations have been performed on the equivalent circuit extracted from the layout view using the corner and Monte Carlo models. At this point, preserving the same aspect ratios and design of the original Miller amplifier (i.e., the same transistor size, the same frequency compensation, and the same capacitive load), the differential input stage has been modified, following the approach given in [6] and added RC high-pass filter with 800 kHz cut off frequency. The values of the resistor and the capacitor were chosen to be 20 kΩ and 10 pF, respectively. As discussed later in Section IV, the modified topology exhibits a good resistivity to EMIs, but the gain is now slightly reduced (about 63 dB) and, more importantly, the GBW fell down to 6 MHz, with stability problems, resulted in project to be considerably reviewed in order to fit the required performances, due to the cross-couple differential pair and due to the RC high-pass filter, which affect the signal path. The next step is to verify the solution proposed in [8], which is based on a simple low-pass filter with 800 kHz cut off frequency (R = 20 kΩ, C= 10 pF), connected straight to the differential pair. It is worth adding that the design of the original Miller amplifier has been preserved, as for the solution proposed in [6]. In this case, as expected, the gain is still 70 dB, while the input filter significantly deteriorates the GBW, which is now about 6.7 MHz, and the PM, which are only a few degrees. On the other hand, as examined later, the circuit in [8] exhibits a high resistivity to interferences
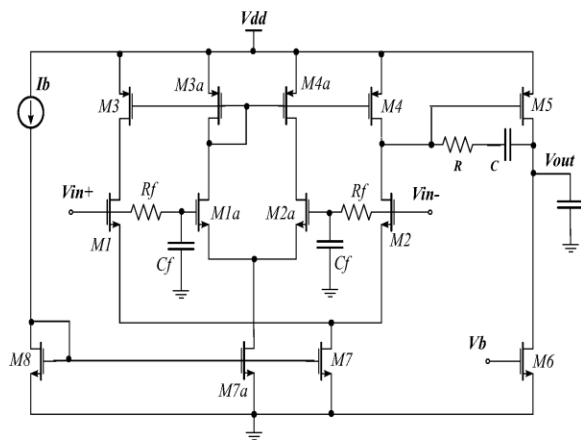
3. PROPOSED OPERATIONAL AMPLIFIER

In two-stage Op-Amps, the input stage is the most susceptible to Electromagnetic interference or EMI, as described earlier also. As the parameters are compared at the input interference, the interferences arise, indeed, from the input pins; they proceed through the current mirror, which acts as an active load, and they propagate to the second stage, where the offset voltage makes the EMI effects more evident it became quite appreciable. Therefore, if this process mechanism can be interrupted somewhere, the EMI resistivity can be improved. As from previous discussion, a straight modification of the input differential pair can significantly increase the resistivity of the overall Op-Amp, but it can considerably modify the frequency response of the amplifier, i.e., the GBW product and the phase margin, forcing to a posterior design review. On the other hand, another way to interrupt the EMI propagation is to create a photo image circuit, based on a supplementary differential pair i.e., is much affected by the interferences due to an RC low-pass filter, and which is connected to an auxiliary current mirror. This is the basic idea of the proposed Op-Amp is shown in Fig. 2. The effective amplifier input stage consists of transistors named M1, M2, M3, M4, M7: more precisely, M1 and M2 are the input differential pair, while M3 and M4 are the active loads, and M7 is the current generator. As in the classical Miller Op-Amp, the biasing circuit is simply represented by means of the transistor M8 and the ideal current generator by Ib, for the sake of clarity. The auxiliary input stage is based on the transistors M1a, M2a, M3a, M4a, and M7a. M1a and M2a act as a replica differential pair, which is quite resistant to the interferences due to the RC low-pass filter; its bias current is fixed by M7a, which is less affected by EMI, as well. M3a and M4a act as the current mirror. In the overall amplifier, the same aspect ratios and design of the original Miller amplifier (i.e., the same transistor size, the same frequency compensation, and the same capacitive load) were preserved, leading to a very easy project .Moreover, to have a fair comparison with the state-of-the-art solutions, the RC low-pass filter has the same 800 kHz cut-off frequency and the same R_f and C_f values. Fig.3. Effect of 900 mV_{pp} EMI injected on the input pin. Due to the supplementary stage of input, the overall amplifier exhibits a better resistivity to EMIs, while the frequency response and phase margin result just slightly modified. The gain of the amplifier still results in 70 dB, while the GBW product is 40MHz and the phase margin is 70◦. Thus, the proposed Op-Amp can be easily derived from the classical Miller amplifier and it does not require a design review. However it may be compared with the other input parameters to obtain precision in the current research architecture.
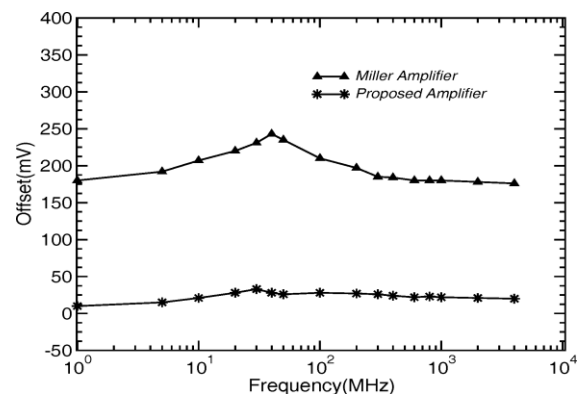

Figure 2 Proposed Op-Amp.

Figure 3

Figure 4 lectromagnetic produced effect on input   Pins at 900 mVpp

4. RESITIVITY TO ELECTRO-MAGNETIC INTERFERENC

In order to verify the EMI resistivity, the interfering signals have been represented by a sinusoidal waveform generated with zero dc mean value and superimposed to the input pin, while the amplifiers were in the voltage-follower configuration, as shown in Fig. 1. The closed-loop configuration is, indeed, more widely used than the open loop one, and it represents a worst-case condition, as well, because the input differential pair is exposed to a large signal. The EMI amplitude was first assumed to be 900 mVpp; a very large value compared to the 1.8 V_{dd}, the frequency range was from 1 MHz to 4 GHz, so in order to account for the spectrum of the possible interfering signals including the cellular phone bands. It is worth adding that including frequency below the GBW product of the amplifier means that the EMI susceptibility is quantified not only out-of-band but also in-band. The susceptibility may appear at low to medium frequency as well; this is due to the high amplitude of the interferences, which forces a nonlinear behaviour of the amplifier. Many cycles of simulations were performed on the circuits extracted from the layout using typical, slow and fast transistor models. Moreover, the mismatch simulations were done, as well. In many analog applications, indeed, a special care must be devoted to the matching issue and this is especially true in this case, where the resistivity to interferences is improved due to a replica circuit. For example, a good solution is to lay out the input stage devices, which must be matched with each other, in a common-centroid arrangement. Furthermore, a large use of dummy strips in matched devices was done; symmetrical metal paths for the signals were designed, and substrate contacts (guard rings) were added for suppression of substrate noise and for the reliability. Nevertheless, Monte Carlo mismatch simulations were performed, considering a not optimal matching, using typical, slow and fast models (as stated above), and the results in the worst-case conditions are shown in Fig. 3. In this figure, the offset of the proposed amplifier is compared to the one of the classical Miller topology: the proposed amplifier shows an EMI susceptibility reduced by more than one order of magnitude. The maximum offset caused by EMI is, indeed, of a few tens of millivolts, while the offset of the Miller amplifier (in the same operating conditions) ranges from 150 mV up to more than 200 mV. Simulations were also performed with interfering signals of 1.8 V_{pp} and the simulation results are shown in Fig. 4.
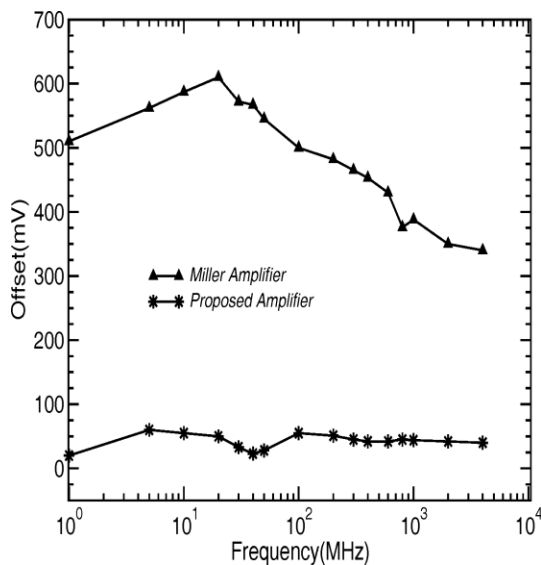

Figure 5 Electromagnetic produced effect on input Pins at 1.8 Vpp.

The proposed amplifier exhibits a strong resistivity to very large interferences, as well. The maximum offset caused by EMI is, indeed, about 50 mV, while the offset of the Miller amplifier (in the same operating conditions) ranges from 350 mV up to more than 600 mV. Furthermore, in some applications, the interferences, which can affect the Op-Amp input pin, may be quite smaller and, therefore, the offset of the output voltage is shown in Fig. 5
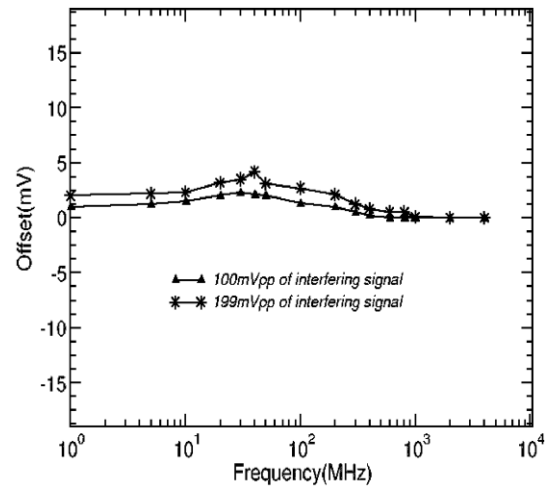

Figure 6 Electromagnetic Produced Effect on Input Pin at 100 mVpp.

The above figure clearly states the electromagnetic effect produced on input pin terminal at $100 \mathrm{m} V_{PP}$. In the case of a 100 mVpp EMI signal. As expected, the proposed Op-Amp exhibits a good Electromagnetic interference resistivity is observed and the output-voltage offset is also negligible. This is very obligatory parameter as the overall working is concerned.
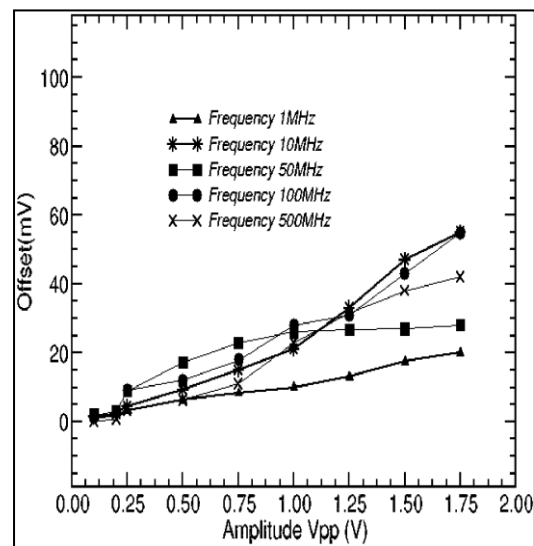

Figure 7 Electromagnetic produced effect on input   Pins at 100 mVpp to 1.8 Vpp.

In Fig. 6, the offset voltage is plotted, sweeping the interferences amplitude from 100 mVpp to 1.8 Vpp at fixed frequencies, in order to completely characterize the EMI behaviour of the proposed solution. As highlighted by Fig. 6, the output-voltage offset increases with the amplitude of the EMI signal, as expected, while the susceptibility versus the interference frequencies is not obvious. The more critical frequencies of the interferences are, indeed, the medium one (10–500MHz), while

the susceptibility is generally lower at very high frequencies (above 1 GHz).Moreover, if the package and the PCB are considered as a part of the IC, they act as a low-pass filter with a cut-off frequency in the range of gigahertz.

Figure 8   Comparison B/W Miller Opamp And Proposed Opamp

	Gain	P M	GBW	Offset at 900mV$_{pp}$	Offset at 1.8mV$_{pp}$
Miller OpAmp	75dB	75^0	70MHz	200mV at 35MHz	550mV at 18MHz
Results of (4)	65dB	0^0	7MHz	18mV at 35MHz	40mV at 18 MHz
Results of (5)	70dB	7^0	7.5MHz	14mV at 30 MHz	35mV at 15 MHz
Proposed OpAmp	70dB	68^0	50MHz	25mV at 15MHz	60mV at 5 MHz

5. CONCLUSION

For the sake of clarity, Table I highlights the main characteristics of the proposed Op-Amp, compared to the classical Miller topology and the state-of-the-art solutions. It is worth noting that the solutions proposed in [6] and [8] exhibit a very good resistivity to interferences, but they require a design review to increase the GBW and the phase margin, which are critically reduced due to the RC filter that is connected straight to the input differential pair. The proposed OpAmp shows a strong resistivity as well, and it can be easily designed starting from the Miller architecture. Moreover, the basic idea of the replica input stage can be used in other two-stage topologies, improving their resistivity to EMI, and it is well suited for low-voltage applications.

6. REFERENCES

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