Minimizing Power Consumption in CMOS Full Subtractor using SVL Technique

Anand Singh Narwariya
M. Tech. (VLSI design), EC Department
I.T.M. Gwalior, (M.P.)

Shyam Akashe
Professor, EC Department
ITM University, Gwalior, (M.P.)

ABSTRACT
Full Subtractor using Self Controllable Voltage Level (SVL) Technique is designed in this paper. The circuit can supply an increased dc voltage to an active-load circuit required or can decrease the dc voltage supplied to a load circuit under standby mode is developed. Full Subtractor is a consumed low power and low Leakage as compare to conventional design with SVL technique. We may reduce the value of total power dissipation by applying the U-SVL (upper Self Controllable voltage level) technology in which the supply potential is increased and L-SVL (Lower Self Controllable voltage level) technology in which the ground potential is raised. The analysis paper represents how to control power using SVL techniques. The SVL technique based Full Subtractor compared to conventional design that based on power consumption, propagation delay speed and layout area is more preferred. Low-power techniques projected to reduce power in nanoscale CMOS-Very Large Scale Integration (VLSI) systems, Using SVL technique. The result shows that there is significant reduction in Power assimilation of Full Subtractor in reference mode. This design is much useful in designing the system that low power consumed. The circuit is designed using Cadence Tools in 45nm Technology.

Keywords: SVL technique, Full Subtractor, CMOS Circuit, Low Power and High Speed

1. INTRODUCTION
The Full Subtractor is an assembled circuitry representing the small unit for subtraction in digital systems. Most of the gates used in digital design are not reversible for relevance NAND, OR and E-XOR gates [1]. Hence the reversible logic synthesis of Full Subtractor is very critical for designing of small size portable devices [2]. There are numerous potential logic designs that may give good performance as compared to the basic CMOS logic design [3]. The performance estimation of Full Subtractor is predicated on the basis of area, delay and power consumption [4], [12]. To perform the designing, full custom implementation and simulation of Subtractor at the CMOS circuit level suggests CMOS 45nm technology [5]. It is designed to check if the circuit may perform with all the possible combinations of the input beside the logic performance [6] and to evaluate the standard of the output signals in terms of voltage levels [7]. The access performance of the circuit is in measured terms of speed, area, delay and power consumption [8], [15]. The CMOS circuit Full Subtractor designs using numerous totally different logic designs are conferred and unified into the integrated design methodology. The Conventional Full Subtractor CMOS circuit diagram is shown in fig. 1 and its truth table in table 1. The numbers of logic gates needed to make this Subtractor are added so as to increase the number of CMOS circuits. Therefore the delay and area will be large. The necessity for optimising Full Subtractor using cadence is to reduce the area, delay and power consumption [10], [11]. The CMOS gpdk 45nm technology incorporates the cadence schematic Editor and Analog Environment software used to produce a schematic diagram and implementation of our simulation. However, it contains the Cadence Virtuoso Editor that allows us to design the layout of the Full Subtractor, as well as to assess the performance the of many performance parameters for the circuit. In addition, transient analysis is performed [17]. The proposed specifications supply a good choice of variable between two types of implementations, even with an analogy problem. We selected the design of a Subtractor in order to minimize the area as much as possible. It is not only used for arithmetic calculation in many device processors but also used in other part of processor for calculating address. Stack pointer use subtraction operation in push-pop logical operation for storage of address. The simplest combinational circuit which performs the arithmetic subtraction of 2- binary digits is called Full- Subtractor [18] .This is the necessary building block for designing a VLSI system. Power dissipation in any Full Subtractor circuit depends on both static and dynamic power dissipation. The static power delivered is the multiple of supply voltage and leakage current. The leakage current is described by the equation.

$$I_o = I_s\,(e^{qV/kT} - 1) \quad (1)$$

Where I_s = reverse saturation current, V= diode voltage, q= electronic charge, k= Boltzmann's constant, T= temperature.

The static power delivered is the multiple of supply voltage and leakage current. The total static power dissipation P_s is given by:

$$P_s = \sum_1^n I_{leakage} \times V_{dd} \quad (2)$$

Where n = no of devices

2. FULL SUBTRACTOR
A full Subtractor is an assembled circuit that performs a subtraction between 2- bits taking into account that a 1 may have been borrowed by a lower important stage. This circuit has 3-inputs and 2-outputs. In which 3-inputs A, B and C are applied at the different gates and corresponding output are gated. These are the three inputs which consist of three 1- bit numbers A, B and C. We have a present the gate level implementation of each Full Subtractor. Those output are the D (difference) and B (borrow) is denoted. The gate are used to construct the Subtractor have their own specifications and aren't altered during this work, the gate level diagram of full Subtractor.

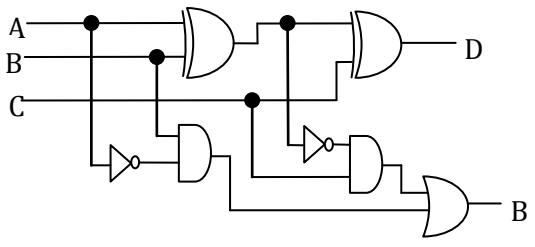

Figure 1 Gate Level Design of Full Subtractor

In the process of subtracting 2-bit number the subtrahend are taken in to consideration. There will be a '1' borrowed from the

before adjacent lower number bit. As a result, there are 3 bits to be tackled at the input end of a Full Subtractor, particularly a borrow bit designated as C and the two bits to be subtracted. There are 2- output, particularly the Difference D and the Borrow Y. Borrow output bit tells whether or not the number bit has to borrow a '1' from the next possible higher number bit.

Truth Table describing Full Subtractor nature

Table 1- Truth Table of Conventional Full Subtractor

A	B	C	Bout	Diff
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

The simple Boolean functions of output can be acquired from the truth table. The logic equations are:-

$$\mathrm{D(diffrence)} = \mathrm{A} \oplus \mathrm{B} \oplus \mathrm{C} \quad (3)$$

$$\mathrm{B(borrow)} = \mathrm{A'B} + \mathrm{A'C} + \mathrm{BC} \quad (4)$$

3. FULL SUBTRACTOR USING SELF CONTROLLABLE VOLTAGE LEVEL (SVL)

The modern VLSI technology requirement for devices operating at Low-Power and providing high performance design requirements of modern technology can be acquired by taking use SVL technology. A Self Controlled voltage level technique may be used to control circuit, either at the upper end of the cell to reduce the value of supply voltage called U-SVL scheme or to lift the potential of the ground node at the lower end of the cell, called L-SVL scheme. By this technique reduction of power dissipation is occurred. The power dissipation is reduced less than conventional design. The complete effect of these techniques on the power consumption is described as follows.

3.1 Design Full Subtractor using U-SVL

In U-SVL technique, a combination of one PMOS & two NMOS are connected in parallel. So that an input clock pulse is applied at the PMOS of circuit of U-SVL and rest of all NMOS are connected to drain terminal. Full Subtractor using U-SVL scheme is depicted in Figure below. Under this scheme, full supply voltage of V_{dd} is applied to the semiconductor device. The U-SVL schematic is intended on a broad channel pull up p-MOSFET & pull down n-MOSFET.

The circuit diagram of full Subtractor designed using U-SVL technique. This approach is more valuable for reducing the power consumption also for the leakage current. For very low Power consumption, U-SVL technique is most responsible. Subtractor designed at micron CMOS technology, produces the better results. But now a day of nanotechnology at V_{dd} = 0.7 V, power consumption is 1.622µw.

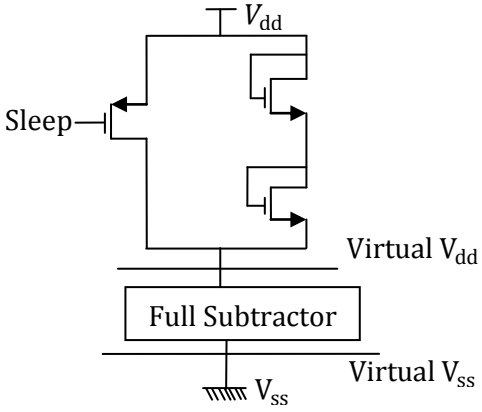

Figure 2 U-SVL Scheme of full Subtractor

3.2 Design Full Subtractor using L-SVL

In L-SVL technique a combination of one NMOS & two PMOS are connected in parallel. So that an input clock pulse is applied at the NMOS of circuit of L-SVL and rest of all PMOS are connected to ground. This ground terminal is connected to the L-SVL circuit. Full Subtractor using L-SVL scheme is shown in Figure 3. The switch brings 0Volt at the ground node & raises the ground level (virtual ground). The L-SVL circuits initiates wide channels pull down n-MOSFET and pull up p-MOSFET.

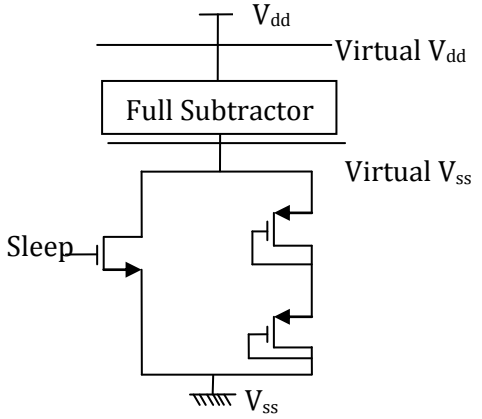

Figure 3 L-SVL Scheme of Full Subtractor

Depending upon the clock and inputs, variation in output is varied. Figure 3 shows the variation of power V_s supply voltage of Full Subtractor design using L-SVL scheme. Where the power consumption is measured at the various supply voltage at V_{dd} = 0.7 V, power consumption is 1.24µw.

3.3 Full Subtractor with SVL technique

The SVL design comprises of an upper U-SVL circuit and a lower L-SVL circuit, the schematics shown in Figure 4 are applied to the Full Subtractor. The U-SVL is design on wide channel pull up p-MOSFET and pull down n-MOSFET, so U-SVL and L-SVL design can provide higher supply voltage V_d = V_{dd} and a reduced ground-level voltage V_s (V_{ss} = 0).

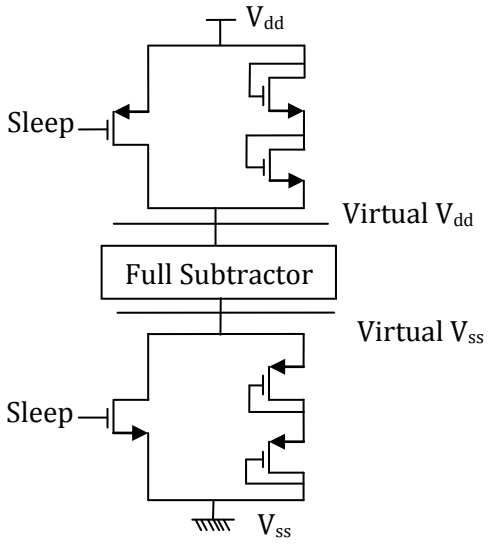

Figure 4 SVL Technique of Full Subtractor

The circuit design of U-SVL and L-SVL correspondingly generate a lower supply voltage V_{dd} = V_{dd} vn < V_{dd} and a comparatively higher ground-level voltage V_s = V_p > 0V, where V_n and V_p are the total voltage drops of all U-SVL and all L-SVL, correspondingly.

Layout Diagram Full Subtractor with SVL Technique

The Layout of Full Subtractor with self controllable voltage level (SVL) Technique is shown in figure 5, in which an extra circuitry for controlling the leakage current is used. SVL is classified into two blocks- namely upper SVL (U-SVL) and lower SVL (L-SVL).U-SVL is connected to V_{dd} and L-SVL is connected to ground. In both upper and lower SVL comprises of 1- NMOS and 1- PMOS and gates are connected and applied a pre-charge voltage of 1V.

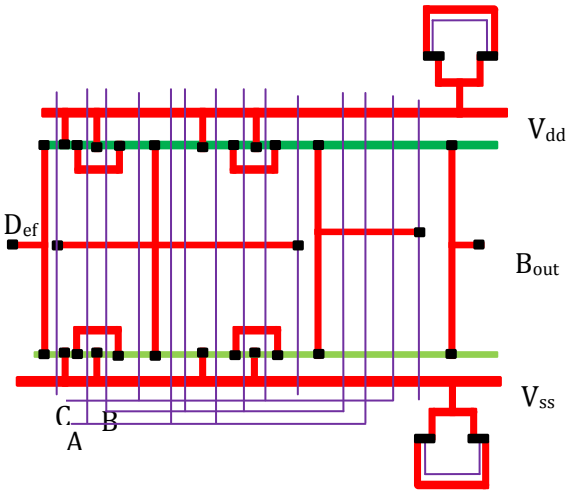

Figure 5 Layout Diagram of Full Subtractor with SVL Technique

4. SIMULATION RESULTS

The circuit work simulated in cadence for 45nm technology, from the result table, we are getting effective and average reduction result in delay, leakage power and Leakage Current with SVL technique compare to U-SVL and L-SVL technique.

4.1 Leakage Power

In Full Subtractor either the transistors are in off mode or in ON mode due to the early switching of opposite level leakage. The power consumption in Full Subtractor consume a power off 1.66nW, with U-SVL and with L-SVL technique power consumes is 2.16nW then, we finally getting the average result of Full Subtractor with SVL (both U-SVL & L-SVL) technique 0.45pW so we achieved a power reduction, this shows more power reduction in comparison to U-SVL & L-SVL at 45nm technology, so from this we analyses a power reduction of 24% using SVL technique with Full Subtractor. It can also be observed through varied supply voltage as shown in comparison table below;

$$P_{leakage} = I_{leakage} \times V_{dd} \quad (5)$$

Where, $P_{leakage}$ = leakage current = V_{dd} power supply.

The leakage power is calculated by this formula and we calculate the effective power in Full Subtractor with SVL technique with supply voltage V_{dd} = 0.7V

Table 2 Shown the Leakage Power

Voltage	Leakage Power of Full Subtractor	Leakage Power with U–SVL Tech.	Leakage Power with L–SVL Tech.	Leakage Power with SVL Tech.
0.6V	0.59	0.57	0.59	0.55
0.7V	2.18	2.13	1.81	1.93
0.8V	5.55	5.72	4.46	4.59
0.9V	10.40	10.22	8.55	8.60
1.0V	17.58	17.48	12.54	12.52

Simulation results have been shown in Figure 6 & it is clear that Leakage power increases with the power supply. Figure also depict that the power dissipation is less as compared to LEVEL-4 at 0.6V to 1.0v input supply.

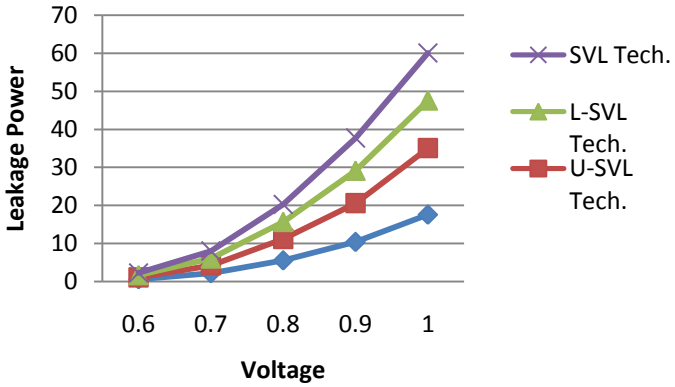

Figure 6 shows the graphs of Leakage power analysis

4.2 Leakage Current

In Full Subtractor either the transistors are in off mode or in ON mode due to the early switching of opposite level leakage. The Leakage Current in Full Subtractor Leakage a Current off 6.21mA, with U-SVL and with L-SVL technique Leakage Current is 4.21mA then, we finally getting the average result of

Full Subtractor with SVL (both U-SVL & L-SVL) technique, this shows more Leakage reduction in comparison to U-SVL & L-SVL at 45nm technology, so from this we analyses a Power reduction of 24% using SVL technique with Full Subtractor. Power dissipation in any Full Subtractor circuit depends on both static and dynamic power dissipation. The static power delivered is the multiple of supply voltage and leakage current. The leakage current is described by the equation.

$$I_o = I_s\,(e^{qV/kT} - 1) \qquad (6)$$

Where, $I_{leakage}$ = leakage current & V_{dd} = power supply.

Table 3 Shown the Leakage Current

Voltage	Leakage Current of Full Subtractor	Leakage Current with U–SVL Tech.	Leakage Current with L–SVL Tech.	Leakage Current with SVL Tech.
0.6V	2.17	1.76	3.59	127.0
0.7V	5.90	2.35	169.10	182.5
0.8V	9.26	8.86	227.6	237.6
0.9V	12.62	51.28	285.8	297.2
1.0V	17.58	106.21	343.5	346.3

Simulation results have been shown in Figure 7 & it is clear that Leakage Current increases with the power supply. Figure 7 also shows that the Leakage Current is less at compared to Level-4 at 0.6V to 1.0v input supply.

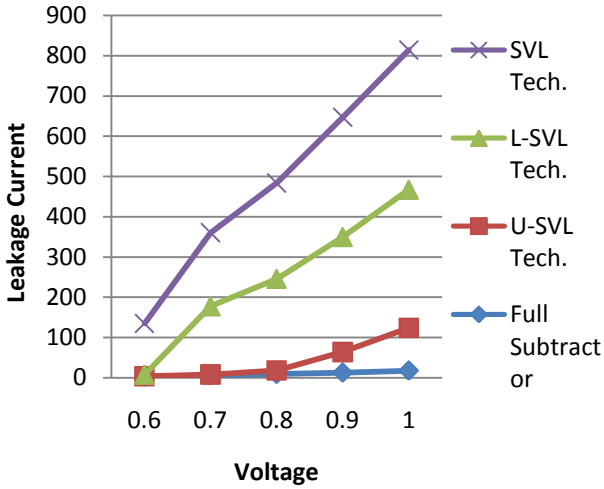

Figure 7 Shows the Graph of Leakage Current Analysis

4.3 Delay

The time difference between the input increasing the reference voltage and output changing the logic state is known as the propagation delay, propagation delay time of Full Subtractor input a larger input will result in a smaller delay time. Delay time of the circuit is measured as the average of response time of gate for positive. The comparative analysis of various circuit delay time is shown below.

Table 4 Shown the Delay Analysis

Voltage	Delay of Full Subtractor	Delay with U–SVL Tech.	Delay with L–SVL Tech.	Leakage Power with SVL Tech. (both U-SVL & L-SVL)
0.6V	4.25	3.21	1.32	3.54
0.7V	9.35	5.36	3.25	6.27
0.8V	15.65	7.23	6.02	10.69
0.9V	21.34	10.25	8.32	18.67
1.0V	*27.02*	*15.64*	*12.06*	*30.45*

Simulation results have been shown in Figure 8 & it is clear that Delay increases with the power supply. Figure 8 also shows that the Delay is less at compared to Level-4 at 0.6V to 1.0v input supply.

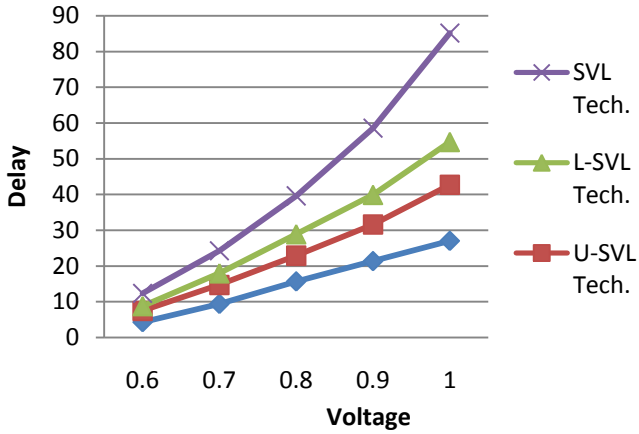

Figure 8 Shows the Graph of Delay Analysis

5. CONCLUSION

The Simulation results clearly explain the reduction in the power consumption by incorporated with SVL technique that is either U-SVL or L-SVL technique. Proposed Full Subtractor is modified by using transistors having less average power consumption with decreases in delay is also decreased by using only PMOS as because delay is more concentrated to PMOS due to less Power, delay and Leakage Current, SVL based Full Subtractor is created by using transistor and have better performance than the U-SVL and L-SVL Full Subtractor as there are fewer transistor counts by which area is reduced and delay is also reduced; the average power consumption of the proposed Full Subtractor is less in comparison to the conventional Full Subtractor, measured result correctly verified the principle of operation and characteristic of the low-power Full Subtractor circuit. The circuit has been used for the design of low power. On designing SVL technique based full-Subtractor using 45 nm technologies, we obtain a very low power consumption circuit, less propagation delay and also with lesser number.

6. ACKNOWLEDGEMENT

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8. AUTHOR'S PROFILE

Anand Singh Narwariya received B.E. Degree in Electronics and Communication from Gwalior Engineering College, Gwalior, (M.P.) in 2011, currently pursuing M.Tech in Institute of Technology & Management Collage, Gwalior (M.P.). His areas of interest in the area of Low Power and High performance VLSI Design.

Shyam Akashe was born in 22nd May 1976. He received his M.Tech from ITM, Gwalior in 2006. He is currently working as Associate Professor in Electronics and Instrumentation Engineering Department of Institute of Technology and Management, Gwalior. Currently, He is pursuing his Ph.D. from Thapar University, Patiala on the topic of Low Power Memory Cell Design. His researches interests are VLSI Design, Low Power and VLSI signal processing, FPGA Design and Communication System.