Design of Low Power 16-Bit Novel Carry Select Adder using 0.18um Technology

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ABSTRACT
In this paper, a Novel 16-bit carry select adder (CSLA) is proposed to perform fast arithmetic operation in many data-processing processors. The proposed design combines the modified 16-bit carry select adder and a carry select adder by sharing the common Boolean Logic term. The area and power of the Novel 16-bit carry select adder significantly reduces when compared with modified 16-bit carry select adder[2].This work evaluates the performance of the proposed design in terms of total number of gates, area, delay and power using Cadence Virtuoso gpdk 180nm technology. In this proposed design the transistor count of a 16-bit carry select adder reduced from 470 to 432 gates which reduce the area by 13.64μm^2. Moreover, the power consumption has reduced from 9.206n watts to 6.648n watts. The delay of the Novel 16-bit carry select adder increased by 29.626*10^{-18}s. The result analysis shows that the Novel 16-bit CSLA is better than modified and regular 16-bit CSLA [1].

Keywords
Carry select adder, Area-efficient, Low power, Hardware sharing, Boolean logic.

1. INTRODUCTION
Design of optimized area and low power large speed data path logic systems are most substantial parameters of research in VLSI System design. Digital computers perform variety of information tasks. Among the functions encountered are the various arithmetic operations. The basic arithmetic operation is addition and is performed by different binary adders. Addition is most fundamental computation process encountered in digital system. In digital adders, the speed of the adder is limited by the time required to propagate a carry through the adder. The sum for each bit position in an adder is generated sequentially only after the previous bit position has been summed and a carry propagated to the next position.

CSLA is one of the fastest adders used to perform fast arithmetic operations. The carry select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry select adder is done with two adders (i.e, two ripple carry adders) in order to perform the calculation twice, one time with the assumption of carry being zero and other assuming one. After the two results are calculated, the correct sum, as well as the correct carry is selected with the multiplexer once the correct carry is known.

Instead of using two ripple carry adders in regular 16-bit CSLA for C_{in}=0 and C_{in}=1, binary to excess-1 converter is used for C_{in}=1 where the number of logic gates are reduced so that area and power consumption are reduced. This modified 16-bit CSLA is compared with the Novel 16-bit CSLA by sharing the common Boolean Logic term where one XOR gate and one inverter gate is used for each sum operation and one AND gate and one inverter gate is used for each carry-out operation. By using this Novel 16-bit CSLA, circuit area and transistor count can be reduced which in turn lowers the power of the adder circuit. The details of Novel 16-bit CSLA logic are discussed in Section 3.

This paper is structured as follows. Section 2 deals with the transistor count and area evaluation of the modified 16-bit CSLA. Section 3 presents the detailed structure and the function of the Novel 16-bit CSLA by sharing the Common Boolean Logic Term. Comparison results are analyzed in section 4. Finally, the work is concluded in section 5.

2. MODIFIED 16-BIT CARRY SELECT ADDER
In this paper the architectures of 16-bit Modified and novel carry select adders are given in terms of Inverter, Nand and Nor Gates. The schematic of modified 16-bit carry select adder (CSLA) is shown in Figure 1, which has five different groups.

The first group consists of two full adders and second group onwards a 2:1 multiplexer is used to select Ripple Carry Adder (RCA) for C_{in}=0 otherwise Binary to Excess-1 Converter (BEC) will be selected for C_{in}=1. If we use n bit RCA then n+1 BEC's are required along with n+1 2:1 multiplexers. The five different groups and their corresponding layouts of are shown in Figure 2.

The group (2) has 2-bit RCA designed by one full adder and one half adders. Using one AND gate, two XOR gates and one inverter, the 3-bit BEC is designed. In this design, three 2:1 multiplexers have been used for selecting RCA part otherwise BEC.
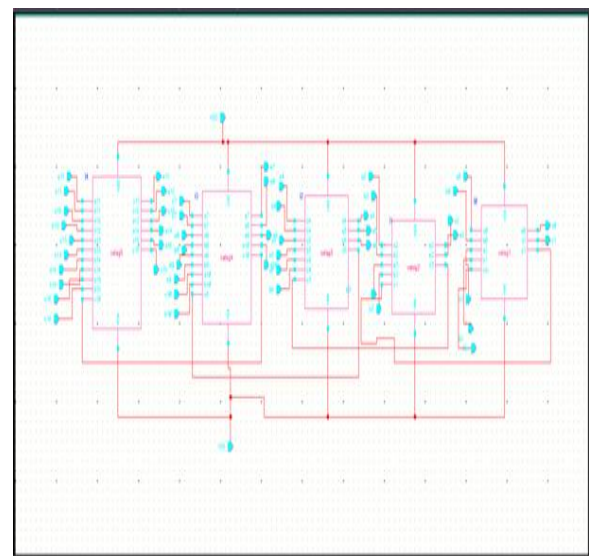

Fig 1: Modified 16-bit CSLA

The transistor count of Group (2) is determined as follows:

TransistorCount=64(1FullAdder(FA)+1HalfAdder(HA)+BEC (XOR+AND+INV)+MUX)

FA=14(1*14)

HA=10(1*10)

AND=2(1*2)

INV=1

XOR=16(2*8)

MUX=21(3*7)

The transistor count of Group (3) is determined as follows:

TransistorCount=95(2FA+1HA+BEC (XOR+AND+INV)+

MUX)

FA=28 (2*14)

HA=10(1*10)

AND=4(2*2)

INV=1

XOR=24(3*8)

MUX=28(4*7)

Similarly, the transistor count of the other groups in the modified 16-bit CSLA are evaluated and listed [1] in Table 1.

Group(1)

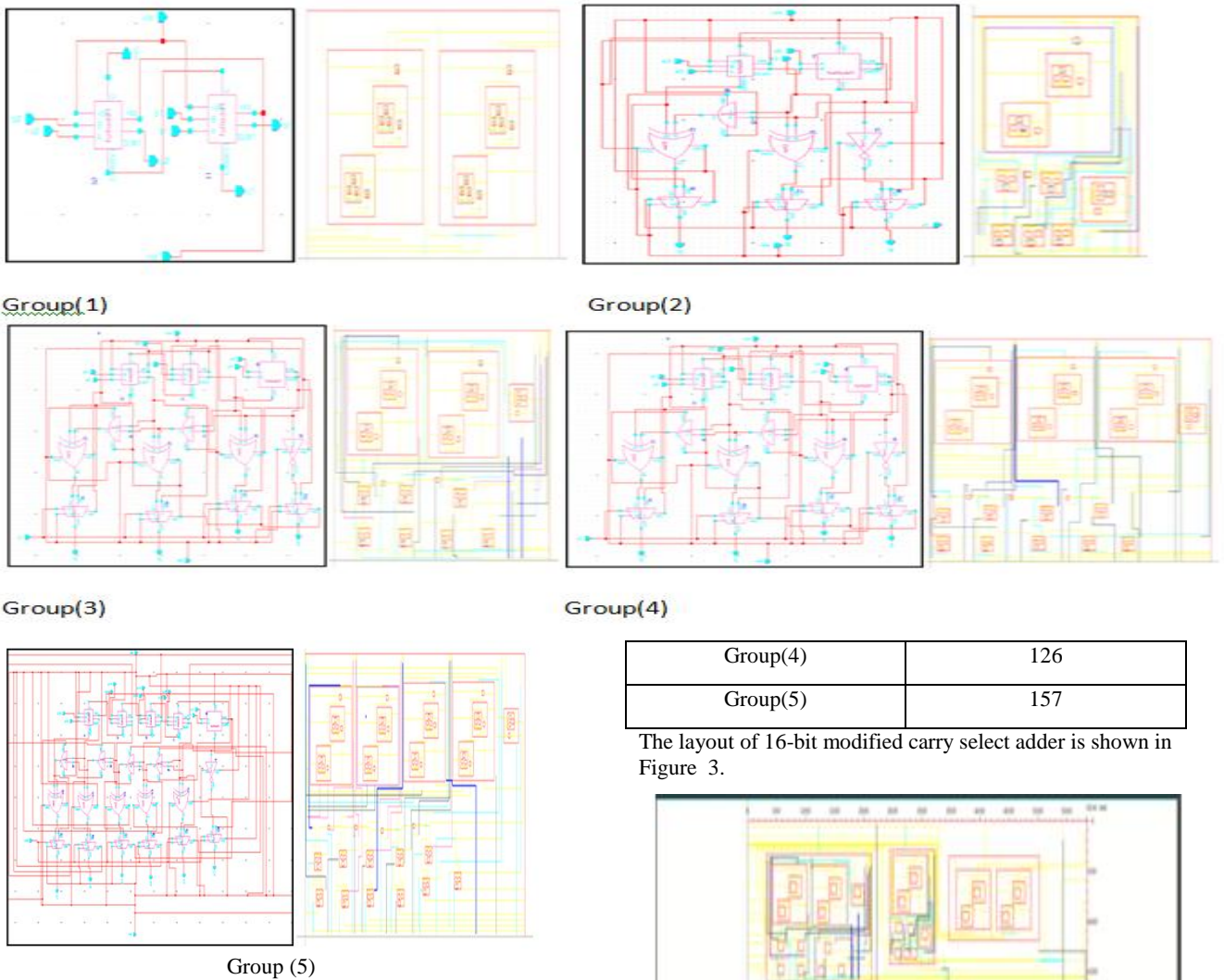
Group(2)

Group(3)

Group(4)

Group (5)

Fig 2: Five Groups of modified 16-bit CSLA

Table 1. Transistor count of 16-bit modified CSLA

Group Number	Transistor Count
Group(1)	28
Group(2)	64
Group(3)	95
Group(4)	126
Group(5)	157

The layout of 16-bit modified carry select adder is shown in Figure 3.

Fig 3: Layout of 16-bit modified carry select adder

The layout is drawn using cadence virtuoso and area is calculated as $21.89\mu m^2$. The power consumed by this adder is found to be 9.206n watts.

3. NOVEL 16-BIT CARRY SELECT ADDER

The proposed 16-bit novel carry select adder has been designed by sharing common Boolean logic term in sum generation to optimize the area and power. Through analyzing the truth table of a single-bit full adder, we can find out that the output of summation signal at carry in (c_{in}=0) is inverse of itself at c_{in}=1.

This is illustrated in the Table 2, S_0 is "0110" at C_{in}=0 and S_0 is "1001" at C_{in}=1.

Table 2. Truth table of 1-bit CSLA using boolean logic

Cin	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

To design this CSLA, we implemented one XOR gate with one INVERTER gate to generate the summation signal. If the carry-in signal is ready, we can select the correct sum output according to the logic state of carry-in signal. To anticipate possible carry input value, we construct one OR gate and one AND gate. Once the carry-in signal is ready, we can select the correct carry-out output according to the logic state of carry-in signal. The proposed single bit CSLA and its layout generating summation and carry signals is shown in Figure 4 and Figure 5 respectively.
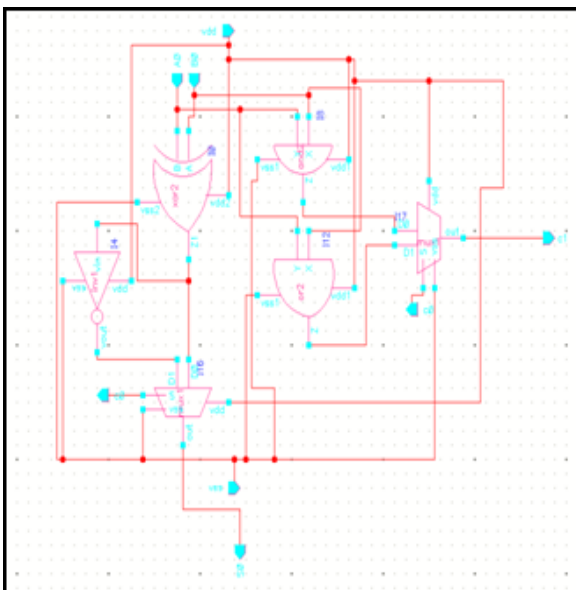

Fig 4: 1- bit CSLA in sum and carry generation

The transistor count evaluation of 1-bit carry select adder by sharing common Boolean logic term is determined in terms of Nand, Nor and Inverter gates is given below:

Transistor Count=27(XOR+OR+AND+INV+2MUX)
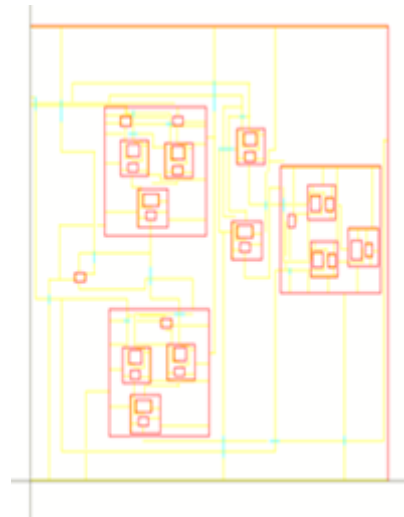
XOR=8

OR=2

AND=2

INV=1

MUX=14(2*7)

Fig 5: Layout of 1-bit Novel carry select adder

Similarly, the transistor count of 16-bit common Boolean logic using carry select adder is 16*27=**432**.The 16-bit proposed carry select adder is constructed from 'sixteen' similar one bit common Boolean logic. Comparing the transistor count of Modified 16-bit CSLA and Novel 16-bit CSLA using shared Boolean logic, it is clear that the successive CSLA saves 38 gates than the Preceding CSLA.

4. COMPARISON RESULTS

The design proposed in this paper has been developed using Cadence Virtuoso gpdk 180nm technology. DRC, LVS and RC extraction is done with Cadence Assura. Here we compared two different CSLA architectures, that is,16-bit modified carry select adder and 16-bit Novel carry select adder using shared common Boolean Logic term. The transistor count of proposed Novel 16-bit carry select adder could be reduced to 432 gates. However, the transistor count in the 16-bit modified CSLA is increased by 38 gates when compared with the proposed design.

The Novel 16-bit CSLA using shared Common Boolean Logic term achieves an outstanding performance in power consumption. Power consumption is reduced in our proposed design because we only need one XOR gate and one INVERTER gate in each summation operation as well as one AND gate and one OR gate in each carry-out operation after logic simplification and sharing partial circuit.

The total power consumed in proposed 16-bit CSLA using shared Common Boolean Logic term is reduced by 2.558n watts and the delay is increased by $29.626*10^{-18}$ s. The comparison of area, power and delay is given in Table 3.

Table 3. Comparison of 16-bit modified & novel csla's

Adder Type	Area(μm^2)	Power(n watts)	Delay(ps)
Modified 16-bit CSLA	21.89	9.206	550
Novel 16-bit CSLA	8.25	6.648	5218

Fig. 6 shows the comparison of area and power of 16-bit Modified and Novel CSLA's. This results show that the CSLA using shared Common Boolean Logic term could achieve a superior performance in aspect of transistor count, area and power.
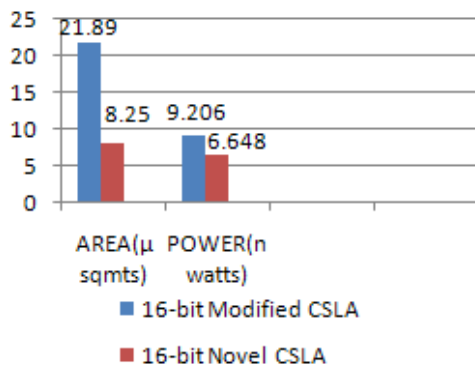

Fig. 6. Comparison of area and power

5. CONCLUSION

An appropriate approach is proposed in this paper to reduce the area and power of 16-bit Novel CSLA. The reduced number of gates of this work gives the great advantage in reduction of area and power consumption. The comparison results show that the area and power of 16-bit Novel CSLA

are significantly reduced by 62% and 27% respectively. The 16-bit Novel CSLA architecture by sharing Common Boolean Logic term is therefore, low area, low power, simple and efficient for VLSI hardware implementation.

6. REFERENCES

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