

# Implementation of High Performance DUC and DDC for Software Defined Radio Applications

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## ABSTRACT

Digital up converters are used at the transmitter side to up convert the baseband signal to intermediate frequency signal. Digital down converters are used at receiver side to down convert intermediate frequency signal to baseband signal. DUC and DDU modules are designed using System generator Xilinx block set and generated verilog code for the same. This paper deals with the implementation of high performance digital up converter and digital down converter for software defined radio application. Simulation is performed using Isim and synthesis is carried out using Xilinx ISE 13.2. Design has implemented on vertex-4 FPGA board. The power consumed in this design is 52.6mWatts and the maximum operating frequency is up to 336.1MHz and total time taken for output is 2.93ns.

## Keywords

DUC - Digital Up Converter, DDC - Digital Down Converter, DDS - Direct Digital synthesizer, CIC – Cascade Integrator Comb, FIR – Finite Impulse response, ADC – Analog to Digital converter, DAC – Digital to Analog Converter, HF – High Frequency, IF – Intermediate Frequency, FPGA – Field Programmable Gate Array.

## 1. INTRODUCTION

SDR technology is defined as radios that provide software control of a variety of modulation techniques, wide-band or narrow-band operation, communications security functions (such as hopping), and waveform requirements of current & evolving standards over a broad frequency range. In short, software modules running on a generic hardware platform of DSPs ( Digital Signal processor ) and general purpose microprocessors can implement radio functions such as modulation/demodulation, signal generation, coding and link-layer protocols. This helps in building reconfigurable software radio systems where dynamic selection of parameters is possible. The communication flow of today is very high. The evolution and growth of telecommunication systems and services run in parallel to Integrated Circuit (IC) design techniques evolution. New fabrication process allows a new functionalities and higher performance. Many applications are operating at high speed and a fixed connection is often preferred. The design of the transmission side of a digital communication modem based on the use of specialized Digital Up Converters (DUC) where baseband processing is performed by a high performance Digital Signal Processor (DSP) and up conversion to Intermediate Frequency (IF) is performed by a Field Programmable Gate Array (FPGA) based design. Similarly in receiver side of digital communication Digital Down Converter (DDC) is used[1][2].

### 1.1 Digital down Convertor

The DDC receives an incoming digital IF signal and modulates the signal into baseband and produces an in-phase

signal and a Quadrature signal as outputs. The design of the DDC can be implemented using FPGAs. The Quadrature modulation is performed by the multiplication of the IF signal with a digital oscillator, the implementation of the digital oscillator is accomplished using a direct digital synthesizer (DDS)[3].

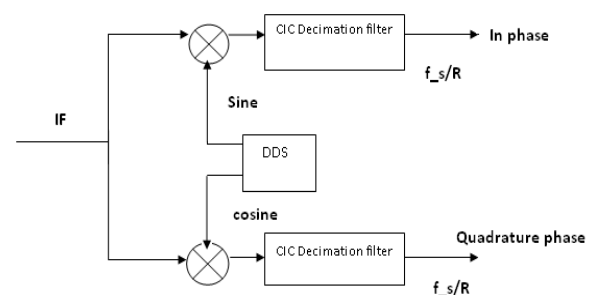


Fig 1: Block diagram of DDC

Direct digital synthesis is a technique by which a sinusoidal signal is created by the generation of digital numbers which controls the input of a sinusoidal look-up table. The digital numbers are generated by a phase accumulator, which receives a binary instruction representing a specific frequency of oscillation. The frequency of this digital oscillator is proportional to the phase increment created in the phase accumulator.

### 1.2 Digital Up Convertor

The DUC receives two baseband signals like in-phase and Quadrature phase signals and modulates these signals into a single real band pass signal. The design of the DUC can be implemented using FPGAs. The Quadrature demodulation is performed by the multiplication of the in-phase and Quadrature signal with the digital local oscillator. The addition of these two resulting signals gives a real band pass signal centered on the digital local oscillator's frequency with an amplitude and phase offset associated with the complex weight assigned to that specific channel. As receiver, a DDS is used to implement the digital local oscillator[4].

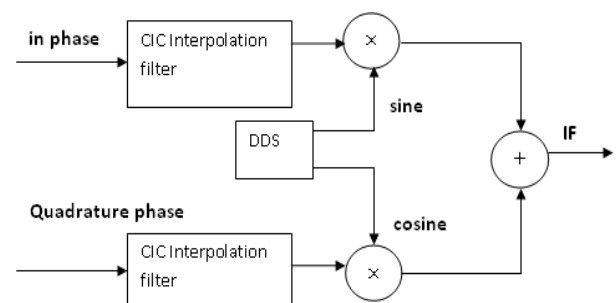


Fig 2: Block diagram of DUC

## 2. FILTER DESIGN

### 2.1 CIC Decimation filter

A multirate filter system is needed in the receiver, such a filter can be implemented using a Cascaded Integrator-Comb (CIC) filter. The CIC is a linear phase FIR filter implemented without the use of multiplication operations operating as a multirate filter to connect two signal processing system components operating at different sampling frequencies.

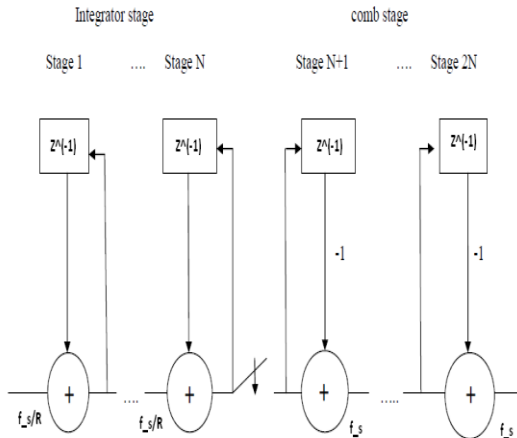


Fig 3: Block diagram of CIC Decimation filter

Its name is derived from its structure, which consists of an integrator section operating at a high sampling rate combined with a comb section operating at a low sampling rate. CIC filters can be used to implement decimation and interpolation filters[5][6]. Above figure 3 shows the architecture of a CIC decimation filter. The CIC filter design parameters are the rate change factor of the multirate filter (R), the number of tap delays in each comb stage (M), and the number of stages in the integrator and comb section of the filter (N).

### 2.2 CIC Interpolation filter

For transmitter, a CIC interpolation filter should be used since it provides excellent results with low computational load. A standard interpolation filter implementation is composed of a zero-insertion phase and a lowpass filter phase. The design of both stages is related to the increase ratio between the input (low sample rate frequency) and the output (high sample rate frequency) of the filter. The CIC interpolation filter implements both phases using a unique design approach. The low sampling comb stage followed by the high sampling integrator stage employs a lowpass linear phase FIR filter[7].

The zero-insertion substage is performed between the two CIC interpolation filter stages. The nulls found at multiples of the frequency  $1/M$  (where M is the differential delay) relative to the low sampling rate are able to suppress the imaging bands found in the spectrum after the multirate filter's zero-insertion substage. As mentioned, the frequency response characteristics of the filter (passband and stopband attenuation, number of nulls, etc.) are determined entirely by the CIC filter parameters (number of tap delays, CIC filter stages, and rate change factor)[8][9].

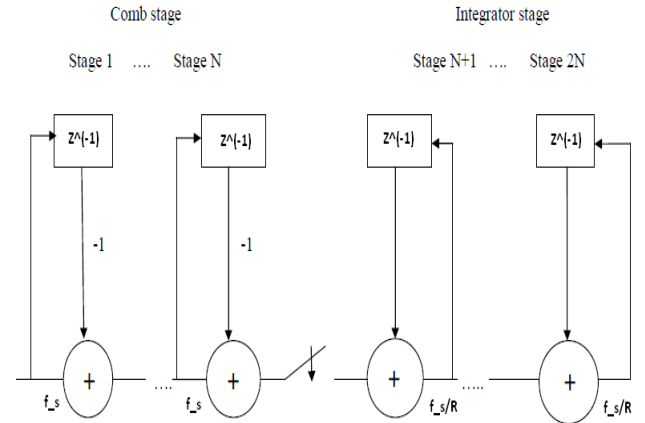


Fig 4: Block diagram of CIC Interpolation filter

## 3. DESIGN AND SIMULATION RESULTS

The model for decimation and interpolation filter is developed based upon specification using MATLAB (simulink) and Xilinx block sets. Hardware is modeled in HDL and simulated using ModelSim PE 10.0c.

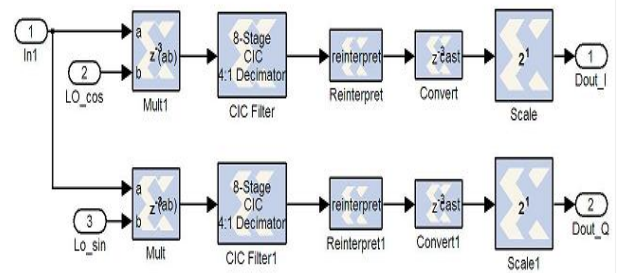


Fig 5: MATlab design of DDC

Synthesis and Functional verification is carried out using Xilinx ISE 13.2. Test environment is developed for verifying DUC and DDC on FPGA. The design is implemented on Virtex 4 FPGA kit. Input to the DDC is 3MHz sine wave. This signal multiplied with sine and cosine carrier signal and produced Inphase and quadrature phase output signal.

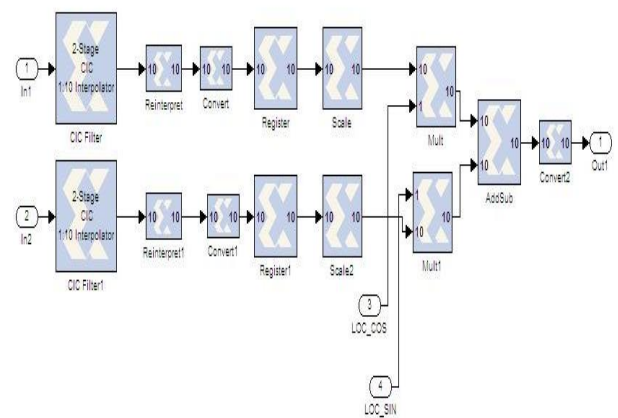


Fig 6: MATlab design of DUC

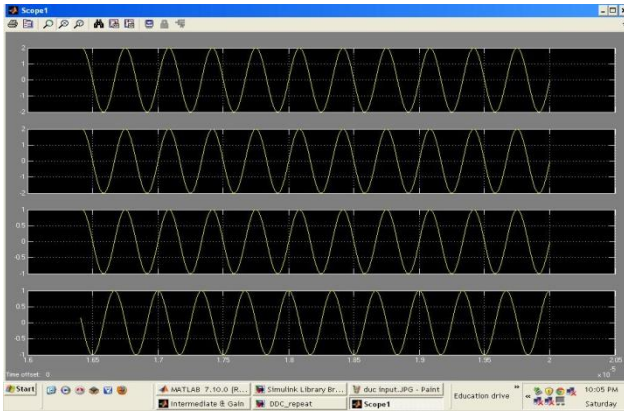


Fig 7: Input and carrier signals

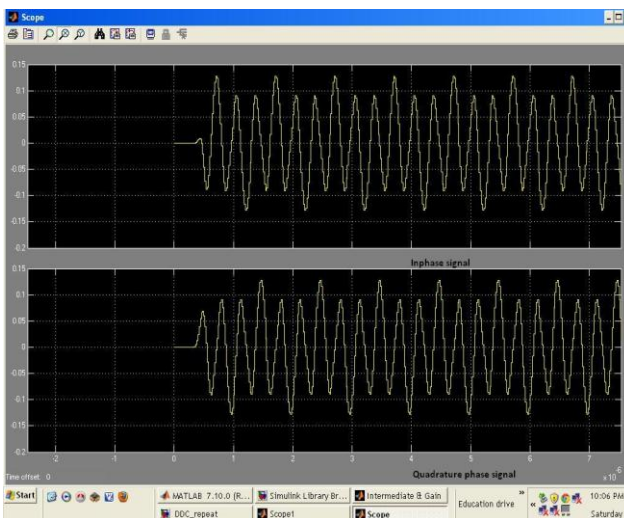


Fig 8: DDC output

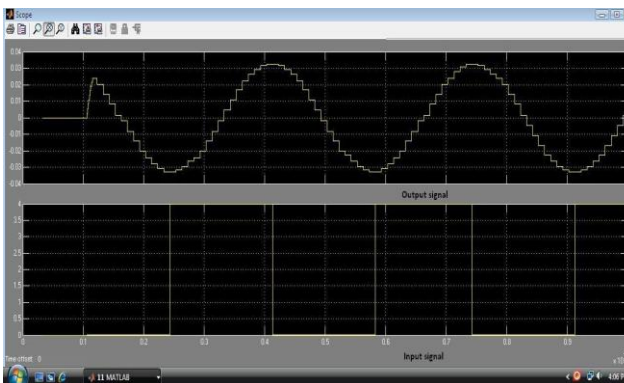


Fig 9: DUC Input and Output Signal

## 4. SYNTHESIS RESULTS

From the synthesis report, the design used 31% of flip-flop's, 24% of look up tables, 38% of slices out of total available in Virtex 4 FPGA board. The power consumed in this design is 52.6mWatts and the maximum operating frequency is up to 336.1MHz and total time taken for output is 2.93ns.

## 5. CONCLUSION

Synthesis and simulation results shows that designed DUC and DDC performance is better than other designs. The power consumed in this design is 52.6mWatts and the maximum operating frequency is up to 336.1MHz and total time taken for output is 2.93ns.

## 6. REFERENCES

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