Implementation of Reversible Logic Gate in Quantum Dot Cellular Automata

Rubina Akter
Department of Information and Communication Technology
Mawlana Bhashani Science and Technology University
Tangail-1902, Bangladesh

Nazrul Islam
Department of Information and Communication Technology
Mawlana Bhashani Science and Technology University
Tangail-1902, Bangladesh

Sajjad Waheed
Department of Information and Communication Technology
Mawlana Bhashani Science and Technology University
Tangail-1902, Bangladesh

ABSTRACT
Quantum Dot Cellular Automata (QCA) is a nanotechnology with many attractive features such as higher speed, smaller size, higher switching frequency, higher scale integration and low power consumption. There are many researches have been reported on the design of reversible logic gates compared to the reversible TR. This paper proposes a modified design of the reversible Feynman gate and also propose reversible TR gate, then design 1-bit comparator using reversible TR gates and Feynman Gate. The result shows an efficient technique to design Feynman gate and one bit comparator. The proposed gates can be easily used to design complex circuits which are used in the Central Processing Unit (CPU) and microcontrollers.

General Terms
Reversible logic gates, Quantum Dot Cellular Automata.

Keywords
QCA, Reversible logic gates, Feynman gate, TR Gate, Majority Voter.

1. INTRODUCTION
Quantum Dot Cellular Automata (QCA) is a promising alternative of Complementary metal–oxide–semiconductor (CMOS) technology [1]. The fundamental unit of QCA is QCA cell. Each QCA cell consists of two electrons with four quantum dots which positioned at the vertices of a square [2, 3, 4]. In the QCA configuration, there is no need for traditional interconnects.

Quantum dots are nano structures created from standard semi conductive materials. These structures are modeled as quantum wells. QCA based designs are depended upon the QCA wire, three input majority gate and inverter gate. An array of QCA cells acts as a wire and is able to transmit information from one end to another [5, 6]. Majority Voter (MV), inverter and the binary wire are the most popular QCA devices. The QCA wire is a basic QCA element. The QCA wire is a set of QCA cell. These QCA cells decorate in a horizontal row. The array of QCA cells propagates information from one end to another through the wire [7]. The 3-input majority gate is composed of five cells; three inputs, one output and a center cell. The center cell is known as the device cell that performs the calculation [8]. An inverter gate is one of the most important basic logic elements in QCA to make a complete logical set. Various circuits have been designed by QCA technology [3, 8, 9] with the help of the inverter gate.

Previously, a numerous number of studies [10, 11] reversible logic are a promising computing paradigm in quantum computing. The main attractive features of the reversible logic circuits are these circuits do not lose information. Reversible circuits are comprised of reversible logic gates. There are a great number of reversible logic gates are described in different papers. These reversible gates are very helpful in designing reversible logic circuits which are very important in Quantum Cellular Automata and optical computing.

Researchers have addressed the design of reversible adders, multipliers, sequential circuits such as in [11, 12, 13]. Among all the reversible logic gate Feynman gate and TR gate is the most important reversible logic gate in QCA. These reversible logic gates are used in many different fields such as Low power CMOS, quantum computer, communication etc. We are highly interested to work with this reversible logic gates. The paper presents the design structures of the reversible Feynman gate and the TR gate in the QCA and also presents the simulation results of each individual design.

This paper is decorated in six sections. Section 1 provides the introduction and related works about QCA. Section 2 gives a brief overview of the working methodology. Section 3 presents the conventional design structure of the proposed circuit in QCA. In the section 4 discussed about the simulation results using a detailed comparison with regard to different characteristics of these presented designs. In section 5 is summed up the proposed circuits and conclude with a future work.

2. METHODOLOGY
The research is apportioned into three parts. Firstly, a literature review is performed to find out the required software tools and selected to verify the proposed circuit. At the layout level is tested several approximate simulators such as the bistable simulation engine and the nonlinear approximation methods. These methods are iterative and do not produce the actual estimates. At last, the QCA Designer 2.0.3 is selected and this simulation tool is described [6].

Secondly, configure the software installation is held to design and test the circuit. At the layout, small building block of QCA is designed and then simulated for testing its correctness. Then these small blocks of QCA are joined together by QCA wire to produce the proposed circuit.

Finally, the perfectness of the circuit is tested by the simulation tools of QCA Designer 2.0.3 [14]. The simulation tools processed the circuit and produce the required waveform for that logical circuit. In the simulation, QCA Designer 2.0.3 provides some parameter that contains default values such as cell size, number of samples, radius of effect, relative permittivity, Relaxation time, etc. In the paper, the simulated waveform for each individual circuit fully matches the logical

input and output.

3. TECHNICAL IMPLEMENTATION

3.1 Reversible Feynman Gate

The QCA implementation for the Feynman gate shown in Figure-1 has been proposed by different authors [15]. Here, X and Y are the inputs and the outputs are X and OUT1. The logical expression of this circuit is X = X, OUT1 = X⊕Y.

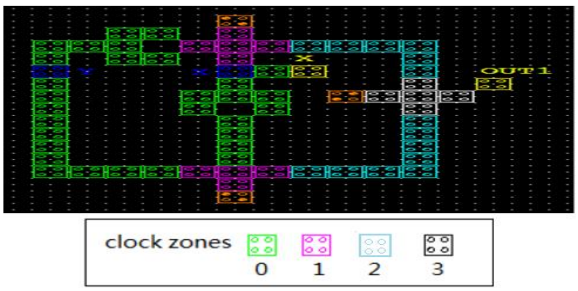

Fig 1: QCA layout structure of the Feynman gate.

We have proposed a different QCA based design of Feynman gate shown in Figure-2. This layout has been designed to provide the most efficient configuration in terms of cell count, latency and complexity. The inputs are denoted as A and B, and the outputs are P, Q. The logical expression of this circuit is P = A, Q = A⊕B.

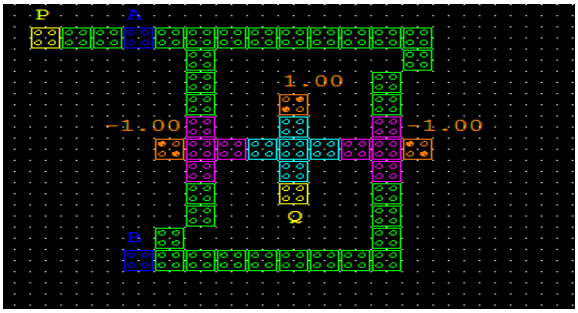

Fig 2: QCA layout structure of the proposed Feynman gate.

3.2 Thapliyal Ranganathan Gate

The proposed reversible TR gate is a 3 input 3 output gate. A novel design structure of a TR gate in QCA is shown in Figure-3. Here A, B, C are the inputs and P, Q, R are their corresponding outputs. The logical expression of this circuit is P = A, Q = A⊕B, R = (A.B') ⊕ C.

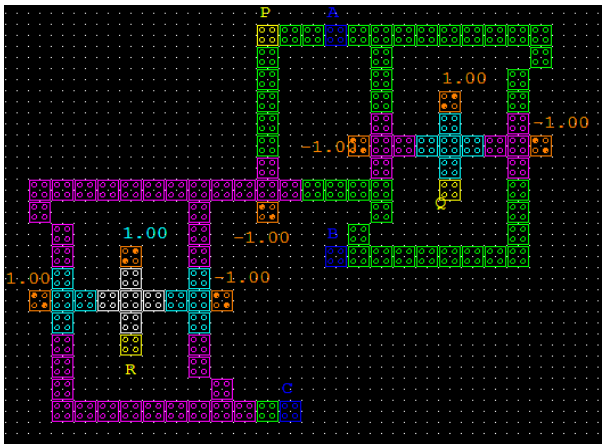

Fig 3: QCA layout structure of TR Gate.

3.3 Proposed 1-bit Comparator design of Feynman Gate

A 1-bit comparator accepts two 1-bit numbers, A and B as inputs and produces an output indicating whether A>B, Y1 = AB', For A = B, Y2 = A NOR B, For A<B, Y3 = A'B. QCA implementation of 1-bit comparator by Feynman gate is shown in Figure-4. Here A, B are the inputs and Y1, Y2, Y3 are their corresponding outputs. The logical expression of this circuit is Y1= AB', Y2 = A NOR B and Y3 = A'B.

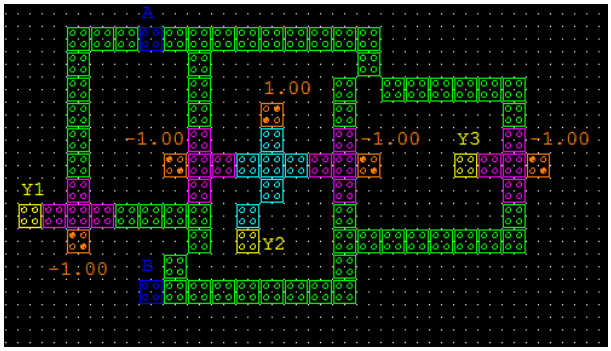

Fig 4: QCA layout structure of the proposed 1-bit Comparator design of Feynman Gate.

3.4 Proposed 1-bit Comparator Design by TR Gate

QCA implementation of 1-bit comparator by TR gate is shown in Figure-5. Here A, B are the inputs and Y1, Y2, Y3 are their corresponding outputs. The logical expression of this circuit is Y1= AB', Y2 = A NOR B and Y3 = A'B.

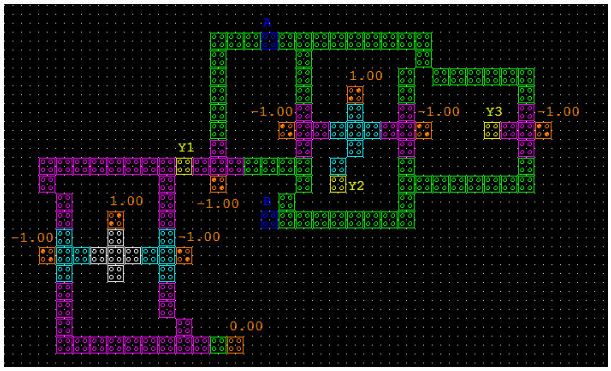

Fig 5: QCA layout structure of the proposed 1-bit Comparator design by TR Gate.

4. RESULTS AND DISCUSSIONTION

In the section is discussed about the results of the simulated waveform of the proposed design. We have implemented two types of reversible logic gate and simulated using 2.0.3 QCA designer. The functionality of the circuit is verified from the simulated waveform. We also show a comparison of the implementation based on the number of cells used, required area and time delay.

At the first portion of the results is described the simulated waveform of Feynman gate shows in Figure-6 and Figure-7. Secondly, shows a comparison of reversible Feynman gate design in Table 1 by which we can compare more efficient Feynman gate design. We also described the simulated waveform of the reversible TR gate. At the last portion of this section we depict more efficient design of 1-bit comparator implemented by Feynman gate and TR gate.

4.1 Simulation Results of Feynman Gate

The proposed designs were functionally simulated using the QCA Designer 2.0.3. The following parameters are used for a Bistable Approximation: cell size=18nm, number of samples=12800, radius of effect=65.000000nm, relative permittivity=12.900000, clock high=9.800000e– 022 J, clock-low=3.800000e–023J, clock-amplitude factor=2.000000, layer separation=11.500000, maximum per sample=100, Temperature=1.000000, Reluxation time=1.000000e-015, Time step 1.000000e-016. Most of the above mentioned parameters are default values in QCA Designer.

Figure-6 shows the input, output waveforms of the existing Feynman gate. Here, the input signals are X and Y. And the output signals are OUT1 and X. The logical expression for this waveform is X=X, OUT =X⊕Y.

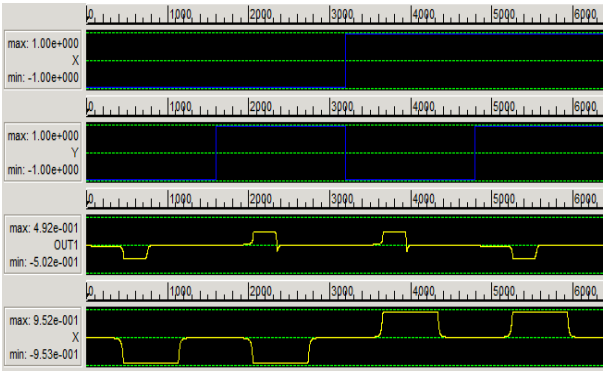

Fig 6: Simulated waveform for existing Feynman gate.

Figure-7 shows the input, output waveforms of the proposed Feynman gate. In Figure-7 we define the input as A and B. And the output signals as P and Q. The logical expression of this Feynman is P=A, Q=A⊕B.

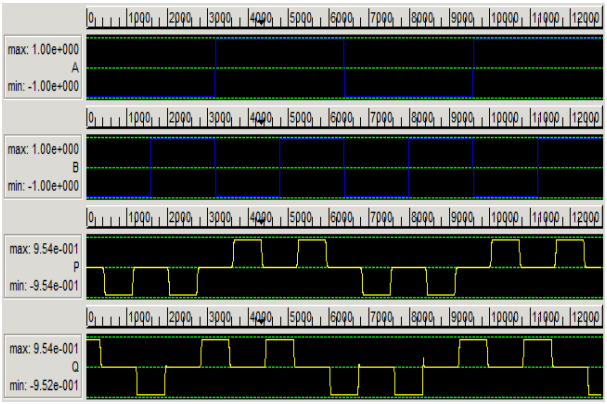

Fig 7: Simulated waveform for proposed Feynman gate.

Table 1 shows a comparison between the existing Feynman gate and the proposed Feynman gate.

Table 1. Comparison of Feynman gate designs

Design	Number of cells	Area (in μm^2)	Time delay
Existing Feynman Gate	65	0.09	1
Proposed Feynman Gate	51	0.07	0.5

Table 1 gives the comparison of proposed designs with the conventional design. It is evident from Table 1 that the proposed designs are more efficient in terms of cell count, area and time delay. Therefore, we proposed the design as First Operating Feynman (FOF) gate.

4.2 Simulation Results of TR Gate

The proposed TR gate functionally simulated using the QCA Designer 2.0.3. Figure 8, shows the input, output waveform of the proposed TR gate. In this simulated waveform the inputs are A, B, C. And the output signals are P, Q, R. The logical expression for this waveform, P=A, Q=A⊕B, R= (A. B') ⊕ C.

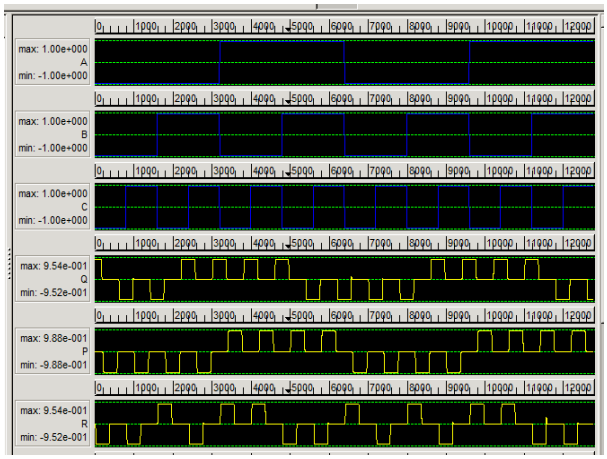

Fig 8: Simulated waveforms for TR gate

The Table 2 presents a data table of TR gate.

Table 2. Features of proposed TR gate

Design	Number of cells	Area (in μm^2)	Time delay
TR Gate	113	0.20	1

The above table shows that, the TR gate consists of 113 cells and it covers 0.20 μm^2 areas with time delay 1.

4.3 Simulation Results of 1-bit Comparator

Figure-9 shows the input, output waveforms of 1 bit comparator implemented by Feynman gate. In this simulated waveform we define the input as A, B and the output signals as Y1, Y2 and Y3. The logical expression for this waveform is Y1=AB', Y2=A NOR B, Y3=A'B.

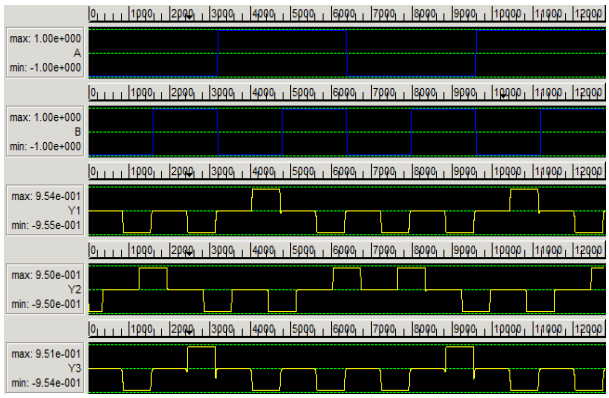

Fig 9: Simulated waveforms for 1-bit Comparator by Feynman Gate.

Figure-10 shows the input, output waveforms of 1 bit comparator implemented by TR gate. In this simulated waveform we define the input as A, B. And the output signals as Y1, Y2 and Y3. The logical expression for this waveform is Y1=AB', Y2=A NOR B, Y3=A'B.

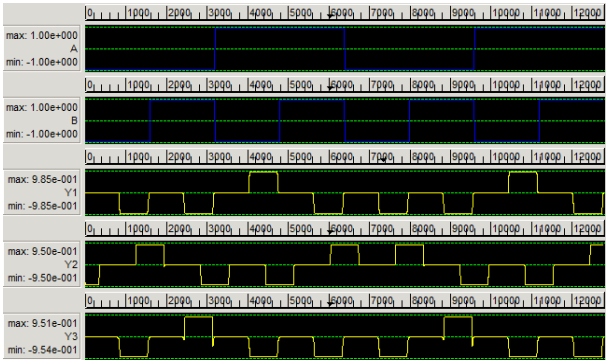

Fig 10: Simulated waveforms for 1-bit Comparator by TR Gate.

Table 3 shows a comparison between the 1-bit Comparator gate design by Feynman gate and TR gate.

Table 3. Comparison of proposed 1-bit Comparator designs

Design	Number of cells	Area (in μm^2)	Time delay
1-bit Comparator by TR	134	0.25	0.5
1-bit Comparator by Feynman	87	0.11	0.5

Table 3 shows that 1-bit comparator designed by Feynman gate is composed of 87 cells and it covers 0.11 μm^2 areas. On the other side 1-bit comparator designed by TR gate is composed of 134 cells and it covers 0.25 μm^2 areas. It is also shown that 1-bit comparator designed by Feynman gate takes a less number of cell and area than the designed by the TR gate.

5. CONCLUSION

This paper explores an efficient structure of Feynman gate using QCA with reduced number of QCA cells compared to the previous designs as shown in Table 1. Also present the design of 1-bit Comparator circuit using Feynman gate and TR gate. The simulation results show that the proposed circuits perform well. During the design an attention is made to reduce the number of cells as well as to reduce the area. This paper helps to design, a higher complex computing circuit using reversible gates. These designs also useful for quantum computing, optical computing, DNA computing, digital signal processing (DSP). Hence, it concludes that the proposed design should be promising step towards the goal of low power design in nanotechnology.

The future work can be addressed as to design a full adder circuit implementing by the Feynman gate and TR gate.

6. REFERENCES

[1] Cho, H., & Swartzlander, E. E. (2009). Adder and multiplier design in quantum-dot cellular automata. *IEEE Transactions on Computers*, *58*(6), 721-727.

[2] Zhang, R., Walus, K., Wang, W., & Jullien, G. A. (2004). A method of majority logic reduction for quantum cellular automata. *IEEE Transactions on Nanotechnology*, *3*(4), 443-450.

[3] Hänninen, I., & Takala, J. (2010). Binary adders on quantum-dot cellular automata. *Journal of Signal Processing Systems*, *58*(1), 87-103.

[4] Kummamuru, R. K., Orlov, A. O., Ramasubramaniam, R., Lent, C. S., Bernstein, G. H., & Snider, G. L. (2003). Operation of a quantum-dot cellular automata (QCA) shift register and analysis of errors. *IEEE Transactions on Electron Devices*, *50*(9), 1906-1913.

[5] Walus, K., Jullien, G. A., & Dimitrov, V. S. (2003, November). Computer arithmetic structures for quantum cellular automata. In *Conference on Record of the Thirty-Seventh Asilomar, Signals, Systems and Computers, 2004.* (Vol. 2, pp. 1435-1439). IEEE.

[6] Walus, K., Dysart, T. J., Jullien, G. A., & Budiman, R. A. (2004). QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata. *Transactions on Nanotechnology, IEEE 3*(1), 26-31.

[7] Lent, C. S., & Tougaw, P. D. (1993). Lines of interacting quantum-dot cells: A binary wire. *Journal of Applied Physics*, *74*(10), 6227-6233.

[8] Tougaw, P. D., & Lent, C. S. (1994). Logical devices implemented using quantum cellular automata. *Journal of Applied physics*, *75*(3), 1818-1825.

[9] Ahmad, F., Bhat, G. M., & Ahmad, P. Z. (2014). Novel Adder Circuits Based On Quantum-Dot Cellular Automata (QCA). *Circuits and Systems, 2014.*

[10] Garipelly, R., Kiran, P. M., & Kumar, A. S. (2013). A Review on Reversible Logic Gates and their Implementation. *International Journal of Emerging Technology and Advanced Engineering, Volume 3.*

[11] Haghparast, M., Jassbi, S. J., Navi, K., & Hashemipour, O. (2008). Design of a novel reversible multiplier circuit using HNG gate in nanotechnology. In *World Appl. Sci. J.*

[12] Thapliyal, H., & Srinivas, M. B. (2006). Novel reversible multiplier architecture using reversible TSG gate. *arXiv preprint cs/0605004*.

[13] Bruce, J. W., Thornton, M. A., Shivakumaraiah, L., Kokate, P. S., & Li, X. (2002). Efficient adder circuits based on a conservative reversible logic gate. In*VLSI, 2002. Proceedings. Annual Symposium on IEEE Computer Society Annual Symposium on* (pp. 74-79). IEEE.

[14] "QCADesigner" http://www.mina.ubc.ca/qcadesigner [Online; Accessed: 29-July-2014].

[15] Rahman, M. A., Khatun, F., Sarkar, A., & Huq, M. F. (2013). Design and Implementation of Feynman Gate in Quantum-dot Cellular Automata (QCA). *International Journal of Computer Science* Issues, Vol. 10, Issue 4, No 1