Cost Efficient Fault Tolerant Decoder in Reversible Logic Synthesis

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ABSTRACT
Fault Tolerant reversible decoders are the prerequisite of high performance computing systems. In this paper, an optimized reversible fault tolerant decoder has been proposed by using novel cost effective gates named Reversible Fault Tolerant Decoder (RDC) and Double Fredkin Gate (DFG). Several lower bounds on the numbers of gates, garbage and quantum costs are also proposed to generalize the architecture of *n*-to-2^n reversible decoder. The comparative performance analysis shows that the proposed design outperforms the existing designs in terms of number of gates used, quantum cost, delay, ancilla inputs and design complexity.

General Terms
Reversible Computing, Quantum Computing.

Keywords
Reversible Decoder Circuit, Quantum Computing, Fault Tolerant, Low Power Computing.

1. INTRODUCTION
Controlling the flow of the input signals by others, digital circuits generate one or more functional output(s). Expunction of input signals dissipates heat and fan-out limits design rigidity performing over long time. During execution of every single instruction, *kTln*(2) joule of energy is wasted because of converting to heat due to per bit erasing, where *T* is the operating temperature in kelvin and *k* is the Boltzmann's constant [1]. Reversible logic circuits condense total energy dissipation due to input signal erasing to zero through providing a unique mapping between the input and output states [2]. Reversible logic also contributes to Quantum Computing [3], Q-Dot Cellular Automat [4], DNA technology [5], Program Testing & Debugging [6], Programmable Devices [7], Discrete Event Simulation, extremely efficient algorithm design and many more.

Moreover, parity checking is one of the most popular methods for single level fault detection in the communication industry. Usually, most of the arithmetic and other processing circuits tend not to preserve the parity and thus intermediate checking is necessary. If the parity of the input data can be conserved during the course of the computation then the intermediate checking would not be required. Thus, Reversible fault tolerant logic circuits preserve input bits and also facilitate the detection and correction of bit errors that produced by itself [8].

Reversible fault tolerant decoder is a combinational circuit that converts binary information of n-input lines to a maximum of 2^n unique output lines. Decoder circuits are used in many computing components such as n-to-2^n decimal to binary decoder, random access memory, instruction processing in control unit, etc. In this paper, the generic architecture of reversible decoder with minimization of cost factors such as number of gates, garbage outputs, ancilla inputs, etc. is presented.

The rest of the paper is organized as follows: Section 2 describes about the preliminary concepts of reversible logic, fault tolerant methodology, quantum realization, etc. Proposed design of the reversible fault tolerant decoder circuit has been presented in Section 3. Several lower bounds of reversible decoder are also presented in section 3. The performance analysis of the proposed design compared to existing is provided in section 4 with section 5 concluding the paper.

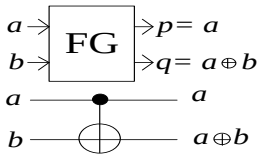
2. BACKGROUND STUDY
This section introduces some preliminary information about reversible logic circuits and their characteristics along with fault tolerant reversible circuits and decoders.

2.1 Reversible Logic
Preserving the inputs of a digital circuitry results in the reuse of logic bits, which can be very useful in reducing energy loss. Reversible computing is the technology that provide exclusive mapping between the inputs and outputs which leads to the reusability of bits. Any reversible circuit consists of one or more reversible unit component(s), called Reversible Gate performs multiple classical logical operations (AND, OR, NOT, etc.) in single clock cycle [9]. Fundamentally, fan-outs and feedback are strictly prohibited in reversible computing. Let, the input vector be $I_v = \{I_{n-1}, I_{n-2}, \cdots\cdots, I_0\}$ and the output vector be $O_v = \{O_{n-1}, O_{n-2}, \cdots\cdots, O_0\}$ of any Reversible logic circuit then according to the above definition the relation between two vectors is, $I_v \leftrightarrow O_v$ [9].

2.1.1 Popular Reversible Logic Gates
Several reversible logic gates have been proposed in the past years. In this section we review these reversible logic gates.

2.1.1.1 Feynman Gate (FG)
Feynman gate [10] is also known as Controlled-NOT gate, is a 2×2 reversible gate that can be described as follows:

$$I_v = \{a, b\} \text{ and } O_v = \{p = a, q = a \oplus b\}$$



Input		Output	
a	*b*	*p*	*q*
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

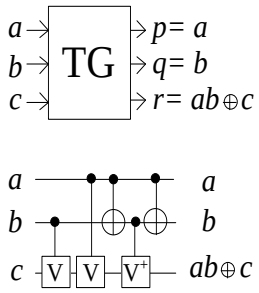
Fig 1: Feynman Gate

Where I_v and O_v are input and output vectors, respectively. Figure 1 shows the block diagram of Feynman Gate and corresponding table shows the unique mapping between input and output vectors of Feynman gate.

2.1.1.2 Toffoli Gate (TG)
Toffoli gate [11], also known as Controlled Controlled-NOT (CCNOT), is a 3x3 reversible logic gate. The Toffoli gate can be represented as:

$I_v = \{a, b, c\}$ and $O_v = \{p = a, q = b, r = ab \oplus c\}$

Where I_v and O_v are input and output vectors, respectively. Figure 2 shows the block diagram of Toffoli Gate and the truth values of input-output vectors in table retrieves unique mapping between input and output vectors.



Input			Output		
a	*b*	*c*	*p*	*q*	*r*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

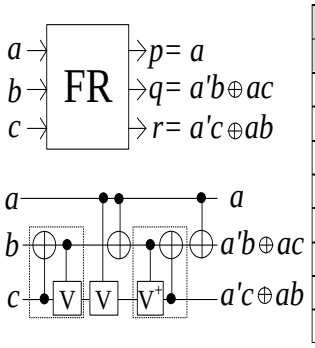
Fig 2: Toffoli gate

2.1.1.3 Fredkin Gate (FR)

Fredkin gate [12], also known as Controlled Permutation gate, is a 3x3 reversible logic gate. It can be represented as:

$I_v = \{a, b, c\}$ and $O_v = \{p = a, q = a'b \oplus ac, r = a'c \oplus ab\}$

Where I_v and O_v are input and output vectors. Figure 3 shows the block diagram of Fredkin gate and the tabular representation of input-output vectors also shows unique mapping between inputs and outputs of Fredkin gate.



Input			Output		
a	*b*	*c*	*p*	*q*	*r*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

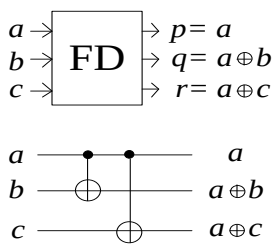
Fig 3: Fredkin Gate

2.1.1.4 Feynman Double Gate (FD)

The 3×3 dimensional Feynman Double gate [13] is another reversible gate, where the input vector (I_v) and the output vector (O_v) are defined as follows:

$I_v = \{a, b, c\}$ and $O_v = \{p = a, q = a \oplus b, r = a \oplus c\}$

The block diagram of Feynman Double gate and the unique mapping between input-output vectors is shown in figure 4.



Input			Output		
a	*b*	*c*	*p*	*q*	*r*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

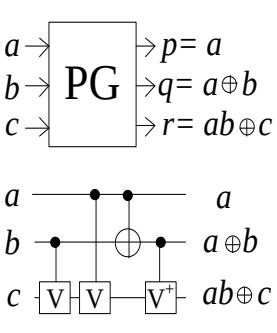
Fig 4: Feynman Double Gate

2.1.1.5 Peres Gate (PG)

Peres gate [14], also known as New Toffoli gate, combining Toffoli gate and Feynman gate is a 3x3 reversible logic gate. The input vector (I_v) and output vector (O_v) of Peres gate can be represented as:

$I_v = \{a, b, c\}$ and $O_v = \{p = a, q = a \oplus b, r = ab \oplus c\}$

Figure 5 depicts the block diagram of Peres gate, is equal with the transformation produced by combining a Toffoli Gate followed by a Feynman Gate.



Input			Output		
a	*b*	*c*	*p*	*q*	*r*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig 5: Peres Gate

2.1.1.6 MUX Gate (MG)

MG [15] is another 3x3 reversible gate (block diagram of MG gate is shown in figure 6). Let, the input-output vectors of MG are I_v andO_v, respectively. These can be represented as:

$I_v = \{a, b, c\}$ and $O_v = \{p = a, q = b \oplus c, r = a'c \oplus ab\}$

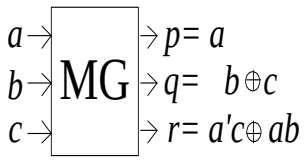


Fig 6: MUX gate

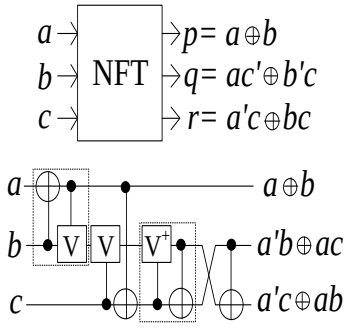
2.1.1.7 New Fault Tolerant Gate (NFT)

New Fault Tolerant Gate [15] is yet another 3x3 reversible gate which can be denoted as:

$I_v = \{a, b, c\}$ and

$O_v = \{p = a \oplus b, q = ac' \oplus b'c, r = ac' \oplus bc\}$

New Fault Tolerant gate is shown in figure 7 along with its truth table in table that verifies the unique mapping between input-outputs.



Input			Output		
a	*b*	*c*	*p*	*q*	*r*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	0	1

Fig 7: New Fault Tolerant Gate

In this proposed design, the new reversible gate has been presented which has been used to construct proposed minimum cost fault tolerant reversible decoder circuit.

2.1.2 Definitions of Measuring Standards

Definitions for some of the general terms used in reversible logics are presented in this subsection.

2.1.2.1 Gate Count

Frequently used logical operations are composed into gate level called Reversible Gate where the number of inputs is equal to the number of outputs and also preserves a unique mapping between input and output vectors [16].

2.1.2.2 Measuring Critical Path Delay

Propagating signal through input to output takes time which mostly depends on attached gates on pathway. The maximum number of gates between any input line and any output line is called the Critical Path Delay [17].

2.1.2.3 Garbage and Ancilla bits Analysis

The unused outputs of any reversible gate or circuit are called Garbage Output which will never be used in future rather than to check reversibility. On the other hand, one or more input lines get saturated to constant level (i.e. 0 or 1) is called Ancilla Input [18].

2.2 Fault Tolerant Methodology

Though reversible gates can recover from bit loss, they cannot detect bit errors in circuits. Fault Tolerant reversible circuit is capable to prevent errors at outputs.

On the other hand, according to Toffoli et. al., conservative reversible gates for which the hamming weight of its input and output are equal are also Fault Tolerant gates. Let, the input and output vectors of any Fault Tolerant gate are $I_v\{I_{n-1}, I_{n-2}, \cdots, I_0\}$ and $O_v\{O_{n-1}, O_{n-2}, \cdots, O_0\}$ where the following equations (i) and (ii) must be preserved:

$$I_v \leftrightarrow O_v \quad \text{(i)}$$

$$I_{n-1} \oplus I_{n-2} \oplus \ldots \oplus I_0 = O_{n-1} \oplus O_{n-2} \oplus \ldots \oplus O_0 \quad \text{(ii)}$$

Feynman Double gate, Fredkin gate and NFT gates are 3×3 dimensional and MIG is 4×4 dimensional fault tolerant gate having unique mapping between Input and Output vectors. The input parity and corresponding output parity of Fault Tolerant gates are same [18]. At the beginning, fault tolerant gate was also called Parity Preserving Gate.

Figure 3, 4 and 7 show the parity (in form of even/odd parity based on total number of one's) of any input state and corresponding output state are same. The operational truth value of fault tolerant Fredkin gate, Feynman Double and New Fault Tolerant gates, are also presented respectively.

2.3 Quantum Circuit Realization

The accessibility and operability of any reversible circuits can be validated by using relative quantum realization. A single data unit in Quantum Computing is called qubit [19] and the value of qubit is the superposition of constant $|0\rangle$ and $|1\rangle$. Any quantum operation is a unitary matrix and it performs multiplying the state of qubit which generates resultant state. Figure 8(a) shows the matrix representation of constant values $|0\rangle$ and $|1\rangle$ including quantum NOT operations. Quantum NOT works on single qubit, while the resultant state of qubit is the inversion of previous state as depicted in Fig. 8 (b).

$$|0\rangle=\begin{bmatrix}1\\0\end{bmatrix} \quad |1\rangle=\begin{bmatrix}0\\1\end{bmatrix} \quad \text{NOT}=\begin{bmatrix}0 & 1\\1 & 0\end{bmatrix} \qquad \begin{bmatrix}0 & 1\\1 & 0\end{bmatrix}\begin{bmatrix}0\\1\end{bmatrix}=\begin{bmatrix}1\\0\end{bmatrix}$$

(a) (b)

Fig. 8: (a) Matrix representation of quantum NOT, (b) The operation behavior of quantum NOT operation

Any reversible logic circuit that can be realized using quantum realization or any quantum operation is directional. The quantum realization of reversible circuit by using different quantum primitives impacts on the operational speed of computation. Total number of 2×2 quantum primitives which are used to realize any reversible circuit is called Quantum Cost of that reversible circuit. The quantum costs of popular reversible gates are almost fixed and are used to define the quantum cost of any reversible circuit. Figure 1-6 show the equivalent quantum representation of reversible gates. The summary of the quantum cost of popular reversible gates is shown in Table 1.

Table 1. Quantum Cost Calculation of Reversible gates

Reversible Gates	Operational Capacity	Quantum Cost
FG	XOR, NOT	1
TG	AND, OR, NOT	5
FR	AND, OR, NOT	5
FD	XOR, NOT	2
MG	XOR, AND, OR, NOT	4
NFT	XOR, AND, OR, NOT	5
PG	XOR, AND, OR, NOT	4

3. PROPOSED DESIGN OF REVERSIBLE DECODER

In this section, two novel 5×5 reversible fault tolerant logic gates called Reversible Decoder (RDC) and Double Fredkin Gate (DFG) have been introduced followed by the generalized architecture of proposed design of *n*-to-2^n reversible decoder.

Theorem 1: Reversible Fault Tolerant 2-to-4 Decoder circuit cannot be realized using 4×4 dimensional circuits.

Proof: Let, *a* and *b* be the inputs of a 2-to-4 decoder circuit and corresponding outputs be (*a'b'*, *a'b*, *ab*, *ab'*) and the resultant truth value can be represented using table 2. Total number of output of 2-to-4 decoder circuit is 4. By adding two constant input lines with primary inputs, parities of input-output combination can be summarized as shown in table 2.

Table 2. Parity matched score for Reversible Fault Tolerant 2-to-4 decoder circuit realized with 4x4 dimensional circuits

Inputs		Outputs				Parity Matched
a	*b*	*a'b'*	*a'b*	*ab*	*ab'*	
0	0	1	0	0	0	No
0	1	0	1	0	0	Yes
1	0	0	0	0	1	Yes
1	1	0	0	1	0	No

Number of parity mismatch is 2 and then required number of input line to fix input-output parity is 1. So, reversible fault tolerant 2-to-4 decoder circuit cannot be realized using 4×4 dimensional circuits.

Rest of the paper has described the structural organization of reversible fault tolerant decoder with minimum dimension.

3.1 Novel Reversible Gates

The proposed 5×5 reversible gates that has been used to construct the proposed reversible *n*-to-2^n decoder are described below:

3.1.1 Reversible Decoder (RDC)

The input vector, I_v and output vector, O_v of proposed 5×5 RDC are (a, b, c, d, e) and ($p = ab \oplus a \oplus c$, $q = ab \oplus b \oplus c$, $r = ab \oplus c$, $s = ab \oplus a \oplus b \oplus d$, $t = e \oplus a \oplus b$). The block diagram of the proposed RDC is depicted in Fig. 9(a) with the quantum circuit realization of RDC in Fig. 9(c) where the quantum cost of RDC is 9.

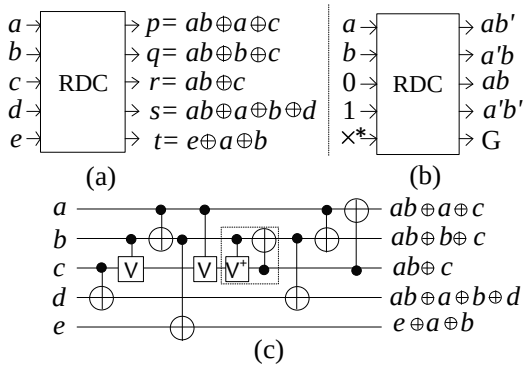


Fig. 9: Proposed Design of 2-to-4 Reversible Decoders

The 2-to-4 reversible fault tolerant decoder can be realized using RDC by setting c and d to LOW and HIGH, respectively. The last input of RDC (i.e. e) does not the affect the output of the 2-to-4 decoder which acts as garbage sink[1].

Proposition 1: Reversible 2-to-4 Fault Tolerant Decoder can be designed using 5×5 reversible RDC gates.

Proof: Let, a, b, c, d, e be the input and p, q, r, s, t be the output of 5×5 reversible RDC gate. The truth value of input-output lines of decoder can be represented by following table with publishing parity matched score.

Table 3. Parity matched score for Reversible Fault Tolerant 2-to-4 decoder circuit realized with 5×5 reversible RDC gates

Inputs					Outputs					Parity Match
a	*b*	*c*	*d*	*e*	*p*	*q*	*R*	*s*	*T*	
0	0	0	0	0	0	0	0	0	0	Yes
0	0	0	0	1	0	0	0	0	1	Yes
0	0	0	1	0	0	0	0	1	0	Yes
0	0	0	1	1	0	0	0	1	1	Yes
0	0	1	0	0	1	1	1	0	0	Yes
0	0	1	0	1	1	1	1	0	1	Yes
0	0	1	1	0	1	1	1	1	0	Yes
0	0	1	1	1	1	1	1	1	1	Yes
0	1	0	0	0	0	1	0	1	1	Yes
0	1	0	0	1	0	1	0	1	0	Yes
0	1	0	1	0	0	1	0	0	1	Yes
0	1	0	1	1	0	1	0	0	0	Yes
0	1	1	0	0	1	0	1	1	1	Yes
0	1	1	0	1	1	0	1	1	0	Yes
0	1	1	1	0	1	0	1	0	1	Yes
0	1	1	1	1	1	0	1	0	0	Yes
1	0	0	0	0	1	0	0	1	1	Yes
1	0	0	0	1	1	0	0	1	0	Yes
1	0	0	1	0	1	0	0	0	1	Yes
1	0	0	1	1	1	0	0	0	0	Yes
1	0	1	0	0	0	1	1	1	1	Yes
1	0	1	0	1	0	1	1	1	0	Yes
1	0	1	1	0	0	1	1	0	1	Yes
1	0	1	1	1	0	1	1	0	0	Yes
1	1	0	0	0	0	0	1	1	0	Yes
1	1	0	0	1	0	0	1	1	1	Yes
1	1	0	1	0	0	0	1	0	0	Yes
1	1	0	1	1	0	0	1	0	1	Yes
1	1	1	0	0	1	1	0	1	0	Yes
1	1	1	0	1	1	1	0	1	1	Yes
1	1	1	1	0	1	1	0	0	0	Yes
1	1	1	1	1	1	1	0	0	1	Yes

By setting c= LOW (Zero), output lines (p, q, r, s) generate the operational truth value of 2-to-4 reversible fault tolerant decoder circuit. So, reversible 2-to-4 Fault Tolerant Decoder can be designed using 5×5 reversible RDC gates. ■

The comparison between proposed and existing 2-to-4 fault tolerant decoder circuits can be realized using table 4.

Table 4. Comparison between proposed and existing design of reversible 2-to-4 decoder circuit

Reversible Decoder	Total Gates	Total Garbage	Delay	Quantum Cost	Ancilla Input
Proposed	1	1	1	9	2
Existing [20]	3	2	2	12	4
Existing [21]	3	2	3	15	4

3.1.2 Reversible Double Fredkin Gate (DFG)

For designing reversible fault tolerant decoder circuit larger than 2-to-4 decoder, proposed design has used another new 5×5 reversible circuit named Double Fredkin Gate (DFG).

The input vector, I_v and output vector, O_v of the proposed 5×5 DFG is (a, b, c, d, e) and ($p = a, q = a'b \oplus ac, r = a'c \oplus ab, s = a'd \oplus ae, t = a'e \oplus ad$). The block diagram of the proposed DFG is depicted in Fig. 10(a) with the quantum circuit realization of DFG in Fig. 10(c) where the quantum cost of DFG is 10.

[1]**Garbage sink/ don't care Input** is another cost factor measurement criteria which has been presented for the first time in this paper. Any don't care inputs are considered as Garbage Sink which does not effect on any functional outputs or propagates garbage value to output line. In reversible network garbage output can be reduced using don't care input lines. For example, Feynman Double gate generates $a \oplus b$ operation with one garbage output and one constant input (shown in Fig. 9). But there is no effect of constant input on another required functional output i.e. $a \oplus b$.

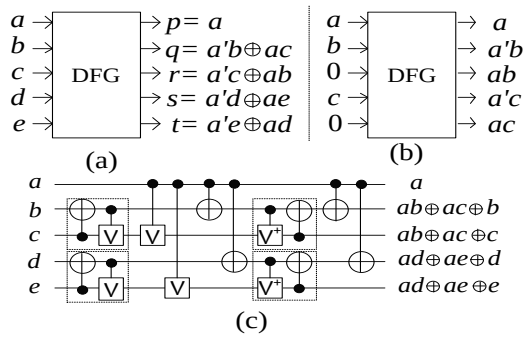


Fig. 10: Proposed design of 2-to-4 Reversible Decoder

The operational behavior of Double Fredkin gate is shown in Fig. 10(b) where input lines *d* and *e* are saturated to Low (Zero).

3.1.3 Reversible n-to-2^n Fault Tolerant Decoder

Proposed design of reversible *n*-to-2^n decoder circuit has been constructed using the cascading mode of RDC and DFG gates. Following algorithm (Algorithm I) describes the construction of Reversible *n*-to-2^n decoder circuit.

Proposition 2: Reversible *n*-to-2^n Fault Tolerant Decoder can be realized using $(2^{n-1}-1)$ number of 5×5 reversible gates where $n \geq 2$.

Proposition 3: Total number of Garbage to realize reversible *n*-to-2^n Fault Tolerant Decoder is $(n-1)$ where $n \geq 2$.

Proposition 4: Total number of Ancilla input to realize reversible *n*-to-2^n Fault Tolerant Decoder is (2^n-2) where $n \geq 2$.

Proposition 5: Total Delay to realize reversible *n*-to-2^n Fault Tolerant Decoder is $(2^{n-1}-1)$ where $n \geq 2$.

Algorithm I: Construction of *n*-to-2^n Reversible Fault Tolerant Decoder

Here *n* is the number of input of reversible fault tolerant decoder circuit [where $n \geq 2$].

Start

1. **IF** $n > 2$ **THEN**
2. **Use** single RDC gates as initial decoder generates the output of a *n*-to-2^n reversible decoder
3. **Repeat** Step 4 for *i*= 3 to *n*
4. **Cascade** 2^{i-2} DFG gates by using i^{th} input line
5. **End Loop**
6. **ELSE**
7. **Use** single RDC gates
8. **End IF**

End

According to above algorithm, pictorial representation of reversible fault tolerant 3-to-8 decoder circuit is shown in Fig. 11. Total numbers of RDC and DFG gates are 2 and 1, respectively. Total number of constant inputs is 6 and number of garbage outputs is 2. Since the quantum costs of RDC and DFG are 9 and 10 respectively, the quantum cost for 3-to-8 decoder circuit is 29 (9+2*10). Accordingly the delay is 3 and ancilla input is 6 which can be realized from Fig. 11 and propositions defined earlier.

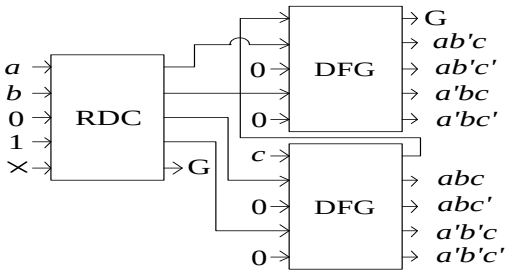


Fig. 11: Proposed design of Reversible Fault Tolerant Decoder Circuit

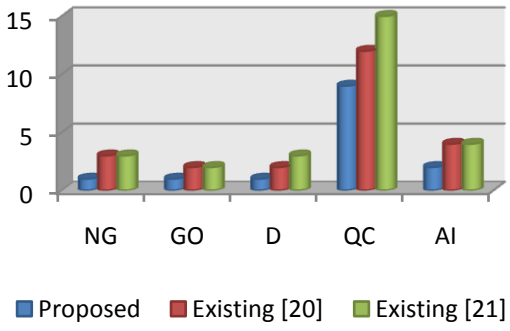
The comparison between proposed and existing 3-to-8 fault tolerant decoder circuits can be realized using Table 5.

Table 5. Comparison between proposed and existing design of reversible 3-to-8 decoder circuit

Reversible Decoder	Total Gates	Total Garbage	Delay	Quantum Cost	Ancilla Input
Proposed	3	2	3	29	6
Existing [20]	7	3	4	32	8
Existing [21]	≥7	≥3	≥7	≥35	8

4. PERFORMANCE ANALYSIS

Section 3 presented the design and proofs of a new *n*-to-2^n reversible fault tolerant decoder circuit and its performance compared to existing ones. This section will present a comparative performance analysis proposed designs with others. From Table 4 and 5 and graphical representation in figure 12 and 13, it can be established that proposed design of *n*-to-2^n decoder outperforms the existing designs in every aspects such as the proposed 2-to-4 decoder has 1 logic gates while existing decoder uses 3 with minimum quantum cost, delay and ancilla inputs. This proves the superiority of the proposed design than existing ones.



NG= No. of gates, GO=Garbage Output, D=Delay, QC= Quantum Cost, Ancilla Input=AI

Fig. 12: Comparisons between proposed and existing design of 2-to-4 decoders

5. CONCLUSIONS

Reversible circuits contribute to the efficient and high performance computing due to their reduced power consumption. And with fault tolerant capability the reversible circuits can perform with more rigidity and robustness. Thus motivated this paper presented two new reversible fault tolerant circuits namely Reversible Fault Tolerant Decoder (RDC) and Double Fredkin Gate (DFG). A new *n*-to-2^n fault tolerant decoder is also proposed combining RDC and DFG. In addition, this paper proposed several lower bounds on the

numbers of gates, garbage outputs and quantum costs.. The comparative analysis proves that the proposed design completely outperforms those of existing fault tolerant decoders producing the minimum cost n-to-2^n fault tolerant decoder. The prospective future research can be contributed to design n-to-2^n decimal to binary decoder following this circuit and this work can also be used in parallel circuits, network components etc. [22].

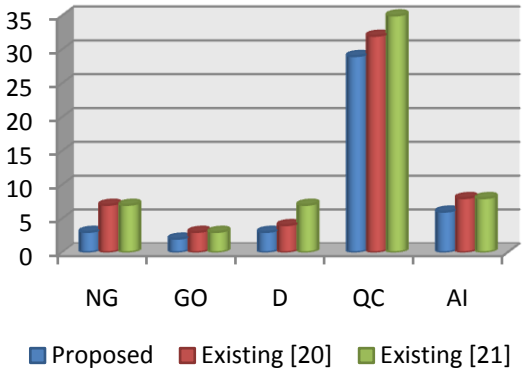


Fig. 13: Comparisons between proposed and existing design of 3-to-8 decoders

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