Design and Performance Evaluation of High Speed MAC Unit with Parallel Pipeline Technology

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ABSTRACT
In recent days advanced digital process demands more sophisticated parameters such as throughput, power and area. It is very difficult to maintain high throughput while maintaining optimum power consumption and cell area. In most of the digital systems multipliers are deciding their performance in terms of above parameters. In the present work high speed Vedic multipliers are designed with pipeline technology. As the MAC speed is decided by Vedic Multiplier, in the present paper Multiplier and Accumulator (MAC) is designed with two way pipeline technology to meet high throughput. Vedic Multipliers are used in designing MAC unit as they are fast multipliers and further enhancing the data speed. The MAC is implemented with Cadence Encounter(R) RTL Compiler.

Keywords
Vedic Multiplier, Throughput, MAC, data rate, Cadence, Pipeline, Parallel processing

1. INTRODUCTION
Vedic multipliers are high speed multipliers designed for high end applications such as digital signal processing, high speed arithmetic unit, Fast Fourier Transmission, parallel processing systems, Floating point Multiplier, Image processing, Business Management systems and many other heuristic systems. In the present scenario designing fast multiplier is key constraint in evaluating performance of a digital system. To achieve a fast and efficient multiplier it is essential to design a multiplier with lower power consumption, less area and good throughput [1][2][3]. The principles and various techniques involved in Vedic Multiplier are discussed and in the present paper the principle UrdhvaTiryagbyam [2][4] (vertically and crosswise) is adopted. When compared to the Traditional Multiplier the Vedic Multipliers reduces the steps involved in multiplication, and also improved the throughput. So Vedic Multipliers are helping digital systems in increasing the data speeds. The data speeds further enhanced in Traditional Vedic Multiplier (TVM) by incorporating a pipeline in multiplier and adder path[5].In Pipeline Vedic Multiplier (PVM) Technology while the present data is processing in adders, the next data can be fetched into multipliers using pipeline stages. The same PVM performance The above equation is evaluated from the MAC block diagram which is shown in figure 1.So the MAC is designed with parallel Pipeline and obtained good throughput. Before the MAC with parallel pipeline is designed, the Vedic Multiplier isimplemented withParallel Pipelined Vedic Multiplier (PPVM), and it isobserved less area [7] when compared with TVM.In PPVM the number of multipliers and can be further increased with the help of Multiplier and Accumulate (MAC) unit.

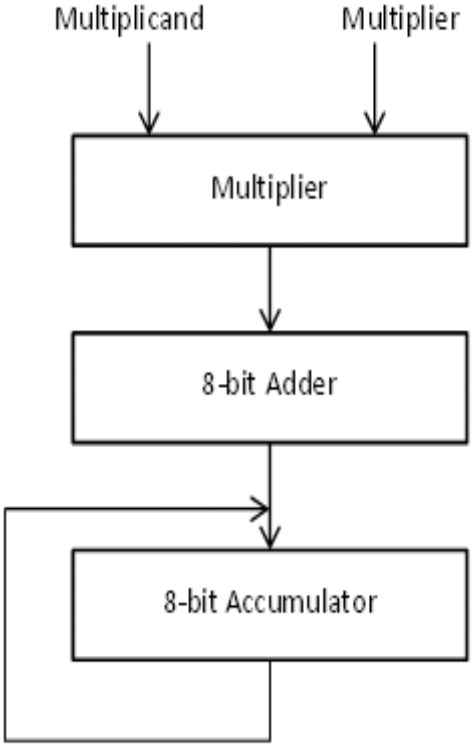

Figure 1 Block diagram of MAC Unit

In multiplier the adders will sum the partial products one by one in sequential order, but in MAC the sum of the partial product will be feedback to the adder through an accumulator. The MAC reduces the overhead about the overflow and improves the data fetching rates. But the MAC alone cannot improve the throughput of the Vedic multiplier. The MAC alone produces a large delay and it is observed with the following equation,

$$Totaldelayof MAC = delayof Vedicmultiplier + (2xadderdelay)$$

adders are reduced to achieve less area when compared with TVM and PVM. The worst case propagation delay in the 32X32 OptimizedMAC unit using Vedic multiplier case was found to be37.799ns [6].In the present paper an optimized MAC unit is designed and tested with 8-bit Vedic Multiplier with Cadense Encounter tool.

2. DESIGN OF MAC UNIT

In most of the MAC units, the Vedic Multipliers are used for designing, because of its enormous advantages in speed and power consumption. In the present work MAC unit is designed and compared using simple adder and Carry Save Look Ahead (CSLA) adder. In the proposed method the MAC unit is tested with parallel pipeline and compared with single pipeline method also. The MAC unit contributions in efficient computing in terms of speed, delay and cell area in applications such as DSPapplications like Convolution, Correlation, Discrete Fourier Transform, Fast FourierTransform, High speed arithmetic calculations and etc.[8].

In the present work MAC unit is first incorporated with Traditional Vedic Multiplier and the design is tested with both simple adders and CSLA adders. Secondly the MAC unit is designed by incorporating single pipeline and two way pipeline. In single pipeline Vedic multiplier technique high throughput around 10nsec is observed[5]. A 22nsec propagation delay is observed in traditional 8X8 MAC with Vedic Multiplier.A diminishing throughput is observed in traditional MAC unit when compared with Traditional Vedic Multiplier because of its large cell area which is represented in equation 1.

4. RESULTS

The RTL schematics are obtained for the enhanced MAC design in Cadence Encounter(R) RTL tool. In Enhanced method two channels are used and operated in alternative clock phases. These two channels operated in alternative clock phases to improve the data fetching rate. The first CSLA is used to add the partial products generated in previous stages of pipeline. The second CSLA is used to function as Accumulator. The buffers are used as intermediate buffers to implement the parallel processing. Finally high throughput of 6.25ns is observed in 8X8 MAC unit with PPVM. Operating the channels in alternate clock phases also optimizes the power consumption in the multiplier circuit. A layout is generated for MAC unit with PPVM in Cadense Encounter tool and it is shown in figure 7. The Comparision table of throughput, power and cell area of different MACs are presented in table 1.

3. PROPOSED MAC DESIGN Place

In the traditional MAC the throughput is further optimized by incorporating a pipeline in circuit design. Here a good throughput is recorded in MAC unit. The work is extended to MAC designing with Vedic multiplier and with single pipeline in which, a propagation delay of 15nsec is observed. Here it is again proved that pipeline always helps to enhance the speed in fast processing systems. The RTL schematic of MAC with PVM is shown in figure 4. Although the MAC unit with pipeline occupies the large cell area, due to the usage of parallel processing element pipeline it enhanced the data throughput. But when compared with TVM and PVM this throughput is not encourageable. So this work is further extended by incorporating two way pipeline to improve the performance of the MAC design. The two way pipeline is designed such that it works in opposite clock phases. This design is named as MAC with PPVM. The block diagram is shown in figure 6. In this design mesmerising results are achieved in throughput of 6.25ns is observed. The MAC with PPVM is designed in Cadense tool and simulated in Encounter tool. The RTL schematic of MAC with PPVM is shown in figure 5. In figure 4 only one channel is shown which is used for MAC with PVM. But where in the figure 4 two channels are shown which are used for MAC with PPVM. The two channels are represented in block diagram shown in figure 6.

Table 1: Comparision table of throughput between various MAC units

	AREA	POWER	DELAY
MAC	646	117.3mW	22nsec
MAC with PVM	520	111.2mW	15nsec
MAC with PPVM	1305	297.1mW	6.25nsec

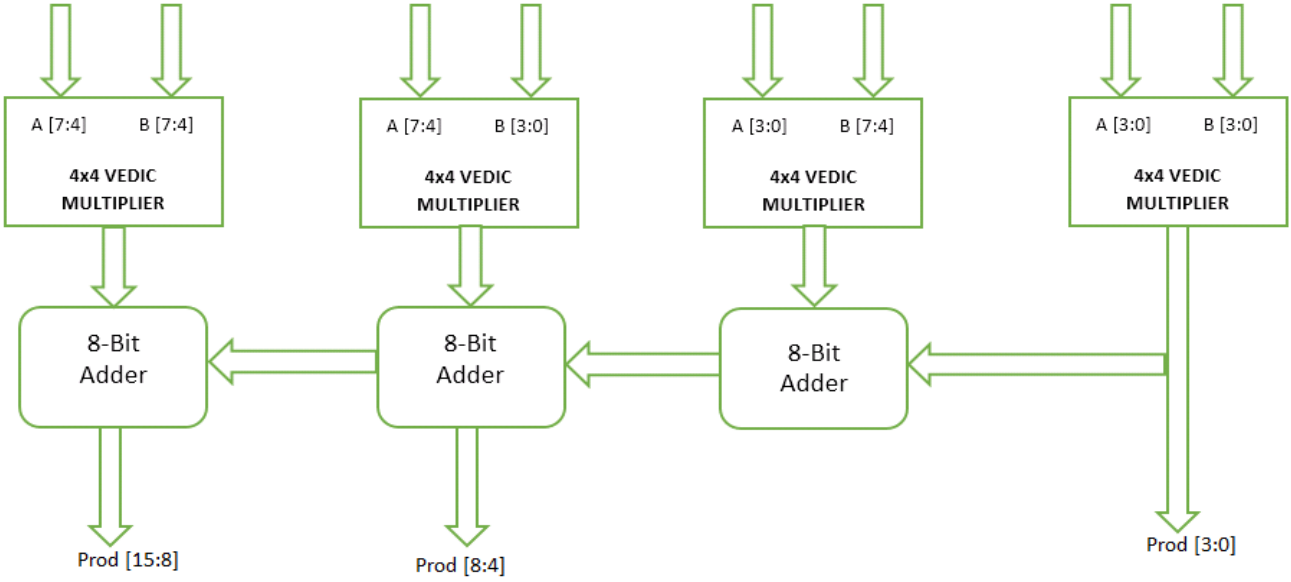

Fig. 2: 8x8 Traditional Vedic Multiplier using 4x4 Vedic Multipliers

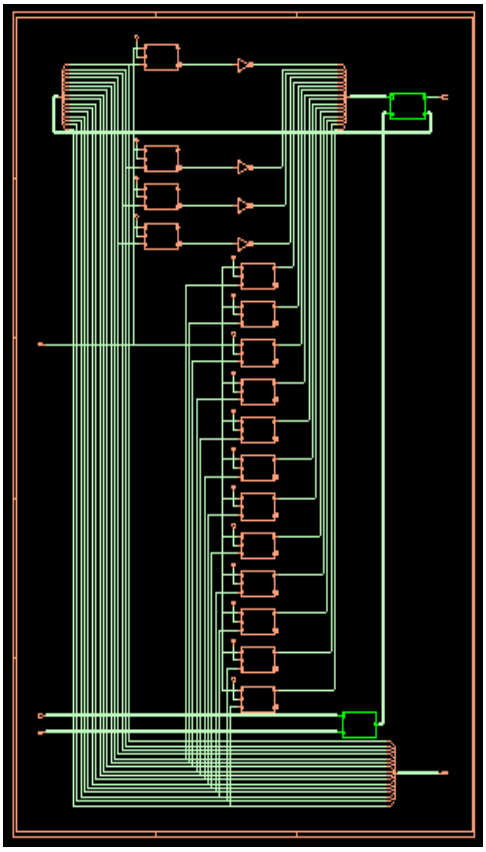

Figure 3: RTL Schematic of MAC with TVM

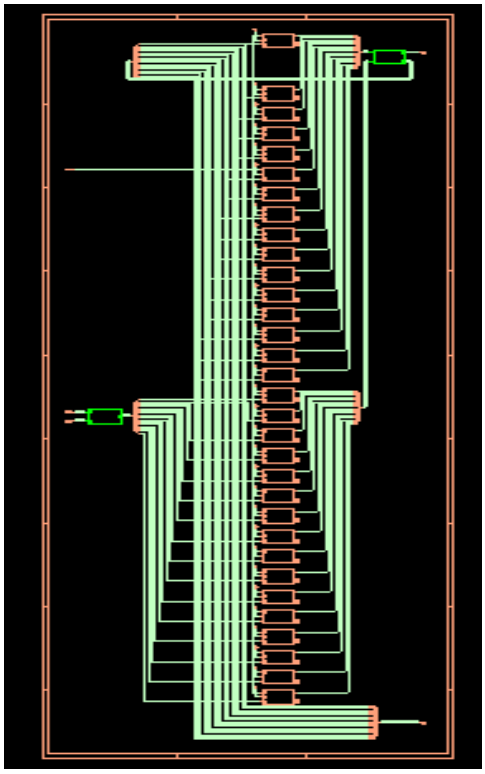

Figure 4: RTL Schematic of MAC with PVM

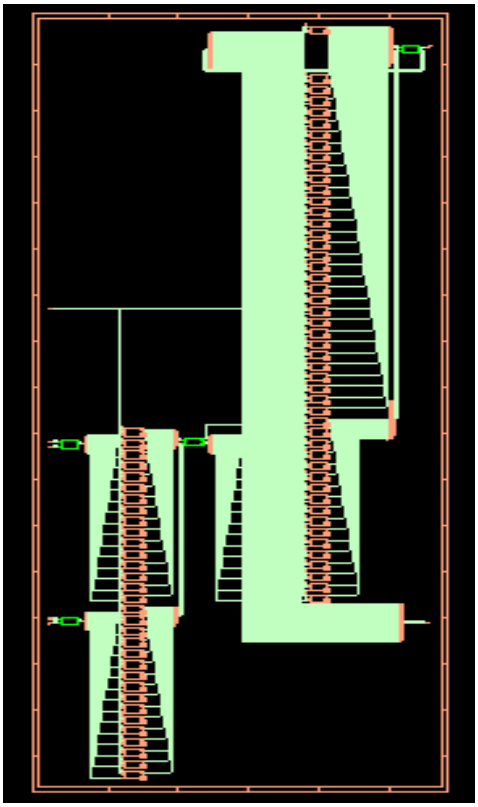

Figure 5: RTL Schematic of MAC with PPVM

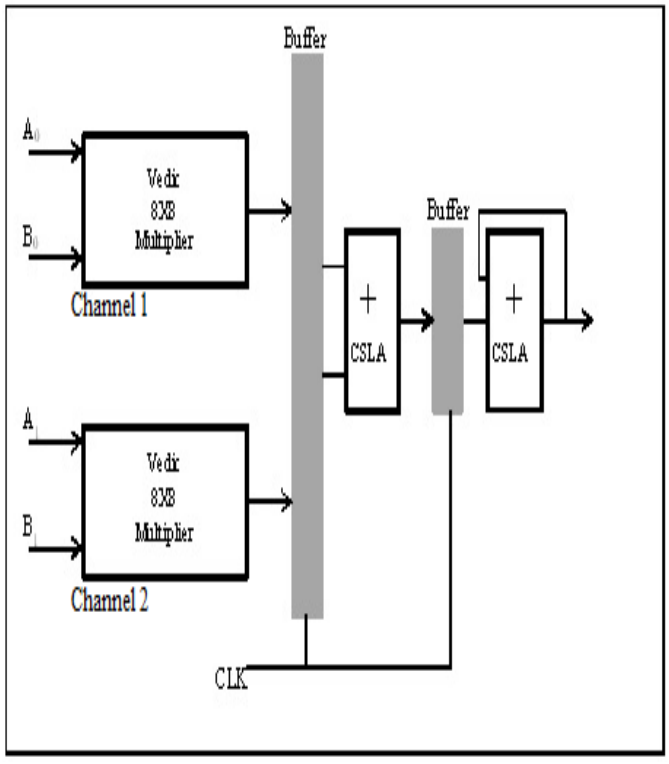

Figure 6: Optimized MAC method (MAC with PPVM)

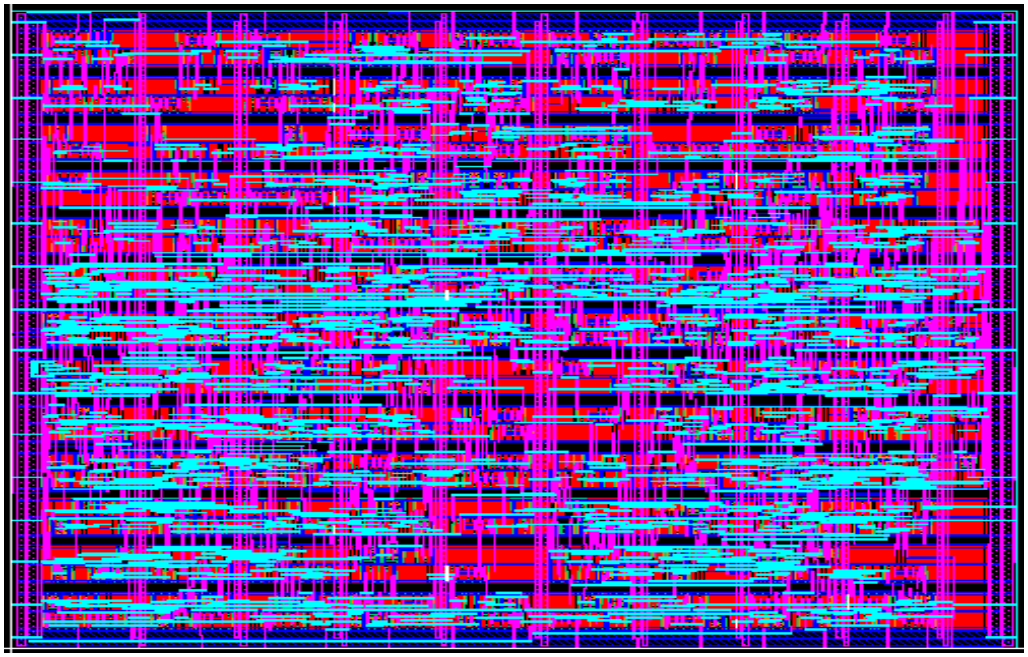

Figure 7: Layout diagram of MAC with PPVM

5. CONCLUSION

As the present digital systems performance depends totally on speed the present work mainly concentrated on high throughput. High throughput is achieved when compared with TVM, Traditional MAC unit, MAC with PVM. The circuits are designed and analysed in Cadense Encounter tool. The large cell area causes increase in power consumption. The power consumption somewhat controlled up to some extend by utilizing clock pulse efficiently.The channels are operated on alternate clock pulses. The circuit is operated in opposite phases of clock pulses also and reduces the wastage of waiting period time.

6. REFERENCES

[1] Booth, A.D., "A signed binary multiplicationtechnique," Quarterly Journal of Mechanics andApplied Mathematics, vol. 4, pt. 2, pp. 236– 240,1951.

[2] Jagadguru Swami Sri Bharath, KrsnaTirathji,"Vedic Mathematics or Sixteen Simple Sutras FromThe Vedas", MotilalBanarsidas,Varanasi(India),1986.

[3] PratikshaRai et al., "Design of Floating PointMultiplier Using Vedic Aphorisms", IJETT, Vol11, No 3, May 2014, pp123-126.

[4] Jagadguru Swami Sri BharatiKrsnaTilihjiMotilal Maharaja.(1986), VedicMathematics, et al. "Design And ImplementationOf Efficient Multiplier Using Vedic Mathematics,proc. Of Int. conf. on Advanced in Recent Technologies in Communication and computing",proc.Of Int. conf. on Advanced in RecentTechnologies in Communication and computing,2011.

[5] Y. Narasimharao et al., "Design of high speed Vedic multiplier withpipeline technology", JATIT, VOL 67, Issue no 3, September 2014.

[6] V.K.Karthik et al., "Design of Multiply and Accumulate Unit using Vedic Multiplication Techniques", IJSER, Vol 4 no6, june 2013.pp756-760.

[7] Y. N. Rao et al., "Simple and Efficient Low Power Parallel Pipelined Vedic Multiplier", Vol 9, NO 21, IJAER, pp9765-9774.

[8] Anveshkumar et al., "Low Power ALU Design by Ancient Mathematics", doi: 978-1-4244-5586-7/10/$26.00, IEEE, © 2010, pp862-865.