# Design of Low Voltage Low Power OP-AMP using DTMOS Technique

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## ABSTRACT
This paper demonstrates the design of low voltage, low power CMOS op-amp using DTMOS technique for low-power applications. The design goal is to achieve high gain, phase margin and minimum power dissipation at lower supply voltage. DTMOS transistor is proposed in this paper for the design of op-amp which replaces the normal CMOS transistors for designing a low power, low voltage two stage op-amp. A dc gain of 96.38 dB, a phase margin of 71.46º by achieving a unity gain bandwidth of 4.077 MHz while operating at 1V supply voltage. The performed simulation results show a power dissipation of 12.19 µW is achieved under 5 pF load in this design. The design and analysis is performed using 180 nm CMOS technology in Cadence Virtuoso ADE**.**

## Keywords
Low power applications, Diff-amp, op-amp, DTMOS, Low power, Low voltage**.**

## 1. INTRODUCTION
From the past few years due to the extensive growth of market for portable devices such as cell phones, portable computers, other low power applications and also the design of analog circuits which requires low power, low voltage with high performance has become an important issue now a day's [2]. One of the limitations for implementation of portable devices and design of other low power circuits at low voltage is the threshold voltage ($V_{th}$). For this reason reduction of threshold voltage is necessary for low-power, low-voltage operation. DTMOS technique is the best solution for reduction of threshold voltage ($V_{th}$).

Therefore, an effective method for reducing power consumption is to reduce the power supply voltage ($V_{dd}$). Reduction of power supply voltage ($V_{dd}$) depends on one of the factor that is threshold voltage. So one of the possible solutions is to implement CMOS transistors with dynamic $V_{th}$, which is the basic idea behind DTMOS technique [1]. DTMOS transistor shows high threshold characteristic when it is in "off" condition to minimize the leakage current as well as, it behaves as a low threshold device in "on" condition at lower supply voltages for high current driving capability. This is one of the feature that makes DTMOS technique most suitable for low-voltage, low power applications.

## 2. DTMOS TECHNIQUE
In DTMOS technique the body and the gate of a DTMOS transistor are tied (or) biased at the same potential as shown in Fig. 1. When a high voltage is applied to the gate of a DTMOS transistor, the front channel of the device is turned on. Due to the body-tied-to-gate structure, the body potential becomes high. By this the threshold voltage becomes low due to the body effect and thus the driving capability of the front channel increases [1].

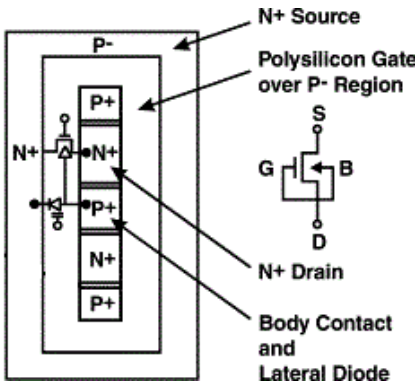


**Fig 1: Dynamic threshold MOSFET**

When a low voltage is applied to the gate, the front channel turns off, so the body voltage becomes low, then due to the body effect, the threshold voltage of the front channel is recovered, thus the leakage current is small. As the gate and body voltage increase, the threshold voltage reduces. With this DTMOS logic the transistor gets into "on" mode at low $V_{th}$ which results in the operation of circuit at low power and low voltages [1].

## 3. PROPOSED OPTIMIZED DESIGN
Here in this op-amp design firstly a Single stage Differential amplifier is designed as an initial stage of an op-amp which is then combined with the cascode stage to design a two stage op-amp. The diff-amp uses two DTMOS transistors at input stage and current mirror as load for that input stage. The design of diff-amp is shown in Fig. 2. By this DTMOS based Diff-amp we have achieved a gain of 45.65 dB as shown in Fig. 3.

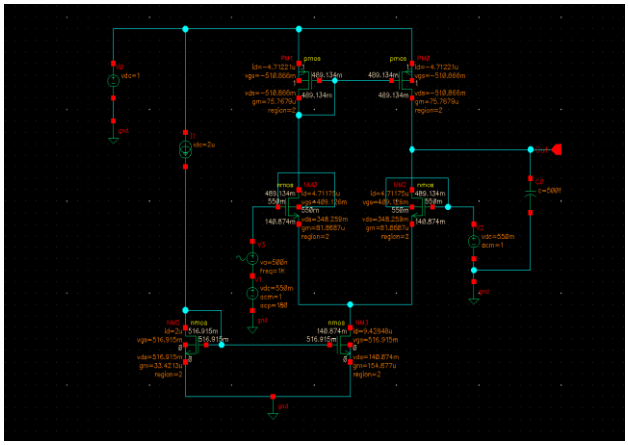

**Fig 2: DTMOS Based Diff-amp**

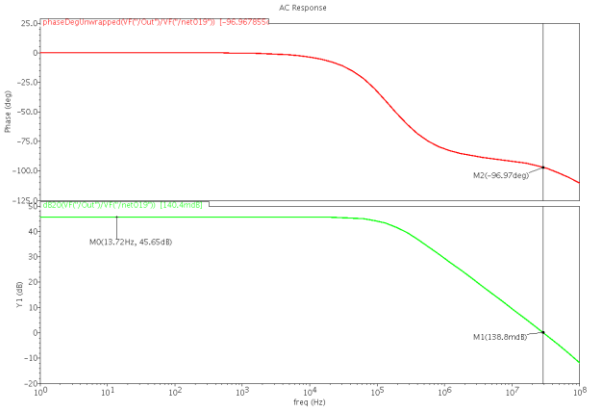


**Fig 3: Gain of Diff-amp**

## 4. DESIGN OF TWO STAGE OP-AMP

An operational amplifier is a high-gain voltage amplifier with a differential input, usually a single-ended output.

Fig 4 shows the proposed design of two stage op-amp using DTMOS technique. This structure consists of two differential pairs with current mirror as load. We used DTMOS transistors pairs (M1, M2, M5 and M6) in both the differential pairs. The current mirror pair M7 and M8 defines the DC gain. The cascode stage, M5 and M6 include an increase of bandwidth and gain of the amplifier. A compensation network $R_C$ and $C_C$ is chosen to achieve desirable phase.

### *A. Power Dissipation*

Power dissipation of the proposed op-amp is calculated using equation:

$$P.D=I_{DD} * V_{DD} \quad (1)$$

### *B. Gain*

The DC gain of proposed op-amp is given in the below equation [4]:

$$A_0 = (g_{m2} + g_{mb2})\left(\left[(g_{m6} + g_{mb6})r_{o6}(r_{o2} \| r_{o6})\right] \| r_{o8}\right) g_{m9}(r_{o9} \| r_{o10}) \quad (2)$$

While $g_{mb}$ can be calculated as given in below equation

$$g_{mb} = \frac{\lambda}{2\sqrt{2\varphi_f + V_{SB}}} g_m = \eta g_m \quad (3)$$

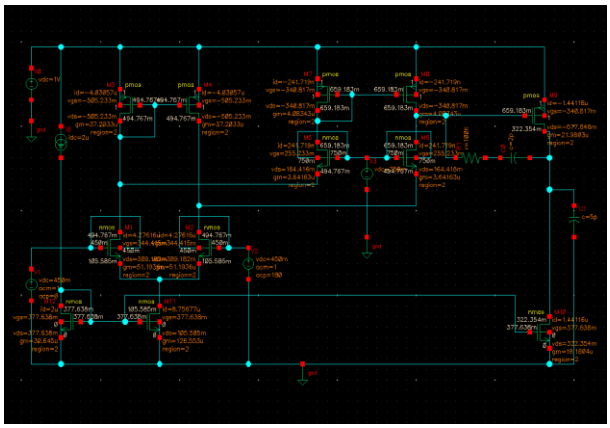

**Fig 4: Schematic Diagram of Two Stage Op-amp**

The forward body-biased MOSFET has been used for designing a low power CMOS op-amp. It operates in two modes. In the "on" mode of the transistor, the source and substrate of MOSFEET is forward biased. The threshold voltage is reduced to help in turning-on of the transistor. In the "off" mode, the transistor is switched to a zero biased source-substrate mode ($V_{SB}$ = 0) in order to increase the threshold voltage. Thus, it helps to reduce the standby leakage current and turns-off the transistor completely.

The DTMOS technique reduces the transistor off-state leakage current and also reduces the threshold voltage during on-state ($V_{BS}$> 0) according to below equation [4].

$$V_{th} = V_{th0} + \lambda\left(\sqrt{|2\varphi_f - V_{BS}|} - \sqrt{|2\varphi_f|}\right) \quad (4)$$

$V_{th}$ is the threshold voltage, $V_{th0}$= threshold voltage for $V_{BS}$=0, λ is the body effect factor that ranges from 0.3 to 0.4, $\varphi_f$ is the Fermi potential with a typical value in the range of 0.3 to 0.4V.

Figure 5 shows the gain and phase margin of the proposed two stage Op-amp.

## 5. SIMULATION RESULTS

The above design op-amp has been simulated in cadence 180 nm standard CMOS technology under 5 pF load. The simulated AC results are shown in Fig. 5, respectively. The Figure show the DC gain of the design is 96.38 dB with unity gain-bandwidth up to 4.077 MHz and it has a phase margin of 71.46°.The total power dissipation of the proposed two stage op-amp is 12.19 µW.

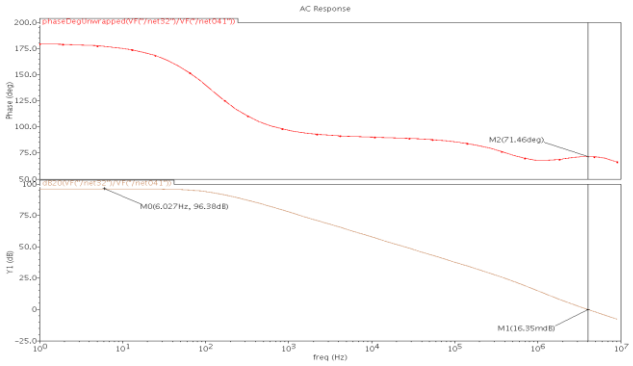


**Fig 5: Gain and Phase margin of Op-amp**

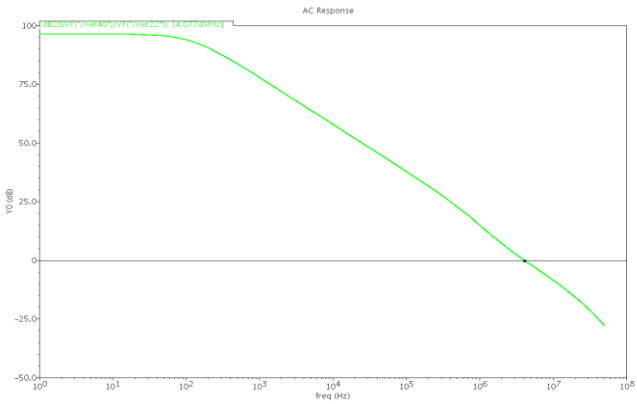


**Fig 6: Unity Gain Bandwidth of Op-amp**

**Table 1: Simulation Results of Two Stage Op-amp**

| PARAMETER | RESULT |
|---|---|
| Gain in dB | 96.38 |
| Phase Margin | 71.46° |
| Unity Gain Bandwidth (UGB) | 4.077 MHz |
| Power Dissipation | 12.19 µW |

# 6. CONCLUSION

The design of a low-power, low-voltage and high performance two stage operational amplifier has been proposed in this paper. The proposed op-amp has been simulated in Cadence Virtuoso 180 nm CMOS technology under 5 pF load. The proposed op-amp is designed for the purpose of low power applications. A DTMOS technique is used for the proposed op-amp to achieve low power. The simulation results show that the desired op-amp has a DC gain of 96.38 dB while achieving a unity gain bandwidth of 4.077 MHz and it has a phase margin of 71.46°. The total power dissipation of the proposed op-amp is 12.19 µW.

Low power applications like ADC and DAC applications can be implemented using with the proposed op-amp.

# 7. ACKNOWLEDGEMENT

The authors would like to thank Dr.I.A.Pasha, HOD, ECE Department, BVRIT. This work was done in CVD (CENTER FOR VLSI DESIGN) Lab and expressing thank to co-ordinator Dr.I.B.K Raju and Asst.Prof Gnaneshwara Chary. They also express their sincere gratitude to the BVRIT, Narsapur, Medak and thanks to parents, friends & colleagues for their contribution in all aspects.

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# 9. AUTHOR'S PROFILE

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