# A High Speed Low Power Adder in Multi Output Domino Logic

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## ABSTRACT
Speed and power is the major constraint in modern digital design so it is required to design the high speed, less number of transistors as a prime consideration. The low power carry look ahead adder using static CMOS transmission gate logic that overcomes the limitation of series connected pass transistors in the carry propagation path. In this approach it is required to find the longest critical paths in the multi-bit adders and then shortening the path to reduce the total critical path delay. The design simulation on microwind layout tool shows the worst-case delay in ns and total power consumption in microwatt range.

## Keywords
Adder, Carry look-ahead (CLA) adders, low power adder, Manchester carry chain, multioutput domino logic.

## 1. INTRODUCTION
The tremendous progress in signal processing technology has given a corresponding development in arithmetic techniques so that high speed operation can be done in low complexity. As the demand for high performance processors grows, there is a continuous need to improve the performance of arithmetic unit and to improve the functionality of algorithms. The most popular high speed adders are look ahead adder, skip adder, conditional sum adder, carry skip adder etc. [1-3]. The high speed adder with CLA (Carry Look Ahead) principal are highly used and can be made dominant as there exist a scope that can improve the carry delay by calculating at each stage in parallel. The Manchester carry chain (MCC) is the most common dynamic (domino) CLA adder architecture with a regular, fast, and simple structure adequate for implementation in VLSI [4,5]. The recursive properties of the carries in MCC have enabled the development of multi output domino gates, which have shown area and speed improvements with respect to single-output gates.

## 2. LITERATURE SURVEY
Various studies and research has been done on this topic and various designs are proposed by the researcher for the efficient designing of Manchester carry chain adders. The efficient implementation of an 8-bit Manchester carry chain (MCC) adder in multi output domino CMOS logic is proposed [6] in which the carries of this adder are computed in parallel by two independent 4-bit carry chains and also showed that the MCC is an efficient and widely accepted design approach to construct CLA adders. It is also proposed that a design technique has been applied for the implementation of 8-bit, 16-bit, 32-bit, and 64-bit adders in multioutput domino logic and the simulation results has been verified. The scholars [7] proposed a new structure for adder base on Metamorphosis of Partial Full Adder logic circuit. in which NAND gate is used instead of AND gate at the end of the G generating path and thus G signal is yielded. MCLA contains two parts; arithmetic adders circuits (Computational units) and carry look-ahead circuits. The arithmetic adder circuits are identical for all adder units, so called Metamorphosis of Partial Full Adder (MPFA).

The logic style used in gates are generally influences the power dissipation, speed, size and the wiring complexity of a circuit. The circuit delay is based on number of transistors in series, inversion levels, transistor sizes which includes channel widths, intra-cell, and inter-cell wiring capacitances [8].

### *2.1 Static Logic Style*
CMOS consists of pull-up network (PUN) and pull-down (PDN) network. It uses the largest number of gates (2N for an N-input gate). So it has large capacitance and delay. In terms of power efficiency, noise margin, voltage scaling and transistor sizing complementary CMOS are better than other MOS devices.

Pseudo-NMOS reduces the number of gates to N + 1 by replacing the pull-up block with single PMOS transistor, such that the capacitance is reduce and the speed is enhanced. The drawbacks of Pseudo-NMOS are lower and asymmetrical noise margin as well as higher standby power consumption.

### *2.2 Carry Look Ahead Adder*
The carry look-ahead adder increase the speed by calculating the carry signals in advance, based on the input signals [5]. The result is a reduced carry propagation time. The logic equation for sum bit I of a binary adder can be written as $S_i$ =8 $X_i$ = xor $Y_i$ xor $C_i$. For a input combination of $X_i$ and $Y_i$, adder stage I is said to be generate a carry if it produces a carry out of `1 independent of the input on $X_0$-$X_{i-1}$ , $Y_0$-$Y_{i-1}$ and $C_0$. For the combination of input $X_i$ and $Y_i$ adder stage I is said to propagate carries if it produces a carry out of `1 in presence of the input combination of $X_0$-$X_{i-1}$, $Y_0$-$Y_{i-1}$ and $C_0$ that cause a carry in of 1.

Corresponding to these definitions the logic equation for a carry generate signal Gi and a carry propagate signal Pi for each stage of carry look ahead adder can be written as.

$G_i = Xi.Yi$

$P_i = X_i + Y_i$

$C_{i+1} = G_i + P_i. C_i$

To eliminate carry ripple Ci can be expand recursively in term of every stage. Such that

$C_1 = G_0 + P_0.C_0$ (1)

$C_2 = G_1 + P_1 .C_1$

$= G_1 + P_1 (G_0 + P_0.C_0)$

$= G_1 + P_1.G_0+P_1.P_0.C_0$ (2)

$C_3 = G_2 + P_2.C_2$

$= G_2 + P_2. (G_1+P_1.G_0+P_1.P_0.C_0)$

$= G_2 + P_2.G_1 + P_2.P_1.G_0 + P_2.P_1.P_0.C_0$ (3)

$C_4 = G_3 + P_3.C_3$

$= G_3 + P_3. (G_2 + P_2.G_1 + P_2.P_1.G_0 + P_2.P_1.P_0.C_0)$

$=G_3 + P_3.G_2 + P_3.P_2.G_1 + P_3.P_2.P_1.G_0 + P_3.P_2.P_1.P_0.C_0$ (4)

In the above equations [9], the logic circuit can be designed by using transmission gate logic will minimize number of transistors, Minimize all internal capacitances, by minimizing the active area of the transistors, and thus minimizing power.

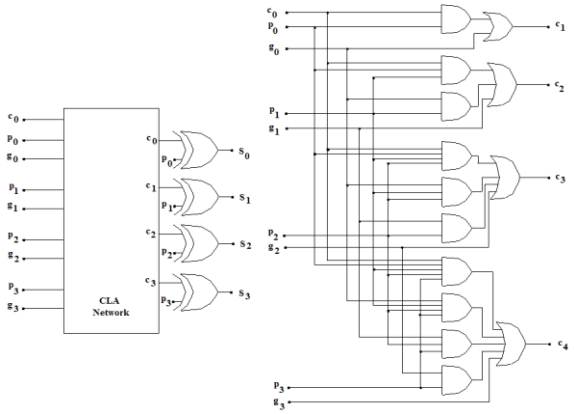


**Fig.1. Carry lookahead adder**

### *2.3 Transmission Gate*

Transmission Gate (TG) has the ability of a high-quality switch with low resistance and capacitance. It is one of the members of the ratio less logic family as the DC characteristics are independent of the input levels. General the sizing is not necessary as capacitance & resistance decrease and increases with respect to the increased gate Width to Length ratio. Transmission Gate is commonly used to implement of XORs and MUXs with the minimum number of transistors.

## 3. RESULT ANALYSIS

In Fig 2, the layout for half adder logic was done in 50nm CMOS technology. The main objectives of the layout are:

- ✓ Reducing all internal capacitances, by reducing the active area of the transistors, thus minimizing power.
- ✓ Reducing total area to minimize manufacturing costs.
- ✓ Maximize area efficiency.
- ✓ Using joining common source/drains on same nets can minimize drain/source junction resistances.
- ✓ Reduce resistance as well as parasitic capacitance especially along critical path, and at high activity nodes.

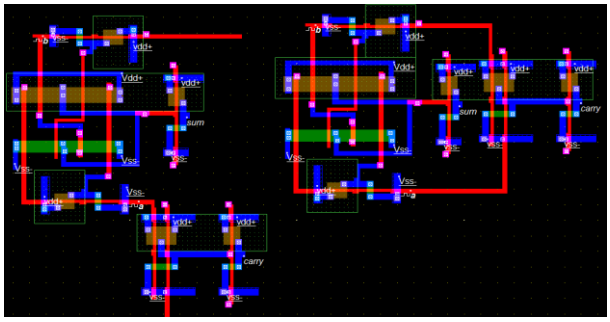

**Fig.2. CMOS layout for half adder logic**

A half adder is used to add two binary digits together, A and B. It produces (S), the sum of A and B, and the corresponding carry out ($C_{out}$). Although by itself, a half adder is not extremely useful, it can be used as a building block for larger adding circuits (FA). One possible implementation is using two AND gates, two inverters, and an OR gate instead of a XOR gate. The timing simulation of half adder logic circuit shown in the fig.3

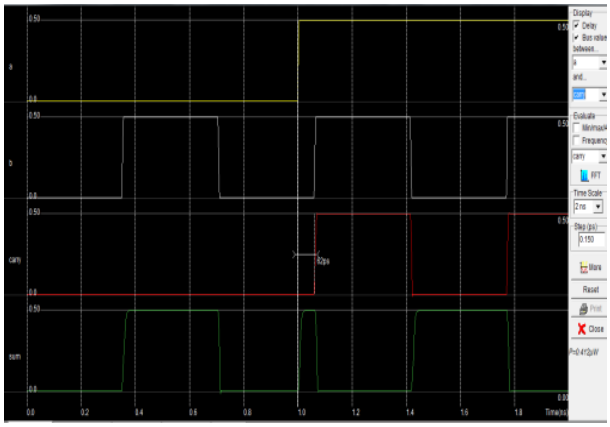

**Fig.3. Timing Simulation of half adder logic**

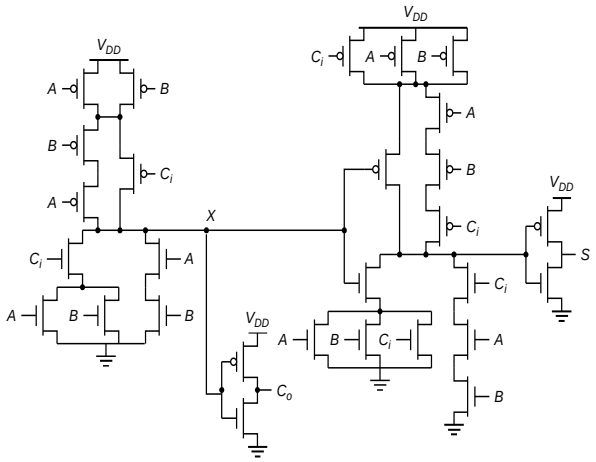


**Fig.4. Static CMOS full adder**

The two Half adder design by using pass transistor logic is use to design full adder logic, the static CMOS full adder circuit shown in fig 4. Where various PMOS and NMOS are in used And the Layout design of 4 bit parallel full adder is shown in fig 5.

The sum of A and B are fed to a second half adder, which then adds it to the carry in C (from a previous addition operation) to generate the final sum S. The carry out, $C_o$, is the result of an OR operation taken from the carry outs of both half adders. There are a variety of adders in the literature both at the gate level and transistor level each giving different performances. The timing simulation diagram for full adder logic circuit shown in Fig 6.

In Fig: 7 the cascade form of four bit full adder stage each of which handles one bit. The carry input to the least significant is normally set to zero and the carry output of each adder is bit connected to the carry input of next most significant bit adder. This kind of operation is slow because the carry require propagating from least significant bit to most significant bit.

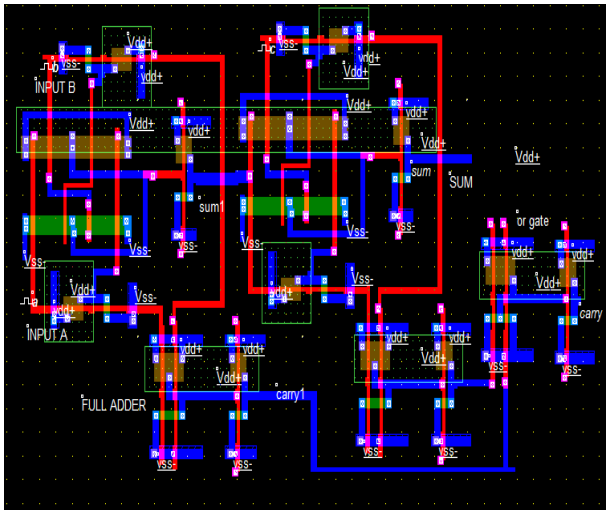


**Fig.5. CMOS layout for full adder**

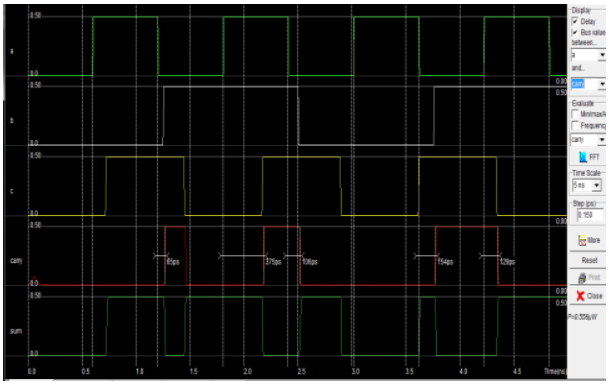

**Fig.6. Timing Simulation of full adder logic**

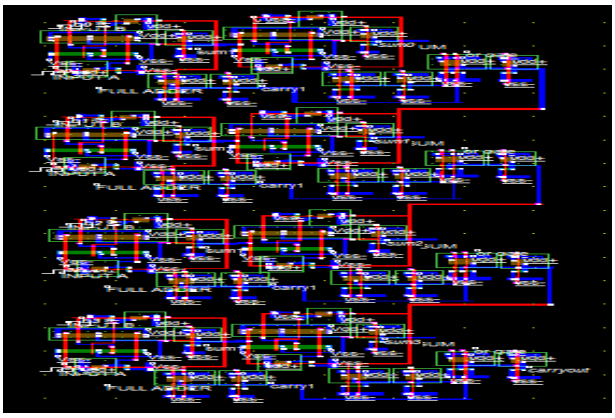

**Fig.7. Four bit Adder consist of 4 parallel full adder logic**

Thus a faster adder can be built by obtaining each sum output $S_i$ with just two level of logic. This can be accomplish by writing an equation for $S_i$ in terms of inputs and $C_0$, multiply, and add logic.

**Table. 1. CMOS logic comparison with different parameter**

| CMOS Logic | No. of Transistor | $I_{ds}$ Current | Power Dissipation | Propagation Delay | Threshold Voltage |
|---|---|---|---|---|---|
| Buffer | 2 NMOS<br>2 PMOS | 0.134mA | 0.24µW | 2 ns | 0.6 V |
| Half adder | 10 NMOS<br>10 PMOS | 0.269mA | 0.412µW | 12ns | 0.4 V |
| Full adder | 23 NMOS<br>23 PMOS | 0.206mA | 0.556µW | 12ns | 0.4 V |
| 4 bit adder | 92 NMOS<br>92 PMOS | 0.256mA | 0.255mW | 24ns | 0.4 V |

## 4. PERFORMANCE ANALYSIS

In Table 1, the performance of designed adder was analyzed and compared with the different parameter. And the comparison of the Required number of transistor, power dissipation, propagation delay and Threshold voltage for buffer, Half adder, full adder and 4 bit adder circuit.

## 5. CONCLUSION

Adder logic circuits are the major part of any processing unit. The CLA is widely used in high performance adder. The result analysis show that the adder layout offered the lowest processing time when implemented with any of the considered technologies circuit size depends on the number of transistors and their sizes and on the complexity of wire. The power dissipation is determined by switching activity and the node capacitance (made up of diffusion, gate associated wire capacitance) which results in turn a function of the same parameter that also controls circuit size. In this paper the CLA architecture designed for half adder, full adder and results are evaluated for number of transistor in used, power dissipation, propagation delay. This work can be extended for designing for parallel adder 4-bit, 16-bit and respectively for improving the speed of adder.

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