Efficient Coded OFDM Modem using FPGA

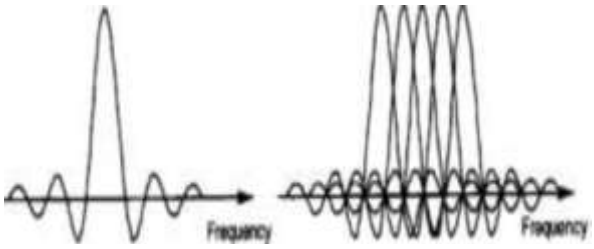
N.Ritishree
Student, M .Tech, DECS
Gudlavalleru Engineering College
Gudlavalleru-521356, Krishna District
Andhra Pradesh, India.

CH.Rambabu
Assistant Professor, Department of ECE
Gudlavalleru Engineering College
Gudlavalleru-521356, Krishna District
Andhra Pradesh, India

ABSTRACT
Due to the increasing demand of transmitting data wirelessly in military, telecommunication industries and in satellite communication engineers had developed different technologies for transmitting the data accurately and also suitable for higher rate transmission which includes the forward error correction (FEC) techniques is referred as the COFDM (coded orthogonal frequency division multiplexing).This paper mainly provides the information related to the transceiver of COFDM and also the corresponding simulation results.

Keywords
OFDM (Orthogonal Frequency Division Multiplexing), BPSK (Binary Phase Shift Keying), COFDM (Coded OFDM), FEC (Forward Error Correction).

1. INTRODUCTION
Coded OFDM is the multicarrier modulation technique based on encoding the digital data. The basic principle involved in Coded OFDM technology is that its splits the higher data rate into several parallel bit stream and these bit stream are modulated by using each subcarrier as shown in figure 1(a), 1(b).



1(a) **1(b)**

Figures 1(a). Spectrum of COFDM sub-channel 1(b).COFDM signal

The main advantage of this technology is that 50% of the band width is saved than the conventional OFDM system as shown in figure 2 and also avoids the problem related to ISI, ICI faced in OFDM.

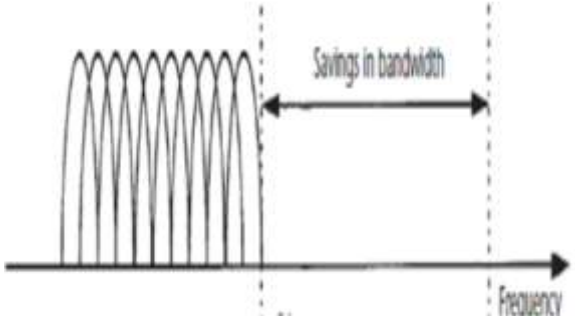


Figure 2. Transmission technique

2. CODED OFDM TRANSCEIVER
The transmitter section of the Coded OFDM mainly consists of the scrambler, convolutional encoder, inter-leaver, BPSK Modulator, IFFT and the receiver part consists of the FFT, demapper, de-interleaver, Viterbi decoder and finally the descrambler as shown in the figure 3.Firstly the input data is generated by using the polynomial x^4+x^3+1 the output is taken from the s4 registers and this is given as the input to the scrambler circuit.

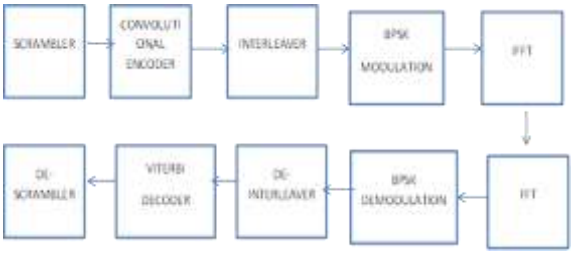


Figure 3.Trans receiver section of Coded OFDM

2.1 Scrambler
While transmitting the data in digital system a large number of 1's and 0's normally occurs by that the timing information cannot be retrieved at the destination. This problem can be eliminated by using the scrambler device at the transmitter side. Scramblers are basically defined based on the linear feedback shift registers and modulo 2 operations, as shown in figure 4 .Themain purpose of scrambler is that to detect the undesirablesequence of bits and inserts the state transitions in a pseudo random manner.

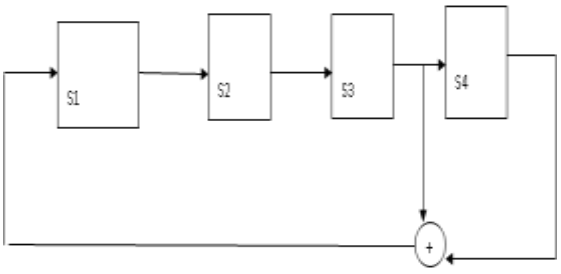


Figure 4.Scrambler

2.2 Convolutional encoder
Convolution codes are commonly specified by the three parameters (n, k, m)

Where n is the number of output bits,

k is the number of input bits ,

m= number of memory registers used.

The efficiency of convolution code is calculated as k/n. From the figure 5 it is clearly noticed that the code rate is ½.M0 represents the input bit and V_1 and V_2 represents the output bits 1 and 2 respectively. The code rate ½ means each input is

coded into 2 output bits. The output stream of encoder is as $V_1V_2V_1V_2V_1V_2$ and so on. The convolutional encoder is an FEC encoder used at transmitter side and at the receiver FEC decoder i.e., Viterbi decoder is used.

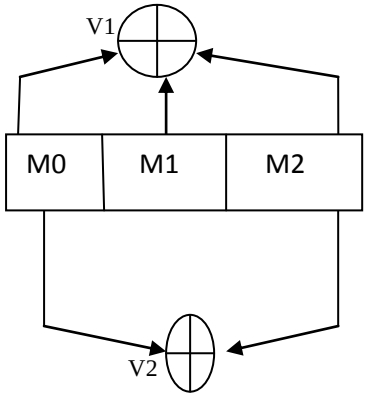


Figure 5.Convolutional encoder

2.3 Interleaver

An interleaver is a device that rearranges the order of sequence of input symbols. The mainuse ofinterleaver is to randomize the location of errors including a signal transmission. Interleaver spreads a burst of errors out so that error correction circuits have better chance of correcting the data. Suppose the input data ={1,0,0,0,1,1,1,1,0,1,0,1,1,0,0,1 }

Total input bits are 16 splitting into MSB and LSB each of 8 bits

=> 10001111 01011001
MSB LSB

again splitting 8 bits to MSB and LSB's each

=> 1000 1111 0101 1001

MSB LSB MSB LSB

Input data{ 1,0,0,0,1,1,1,1,0,1,0,1,1,0,0,1}

ROW0	1	0	0	1
ROW1	1	0	1	0
ROW2	1	1	1	1
ROW3	0	0	0	1

Row permutation {2,0,1,3} is performed

ROW2	1	1	1	1
ROW0	1	0	0	1
ROW1	1	0	1	0
ROW3	0	0	0	1

Outputdata = {1,0,0,0,0,1,0,1,1,0,0,1,1,1,1,1 }
The output of this interleaver is given to the BPSK modulator

2.4 BPSK Modulator

Firstly the cosine and inverse cosine wave of 10 MHZ is generated by using the two different DDS compiler i.e., IP these signals are given as one of the input to the product modulators as shown in figure 6 and the other input to the product modulator is the binary input stream from the interleaver ,the output of the BPSK modulator will be in such a way that when the binary input i.e., if the interleaver input is 1 then cosine wave will be the output otherwise it will be the 180 degree phase of the cosine wave i.e., inverse cosine . Finally the output of the product modulator will be the +coswt or –coswt. This signal is fed to the IFFT (inverse Fourier transform).

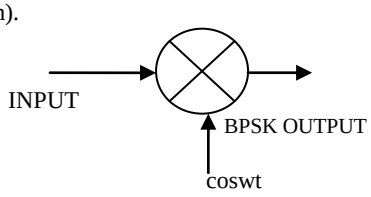


Figure 6.BPSK modulator

2.5 IFFT

The output of the BPSK modulator is given to the real input of the IFFT .The main purpose of IFFT is used to convert the frequency domain to time domain. The output of this IFFT is given as the input to the FFT module and the done signal of the IFFT module is given as the start signal to the FFT module.

2.6 FFT

FFT module is the first block at the receiver side the main purpose of the FFT module is to convert back the time domain signal to frequency domain signal. The output of the FFT is given as the input to the BPSK demodulator.

2.7 BPSK Demodulation

To detect the original binary sequence of 1's and 0's, BPSK demodulation is performed for that two multipliers (using IP CORE) are taken.

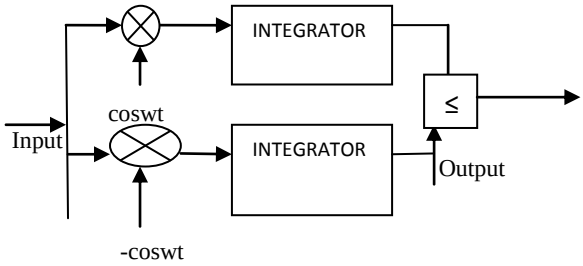


Figure 7.BPSK demodulator

Multiplier has the two input signals each of 16 bits and output signal is of 32bit. One input of the first multiplier is given the cosine wave and the other will be the output of the FFT the resulted output of the first multiplier is given to the integrator .And for the second multiplier one input will be the inverse cosine wave and other input will be the FFT output and the resulted output is given to the another integrator, as shown in figure 7.And this outputs are given to the decision circuit by that the original binary sequence is detected and is same as that of the input to the BPSK modulator.

2.8 Deinterleaver

The deinterleaver operation is same as that of the interleaver operation but the rowpermutations will be different for example if the input data to deinterleaver is as given then the following operations takes place.

Input data={1,0,0,0,0,1,0,1,1,0,0,1,1,1,1,1}

ROW0	1	1	1	1
ROW1	1	0	0	1
ROW2	1	0	1	0
ROW3	0	0	0	1

Row permutation {1, 2, 0,3} is performed

ROW1	1	0	0	1
ROW2	1	0	1	0
ROW0	1	1	1	1
ROW3	0	0	0	1

Output data = {1,0,0,0,1,1,1,1,0,1,0,1,1,0,0,1 }

The output of the deinterleaver is given to the serial to parallel converter because the Viterbi decoder input is the parallel data.

2.9 Viterbi Decoder

The basic structure of Viterbi decoder is in figure 8. It mainly consists of three units namely BMU (Branch metric unit), PMU (Path metric unit), SMU (Survivor management unit)

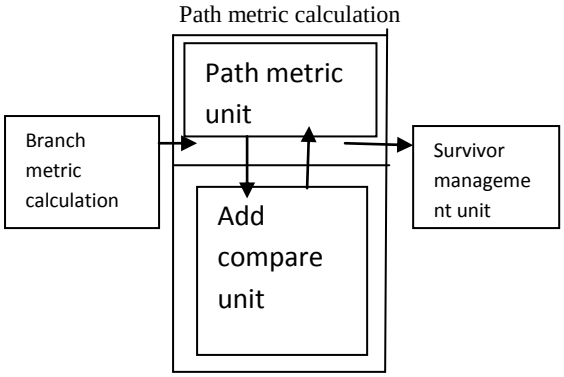


Figure 8.Block diagram of Viterbi decoder

The branch metric unit calculations are based on the hamming distance and previous state path metrics. The path metric is calculated for all the nodes, the minimum of the branch metric is taken as the path metric for each node .the next block present in the figure 8 is the survivor memory unit the main purpose of this unit is to store the states having minimum path metrics. Finally these values are used to get the original data. The output data of the Viterbi decoder is given to the descrambler.

2.10 Descrambler

The operation of the descrambler is same as the input bits generated. The output of the Viterbi decoder is XOR ed with the temp 4 values the resulted output will be same as the bits generated at the input side.

3. SIMULATION RESULTS

COFDMtransceiver system is designed using VHDL and synthesized using Xilinx project navigator XILINX ISE 14.3. Simulation results of COFDM transceiver is shown in simulation figure 9 and hardware results are shown in figure 10 and figure 11 respectively.

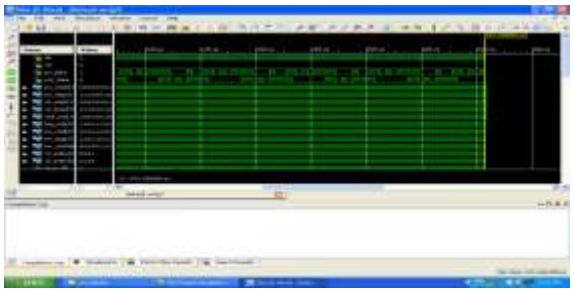


Figure 9.Simulation result of COFDM transceiver.

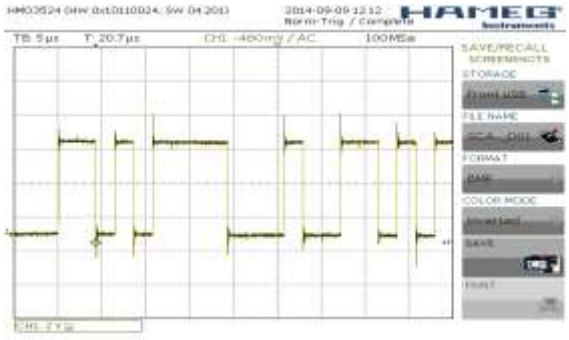


Figure10. Input data generated.

Figure 11.Output data.

4. CONCLUSION

The main focus of this work is to shows the capability of designing and simulating COFDM system which includes the OFDM integrated with FEC technique. Thiswork's main emphasis was on designing and simulation of synthesizable VHDL code of the COFDM transceiver using Xilinx's ISE 14.3 and simulated using the modelsimsimulator.Decice utilization summary of COFDM Trans receiver is shown in table 1 .table 2 shows the total memory used by COFDM Trans receiversystem.

Table1. Device utilization summary of COFDM transceiver

Logic Utilization	Used	Available	Utilization
Number of slice registers	6037	160000	3%
No of slice LUT'S	5571	80000	6%
Number of bonded IOB'S	3	600	0%
No of block RAM/FIFO	5	264	1%
Number of BUFG/BUF GCTRLS	3	32	9%
Number of DSP48E1'S	6	480	1%
Number of fully used LUT-FF pairs	2729	8879	30%

Table 2 Total memory used for COFDM transceiver

Total memory used	188560Kb

The timing analysis of a coded OFDM transceiver is presented as below:

Minimum period : 7.544ns

Maximum frequency : 132.562 MHZ

Minimum arrival time of input before clock: 1.615ns

Maximum arrival time of output after clock: 0.659 ns

Maximum combinations path delay: no path found

5. REFERENCES

[1] S.B.Weinstein and P.M.Ebert, "Data Transmission by Frequency Division Multiplexing Using the Discrete Fourier Transform, "IEEE Transactions on Communication Technology", vol.19, pp.628-634, October 1971.

[2] William Y Zou and Yiyan Wu, "COFDM: an overview". IEEE Transactions on broadcasting vol.41, no.1 pp.1-8, March, 1995.

[3] Simon Haykinw, "Communication Systems", JhonWiley & Sons, Inc., 4th Edition ISB 0-471-17869-1, 2001.

[4] Neil Weste and David J.Skellem,"VLSI for OFDM ", IEEE Magazine on Communications, pp127-131, October, 1998.

[5] S.A. Hanna, "Convolution Interleaving for digital communications", 2nd International Conference on Universal Personal Communications: Gateway to 21st century, vol.1, pp.443-447, 1993.

[6] A.l Intini, "Orthogonal Frequency Division Multiplexing for Wireless Networks", Report Standard IEEE 802.11 a, University of California, Santa Barbara, Dec.2000.

[7] Joaquin Gracia and Rene Cumplido, "On the design of an FPGA – based OFDM modulation ofr IEEE 802.11 a", 2nd International conference on Electrical and electronics Engineering (ICEEE) and x1 conference on Electrical Engineering(CIE),pp 114-117,Sept.2005

[8] Jae-kwon Lee,Jeong_sang Park and Jin-up Kim, "A Convolutional coding scheme for PAR reduction in WLAN-OFDM system", IEEE International Conference on Intelligent Pervasive Computing, pp.98- 100, 2007.

[9] J.S. Reeve and K.Amarasinghe, A FPGA Implementation a parallel Viterbi decoder for a block cyclic and convolutional codes ", IEEE International Conference on Communications, vol.5.pp. 2596-2599, 2004.

[10] William Stalings, Wireless Communications and Networking", Pearson Education, Second Edition, 2002.

[11] Bonghyunk Park, Jaeho Lee, Haewon Jung, Seongsu Park and Hyeong Ho Lee, "Simulation results for FEC in 802.16 OFDM system ", Report by IEEE 802.16 Broadband wireless access working group, IEEE 802 16abc-01/52, Nov.2001.

[12] Robin Hoel, "FEC implementation ", Texas Instruments Design note DN504, 2007.