Energy Efficiency Enhancement for 45nm 1Mb SRAM Array Structures

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ABSTRACT
Energy efficiency is a supreme design concern in many ultralow-power applications. In such applications, high density Static Random-Access Memory (SRAM) plays a significant role. This paper explores and analyzes 1Mb SRAM array structures for energy efficiency improvement by adopting circuit modifications and inclusion of charge sharing circuits. The analysis shows that the array structure optimization and charge accumulator circuits can improve the energy efficiency for the same SRAM bit density and the same supply voltage.

Keywords
Six-transistor (6T) Static Random-Access Memory (SRAM), energy efficiency, minimum energy, SRAM, charge-share

1. INTRODUCTION
Extremely low power SRAM is required in many applications like wearable devices sensor nets and mobile applications. There are various approaches that are adopted to reduce power dissipation in SRAM arrays like power supply voltage scaling and power gating. Lower power supply voltage reduces the dynamic power in quadratic fashion and leakage power in exponential way. But results in reduced noise margin. Forward body biasing methods and multi Vt techniques are used to reduce sub threshold leakage current High dielectric constant gate technology decreases the gate leakage current.

Energy loss is reduced by Adiabatic charging technique. The SRAM working purely on adiabatic charging principles need multiple phase power clocks [1]. Although there is huge saving in energy during writing as well as reading, the design of the SRAM circuit is complex and not same as the design of conventional SRAM. The latency of operation is more.

In energy recovery approach, energy stored in the bit line capacitance that is normally lost to ground during writing is collected and pumped back into the source. Based on the phase of the charging source, pre charging techniques, sense amplifier, the complexity and area of the pumping circuit, there are variants [2, 3, 4 and 5]. The pumping circuit add to the area of the SRAM array.

To overcome the design complexity and latency of complete adiabatic SRAMS, SRAMs that make use of adiabatic charging technique partially have been designed. High resistivity switches are used to vary the power supply voltage slowly in [6].Based on whether adiabatic charging is applied to only power supply line or ground line or bit lines and word lines or only bit lines, there are many types of adiabatic SRAMs [7,8 9 and 10].

Energy stored in the bit lines is recycled by the help of switches to adjacent bit lines in order to save energy in bit line charge- recycle method. This method reduces the swing voltages to a low swing voltage. Based on whether energy recycling is done only during writing cycle or during both writing and reading cycles, there are variants [11 and 12] The circuit uses power switches and complex switching mechanism.

This paper describes the implementation of circuit techniques [13] that effectively use the charge of the non-selected bit lines by charge sharing methods in case of structurally optimized 1Mb SRAM array and the results obtained are compared with the SRAM array without these techniques adopted.

2. DESIGN DESCRIPTION
45nm 1 Mb 6T SRAM array with row and column decoders, bit-line conditioning circuitry, read-write control circuitry, sense amplifiers and clock tree buffers is implemented using hierarchical bit line architecture[Fig.1] in cadence environment. A SRAM cell [Fig.2] is first tested for its working.

Hierarchical bit lines limit the excess bit line swing. The sense amplifiers [Fig.3] in the short local bit lines (LBL) become inactive after the word line falls. The charges from the selected local bit lines pass to the global bit lines by charge sharing method. During writing the charge is pumped back to the global bit lines with the help of write driver circuit as shown in the Fig. 4.

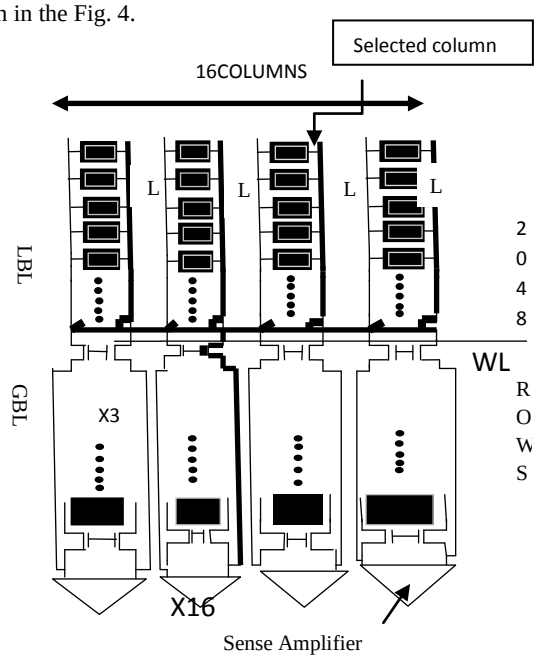

Figure 1 Block diagram of SRAM

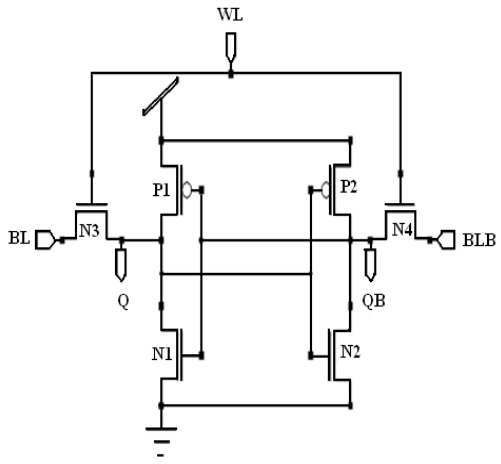

Figure 2: 6t SRAM Cell

The charge (electrons) in the local bit lines which are not selected are allowed to pass to global bit lines (GBL) with the help of switches. Hence the wasted power consumption caused by excess swing of the bit lines is also suppressed. The global bit lines get charges and can support many local lines. The sense amplifiers implemented is differential amplifier type. It is shown in the Fig. 3. The nand type of row decoder addresses the word lines.

The performance of the SRAM cell under noisy conditions is evaluated with the help of SNM [14]. It is found to be 0.34V. The corresponding butterfly curve is plotted as shown in the Fig. 6. The wave forms of the one of the SRAM cells during writing is shown in the Fig. 7 and for a cell in an array of size 1 MB is shown the Fig. 8. The waveforms corresponding to Charge collector circuit is shown in the Fig. 9.The waveforms corresponding to charge sharing circuit is shown in the Fig. 10.

The leakage power of a 6T SRAM cell with power supply voltage equal to 1V is 924.5E-6 watts. The power comparison is carried with the similar SRAM array without energy saving from non selected bit lines. The readings are tabulated in the Table 1.

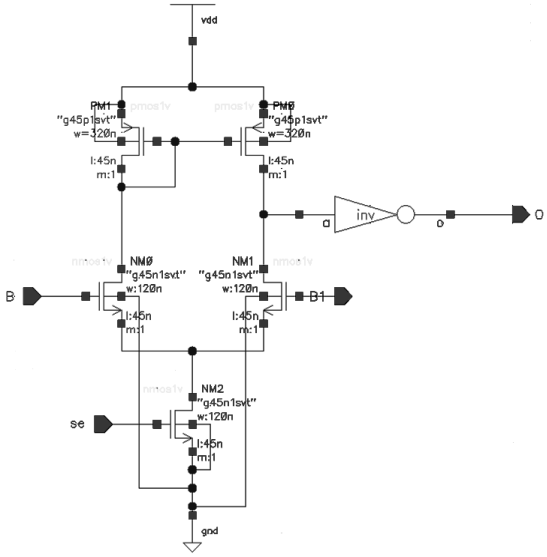

Figure 3 Sense amplifier

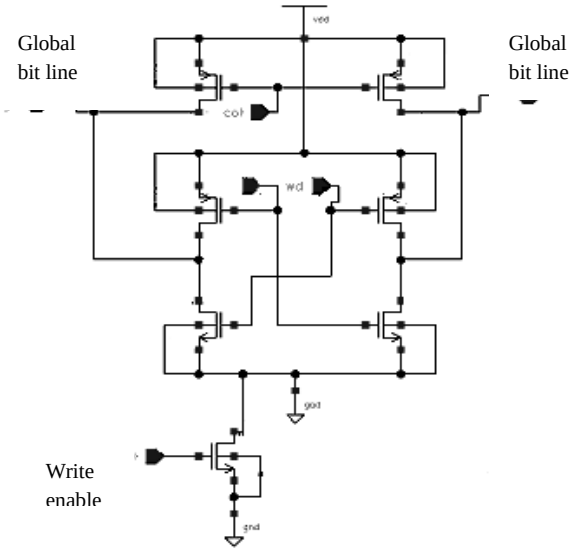

Figure 4 Write Driver circuit (WDC).

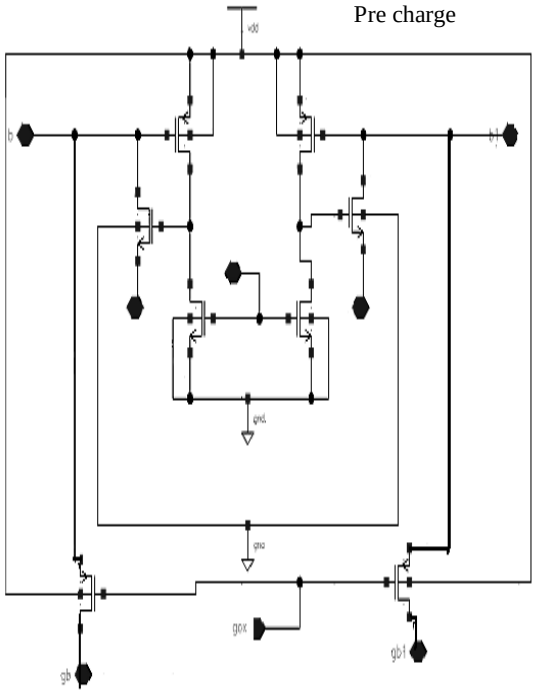

Figure 5 Charge Collector Circuit (CCC).

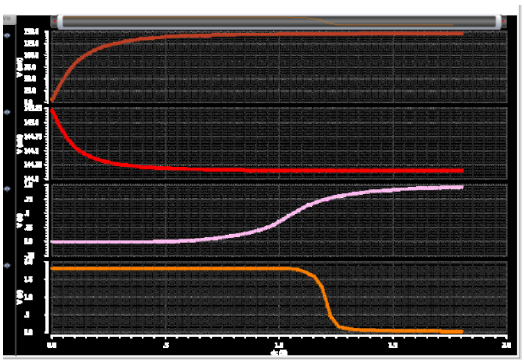

Figure 6 Write operation of a single 6T SRAM cell.

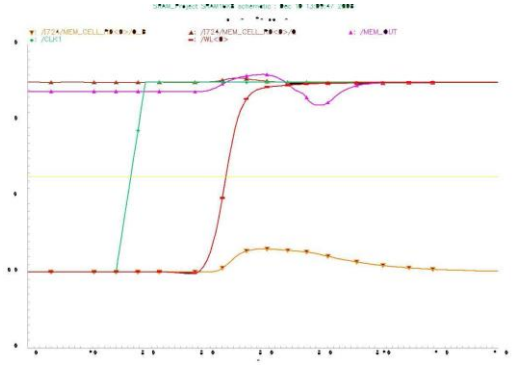

Figure 7 Write and read operation of the 6T SRAM cell in an array of size 1Mb

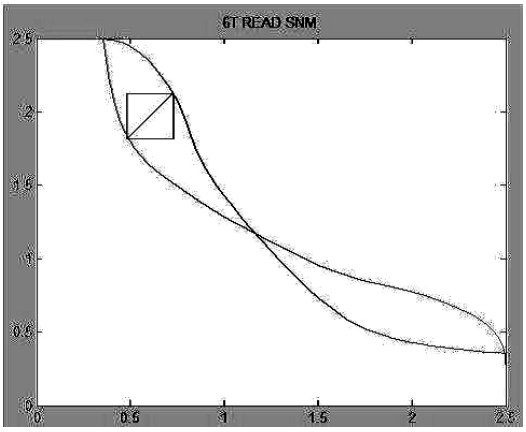

Figure 8: Read static noise margin

The leakage power of a 6T SRAM cell with power supply voltage equal to 1V is 924.5E-6 watts. The power comparison is carried with the similar SRAM array without energy saving technique from non selected bit lines. The readings are tabulated in the Table 1. The power saving is found to be 1Mb 47.7%. at 1V power supply voltage and 63% at 0.58V power supply voltage. The difference is due to reduced dynamic power consumption. The schematic of the entire 1 Mb SRAM Array is shown in the Fig. 12 and the corresponding layout is shown in the Fig. 13 respectively.

The various 6T SRAM cell parameters (per SRAM cell) are found out**.** Diffusion capacitance of access transistors is 1.0512fF. Word line capacitance is 0.076fF. Gate capacitance of access transistors is 1.4832fF. The cell area is 29.33 μm^2 .

Table 1: Power comparisons of SRAM array with and without charge collection.

S No	Circuit Name	Power Dissipation (µw) at 0.7V	Power Dissipation (µW) at 0.59V
1	SRAM array with Charge Collector Circuits.	209.3 µW	51.36 µW
2	SRAM array without Charge Collector Circuits.	400.8 µW	140.3 µW

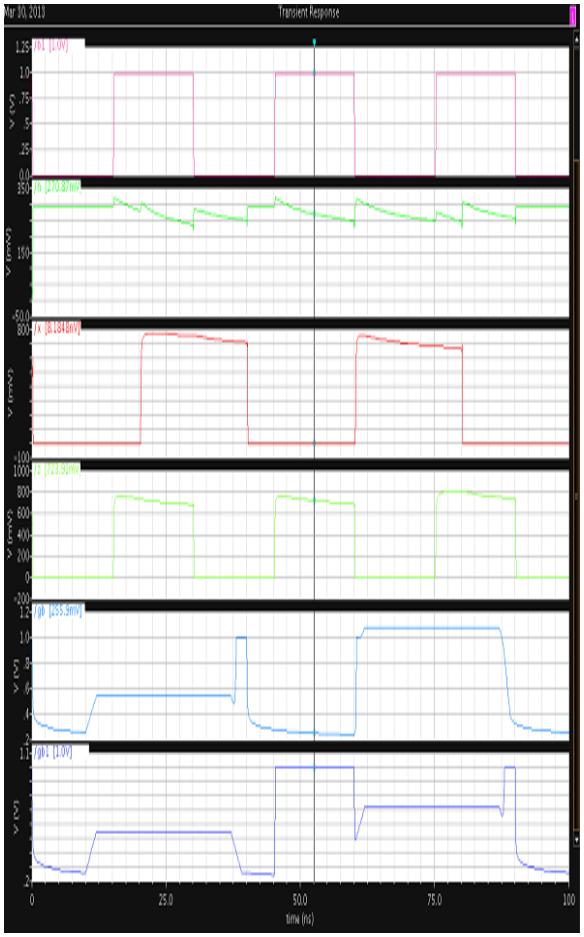

Fig. 9 Wave forms of Charge Collecting Circuit

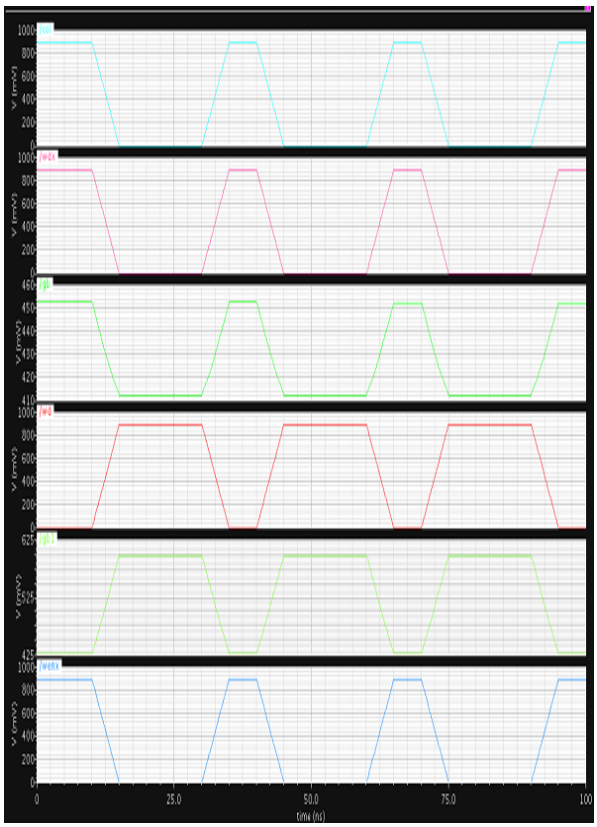

Figure 10 Wave forms of Charge Sharing Write circuit

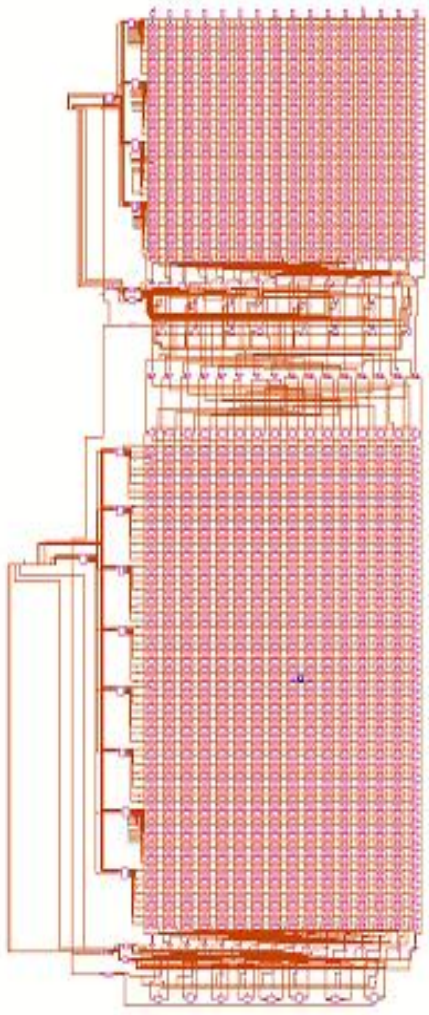

Figure 11 The schematic view of the SRAM array

3. CONCLUSION

The schematic and the layout of 1Mb SRAM Array of have been drawn in Cadence environment using Virtuoso tool. The charge from the unused bit lines are successfully utilized during writing with the help of switching circuits. The power dissipation of the SRAM array with Charge Collector Circuits is compared with that of SRAM array without Charge Collector Circuits .The power saving is found to be 47.7%, when the power supply voltage is 1V. The low power SRAM array can find application in mobile devices and biomedical applications. This type of charge collection can be extended to other memory circuits.

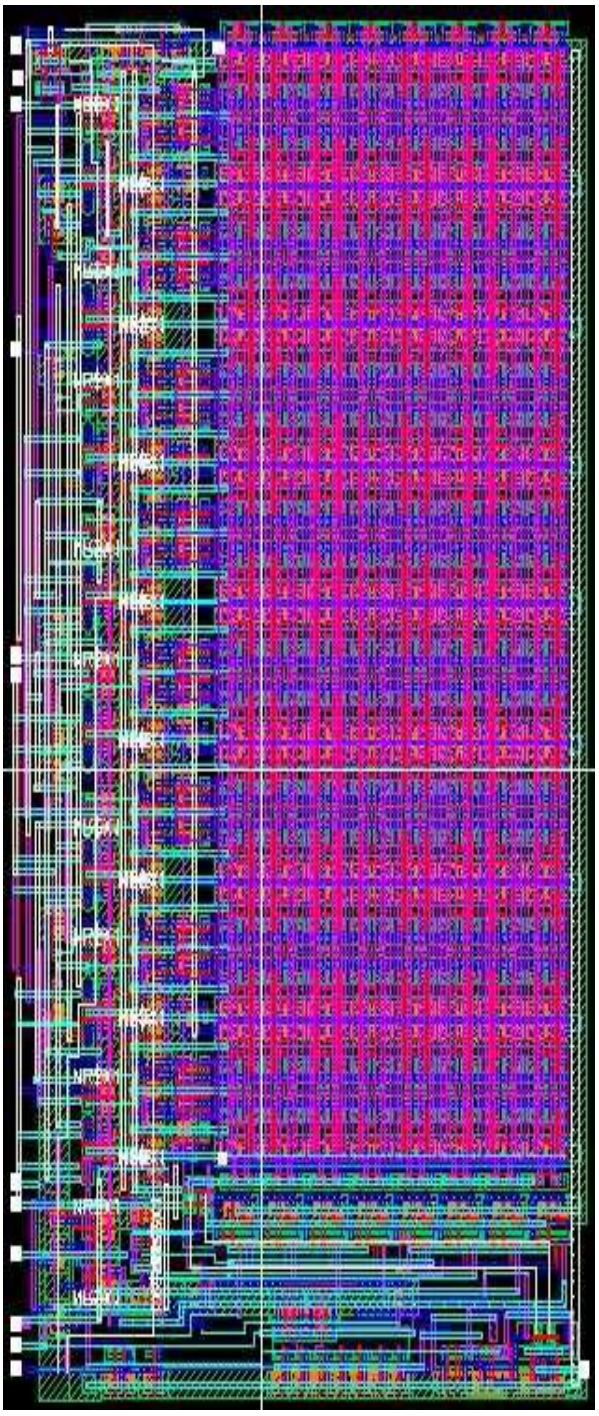

Figure 12 Layout of the design

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