

FPGA Implementation of an Agricultural Management System using Wireless Networks

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ABSTRACT

This paper presents comparison and utilization of resources, delay and minimum period with efficient data transmission using SDI of FPGA. Normally while farming, human labours must visit the fields at time to time and must check the parameters like humidity, temperature, dew point, soil moisture and water level of a well manually and regularly. This traditional method is considered time consuming and needs a lot of work and effort. In the proposed new system, the data related to different parameters will be collected and stored in flash memory. After this process, the data is analyzed, displayed in LCD screen and the data is transmitted by SDI using different coding techniques.

Keywords

Delay, Field Programmable Gate Array (FPGA), LCD display, SDI (Serial Digital Interface).

1. INTRODUCTION

Agriculture in India stood second in worldwide to get farm output. Agriculture plays an important role for the employment to the people. Thus to improve the quality and productivity of the green house human labour are required to visit the green house in regular intervals of time and need to check all the physical variables, which is the traditional method of farming. This is the time taken and it requires more work. To overcome the disadvantages the technology came into existence that which replaces the man with the machinery. Thus automation came into existence.

The modern agricultural management system uses the wireless networks to collect the information from different physical variables. The data which is collected by the wireless networks it is then given to the main server which in turn helps to monitor the system. For every system to be implemented cost must be low and real time monitoring are needed. Thus implementation of the agricultural systems can be done by programmable Logic devices because it allows fast development of device and the design of systems using FPGAs and CPLDs (Complex Programmable Logic Devices).

This modern agricultural management system uses FPGA element which facilitates the system for re-configurability and re-programmability according to different environmental conditions.

2. SYSTEM ARCHITECTURE

When any of the climatic parameters like temperature, humidity, water level, soil moisture and dew point etc. is above the safe value which is used for protecting the crops the values are given as input to the ADC input ports. After this

process, the data is analyzed, displayed in LCD screen and the data is transmitted by using different coding techniques. The following figure 1 shows the system architecture.

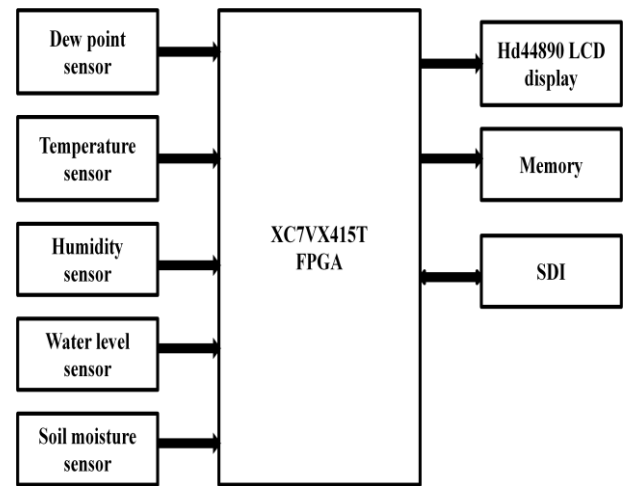


Figure 1 System architecture of agricultural management system

The Xilinx virtex-7 series (XC7VX415T) FPGA is used for implementing the system. The SDI is a standard interface developed by SMPTE and is extensively used in specialized transmit video apparatus. The features of this FPGA are

- It consists of up to 2M logic cells with 6.8 billion transistors at 12.5 GB/s serial transceivers.
- With 6-input LUT technology.
- It has the capability of data buffering with 36Kb RAM with built-in FIFO logic.
- It consists of inbuilt XADC which is 12-bit 1MSPS ADC with thermal and supply sensors as on chip.

Intended for a range of electronics applications to put on view the LCD used in this system is HD44780LCD display. A finite state machine is implemented in FPGA to control and communicate with HD44780.

There are two types of LCD modules one with built-in controller and driver chips and the other with only driver chips. The built-in controllers are again divided into two types, character and graphic LCD modules, in this paper we concerned with character module that is Hitachi Hd44780 with built-in controller.

The Xilinx LogicCORE IP SMPTE SD/HD/3G-SDI core implements for the SDI family of standards. They are SD/HD/3G-SDI standards.

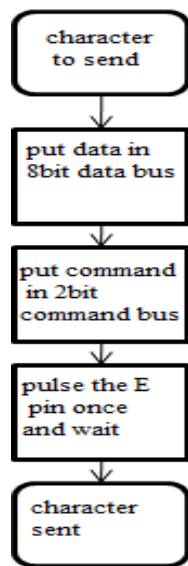
3. IMPLEMENTATION

In this paper, the subsequent commands of the HD44780 were used and they are listed below in Table 1.

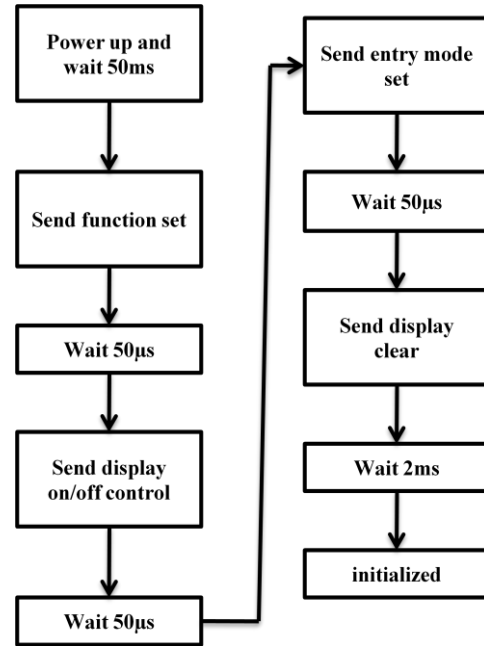
Table: 1- FPGA Implementation instruction set.

Function	Data bits							
	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
Clear display	1	0	0	0	0	0	0	0
Function set	-	-	F	N	DL	1	0	0
Write data	D0	D1	D2	D3	D4	D5	D6	D7
Display on/off	B	C	D	1	0	0	0	0
Entry set	S	I/D	1	0	0	0	0	0

Two modes of data transfer can be done, 4-bit mode and 8-bit mode. In this paper the LCD module is used in 8-bit mode. The following figure 2(A) (B) shows the flowchart of Data transfer.



(A)



(B)

Figure 2(A), (B) flow chart for sending the character and initialization

Following this, a finite state machine is devised to ensure the process flow as above in figure 3.

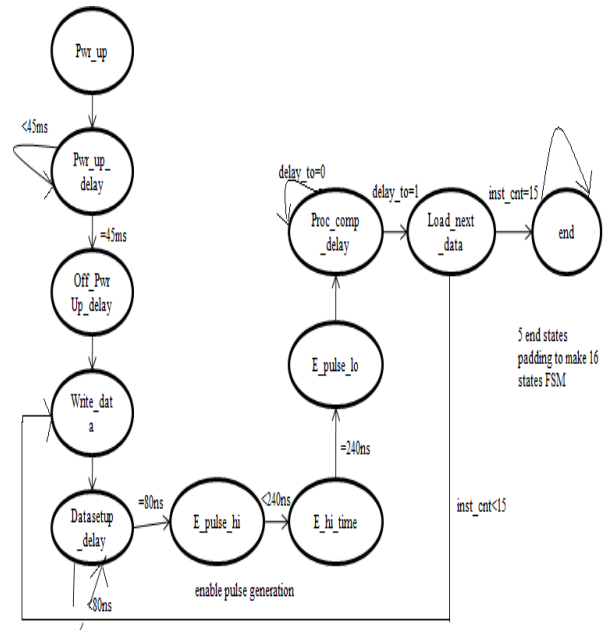


Figure 3 State machine for interfacing FPGA to LCD

The following figure 4 shows the state machine diagram used for designing the full SMPTE SD/HD/3G-SDI core which is used for data transmission.

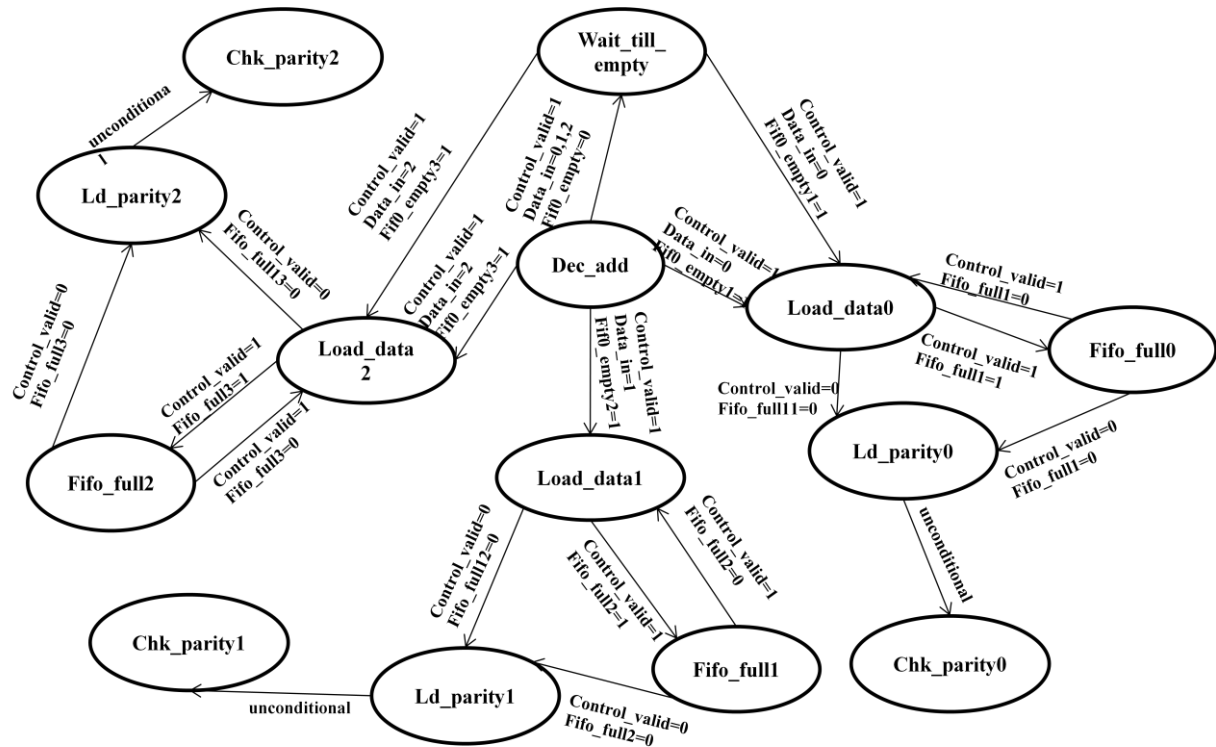


Figure 4 FSM state diagram of SMPTE SD/HD/3G-SDI.

The overall implementation of the SDI module is done using the state diagram shown in fig 4. The decode address state is the default one, it checks whether the valid channel is enable or not, and depending on the mode of operation of the SDI module the operation takes place. Every time during loading the data we must check the FIFO state, if it is full we must wait till it becomes empty and finally we must load the parity bit, at last checking for the parity error by using CRC. Finally, after checking the parity error the state changes to the default state decode address with next clock edge. The following table 2 shows the coding of the state diagram.

Table 2 coding techniques applied to the state diagram

STATE	BINARY CODE	EXCESS-3 CODE	GRAY CODE	ONE-HOT
S0	0000	0000	00011	0000000000000001
S1	0001	0001	00100	0000000000000010
S2	0010	0011	00101	0000000000000100
S3	0011	0010	00110	0000000000001000
S4	0100	0110	00111	0000000000010000
S5	0101	0111	01000	000000001000000
S6	0110	0101	01001	000000010000000
S7	0111	0100	01010	000000100000000

S8	1000	1100	01011	000001000000000
S9	1001	1101	01100	000010000000000
S10	1010	1111	01101	000100000000000
S11	1011	1110	01110	001000000000000
S12	1100	1010	01111	010000000000000
S13	1101	1011	10000	100000000000000

The states of the state machine can be coded by using different coding techniques. The binary encoding is the simplest one which is a state number binary count in sequence. While in one hot one bit is 'high' for any state in the state register and requires a slight logic, hence widely used in FPGA's. Speed is the main parameter for every system or device that is designed and that is indicated by minimum period, here based on the analysis binary encoding is faster. Even though it may be estimated that one-hot would be the fastest this would happen in the one-hot optimized technique. The gray method of encoding is similar in the performance to binary.

4. RESULTS

Open ISE navigator window and open the code generated files and simulate the code. Automatically it generates the RTL and Technology schematic diagrams, synthesis reports and timing diagrams. The following figure 5 shows the FPGA to LCD interfacing TOP module schematic.

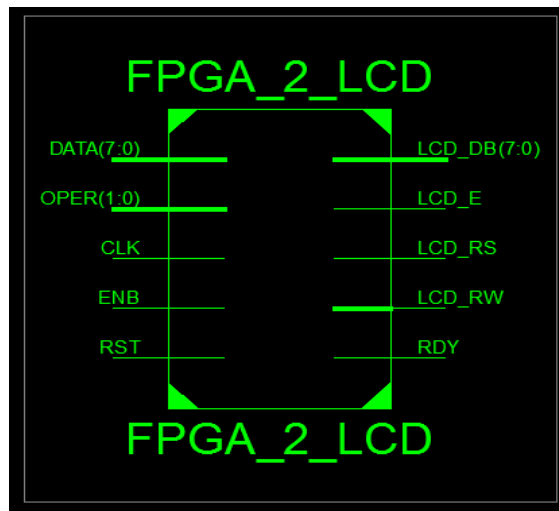


Figure 5 TOP module of FPGA to LCD interfacing

Now after checking the synthesis report, in implementation and simulation is the next step in which behavioural check syntax is done and after successful completion of this

process, we must simulate the behavioural model thus the following simulation results are generated for LCD display as in the figure 6.

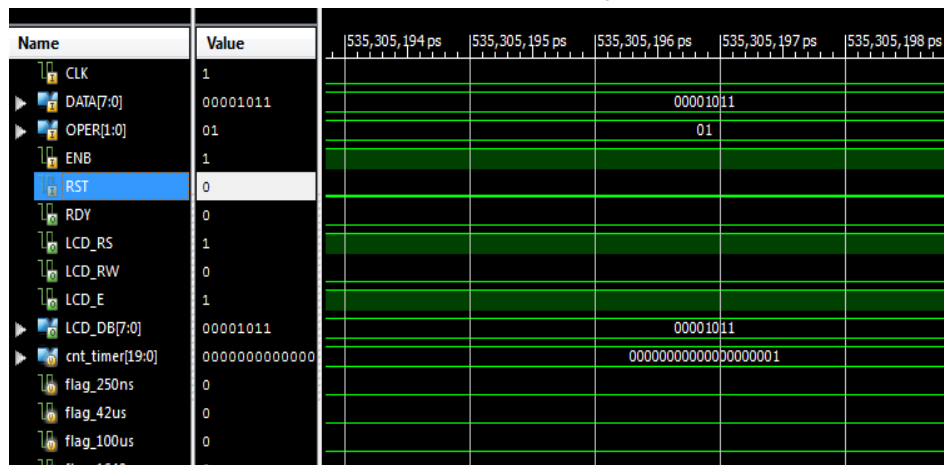


Figure 6 Simulation result of LCD display Module

Here the command given is the 01 which is used for display on/off control. Register select=0. The LCD_DB[7:0]=00001111 which indicates the LSB four 1's as displaying, blinking and controlling.

Similarly, for the SDI module the synthesis and simulation results are as follows in figure 7 and figure 8.

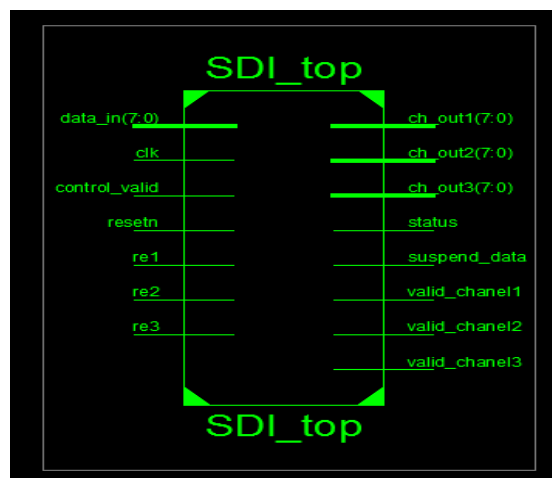


Figure 7 Synthesis Results of SDI top module

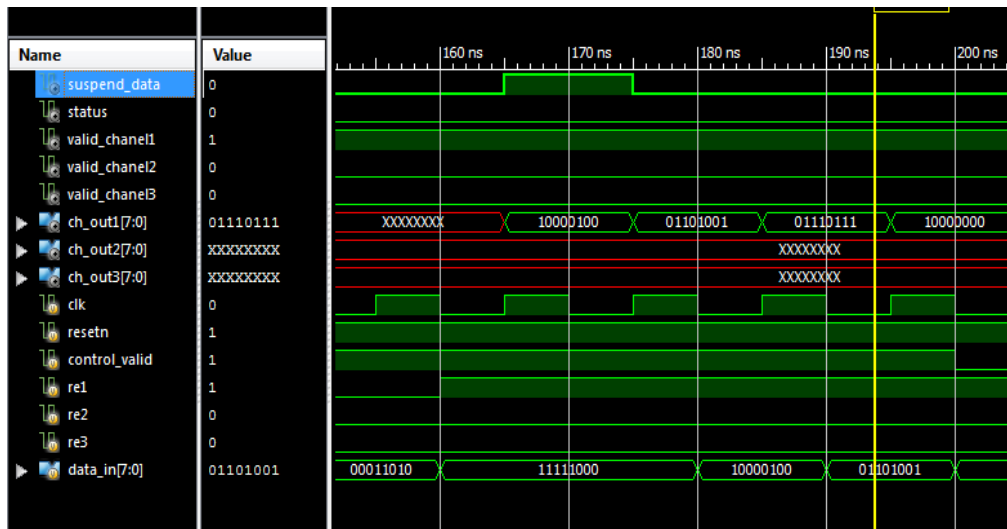


Figure 8 simulation result of SDI module

The above fig 8 shows the simulation result of SDI module with re1 as enable and valid channel1 as enable with data in is present at the output of the channel1. The following table 3 shows the four coding techniques utilization summary, delay and minimum period.

Table 3 Comparison of utilization summary for different coding techniques along with delay and minimum period

Coding techniques	No of Slice registers	No of Slice LUT's	No of LUT-FF's	Delay (ns)	Minimum period (ns)
Binary	112	224	100	0.974	2.094
Excess-3	119	227	104	1.394	2.265
One-hot	132	248	113	1.501	2.712
Gray code	112	219	100	1.314	2.094

5. CONCLUSION

It is clear that the one-hot and excess-3 requires more number of utilization resources and has more delay due to more number of bits used per state. Now among other two coding techniques, gray code requires more complex hardware when compared to the binary during the state transition hence delay is more for gray code compared to binary. Thus Binary gives the best speed and with less number of utilization resources.

Thus the data is analysed, displayed using HD44890 LCD screen and the data is transmitted using SDI using different

coding techniques like Binary, Gray code, Excess-3 code and One hot encoding and the utilization of devices are shown in table of comparison along with the delay and minimum period of different coding techniques.

6. FURUTE SCOPE

It is known that SDI which is a family of society of motion picture and television engineers (SMPTE) is widely used in professional broadcast video equipment. Thus by using the SDI module not only data can be transmitted but also video can also be transmitted.

7. REFERENCES

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