A Review of Noise Susceptible Transistor in Dynamic Logic Circuits

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ABSTRACT
Noise is becoming a major concern in digital systems due to the insistent scaling development in devices and interconnections. In this paper disputes related to process variations, timing, noise suppression, and power are investigated here for performance optimization. A weak PMOS keeper logic is used to improve the scaling of dynamic gates. The keeper has an overhead of one field-effect transistor per gate plus a portion of a shared current mirror. This keeper circuit technique is proposed in this paper for simultaneous power reduction and speed enhancement of domino integrated circuits. The threshold voltage of the keeper logic is modified during circuit operation to decrease the contention current without giving up noise immunity. The charge sharing can also be eliminated by pre-charging internal node.

Keywords
Dynamic gates, Current Mirror,P-MOS keeper logic.

1. INTRODUCTION
Electrical noise is one of the most important reliability concerns in Nano scale integrated circuits. Improvement of noise suppression techniques is required to guarantee reliable operation of integrated circuits. A variety of noise mitigation techniques are presented and explored in the following chapters of this paper for low power MTCMOS circuits [1]. Noise in digital circuits can be divided into three categories: power and ground distribution network related noise, signal interconnect related noise, and device related noise. Power and ground distribution network noise is formed due to the growing demand of average and instantaneous currents by the switching circuits. The demand of average currents generates the DC component of the power and ground distribution network noise. Also due to the due to the capacitive and/or inductive coupling from neighboring wires the voltage disturbance induced on a signal interconnects cause crosstalk noise.

2. RELATED WORK
i Hailong Jiao and VolkanKursun proposed leakage power reduction techniques of multithreshold MTCMOS circuits. During the ideal state of transistor, high currents flow through the sleep transistors. Considerable voltage fluctuations causes on the power and ground distribution networks. Influences of within- die and die-to-die parameter variations on the reactivation noise suppression , timing, and energy consumption of sleep signal slew rate modulated MTCMOS circuits are evaluated with a process imperfections aware robustness metric [1].

ii ManishaPattanaik, Muddala V. D. L. Varaprasad and Fazal Rahim Khan proposed the reduce peak of ground bounce noise low leakage 1bit full adder cells for mobile applications. They design optimal sleep transistor size which reduce the leakage power and ground bounce noise 1bit full adder cells. Their proposed technique design in 90nm technology and operated with 1.2V supply voltage, reduces leakage power by 82 to 84 in comparison to the conventional adder cell [2].

iii Gaetano Palumbo,MelitaPennisiand Massimo Alioto propose reduce delay variations in domino logic gates by modified keeper to reduce the loop gain while keeping the same silicon area, noise margin, and nominal performance [3].

iv Li Ding and PinakiMazumder explain the noise immune

v feedback keepers to prevent the dynamicnode from floating; internal nodes were pre-charged to eliminatethe charge sharing problem; and weak complementary p-networkis constructed to improve the noise tolerance to the levelof skewed static CMOS logic gates and the effectivenoise-tolerant design techniques that incur little over heading silicon area, circuit speed and power consumption are highlydemanded [6].

3. SOURCE OF NOISES IN DIGITAL INTEGRATED CIRCUIT
Noise causes in dynamic logic circuits are classified into two basic types: i) gate internal noises, including charge sharing noise, leakage noise, and so on, and ii) external noises, including input noise, power and ground noise, and substrate noise.
1) Charge sharing noise reduces the voltage level is caused by charge redistribution among the dynamic node and the internal nodes of the MOSFET network.
2) At the evaluation period of dynamic logic, sub-threshold leakage current causes the significant source of noise in wide dynamic logic gates design.
3)Due to the coupling effects a crosstalk among adjacent signal wires at the inputs of a logic gate creates input noise
4) Power and ground noise is mainly caused due to the parasitic resistance and inductance at the power and ground networks and at the chip package.
5) Substrate noise can affect the signal integrity of a logic gate through substrate coupling.
6)Flicker noise creates due to the random motion of electrons in a conductor introduces fluctuation in the voltage measure across the conductor even if the average current is zero.
7) The interface between the gate oxide and the silicon substrate in a MOSFET at the interface forms dangling bonds, giving rise to extra energy state. As charge carrier moves at the interface, some are randomly trapped and later release by such energy states, introducing "flicker noise" in the drain current.

3.1 Dynamic CMOS Logic
Dynamic logic will significantly reduce the number of transistors in design. It works on pre-charge of output capacitance and evaluate the output level depends on the input apply. Both of these operations are programmed by a single clock signal, which drives one NMOS connected to ground and

one PMOS transistor connected to Vdd in each dynamic stage Fig 1shows the CMOS dynamic logic NAND gate implemented using dynamic logic [4]. The pre-charge phase is occur when clk=0. The path to the VSS supply is closed via the NMOS during clk=1 (evaluatephase). The pull-up time is improved by P-MOSFET, but the pull-down time is increased due to the ground switch (NMOS) [4].

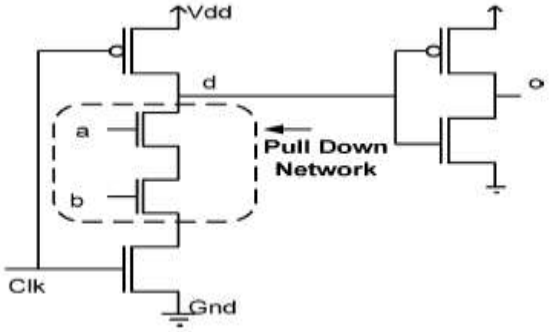

Fig.1: CMOS dynamic logic NAND gate

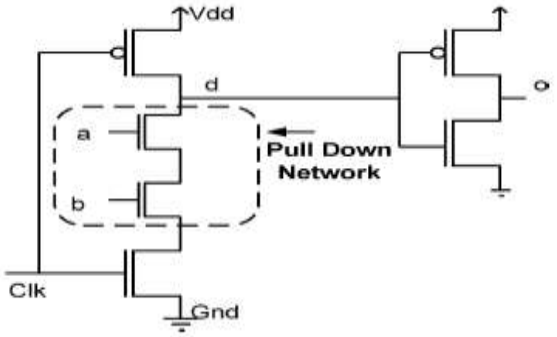

Fig.2: Timing analysis of CMOS dynamic logic gate

In dynamic logic structure the inputs can just change at the pre-charge phase and must be stable at the evaluate phase of the cycle. If this condition is not meet, charge redistribution effects can corrupt the output node voltage. At the end of the evaluation phase output will be erroneous.

3.2 Domino CMOS logic

The problem arises in cascaded dynamic logic is evade by adding a static CMOS inverter into each dynamic logic gate as shown in Fig 3 [3] .The incorporation of the inverter allows design to operate a number of such structure in cascade. At pre-charge phase clk=0 cause the output of first stage of the dynamic gate is pre-charge to high and the output inverter is low [5].

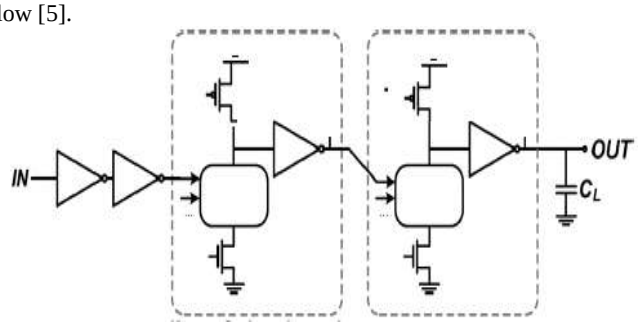

Fig.3: Domino logic

This low output of inverter keeps output of second stage at logic high. At the evaluation phase, there may cause the output node of the dynamic CMOS stage (first stage) is either discharge to a low level through the PDN(1 to 0 transitions) or it charged to high. As a consequence, output voltage of an inverter can also make at most one transition during the evaluation period while going 0 to 1. While cascading dynamic logic in which evaluation of each stage ripples the next succeeding stage for evaluation which is related as the sequence of domino's falling one after another. This structure hence called domino CMOS logic [3].

4. NOISE CONSIDERATIONS IN DYNAMIC DESIGN

4.1Charge leakage

The operation of the dynamic logic depends on the principles of dynamically storing a charge on the output node capacitor. Due to leakage currents, this charge gradually leaks away, resulting eventually in malfunctioning of the gate [6].

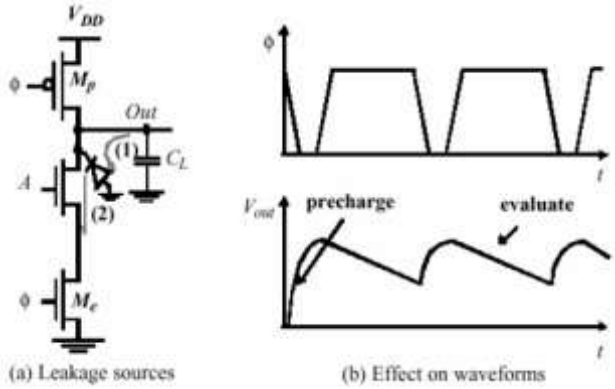

Fig .4: Charge leakage

4.2 Charge sharing

During the pre-charge phase, the output node is pre-charged to VDD. Capacitors Ca and Cb represent the parasitic capacitances of the internal nodes of the circuit. Assume now that during pre-charge all inputs are set to 0 and the capacitance Cawill discharge.During evaluation periodassume that input B remains at 0, while input A makes atransitionfrom 0 to 1. While turning transistor Ma on, the charge stored on capacitor Ciswill redistribute over C_L and Ca. with a drop in the output voltage thatcannot be regained due to the dynamic nature of the circuit. It can be eliminated only by pre-charging internal node [6].

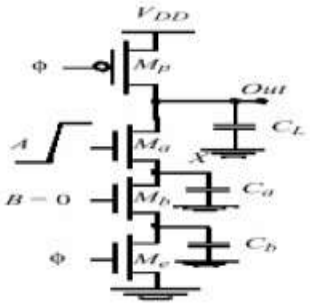

Fig.5: Charge sharing

4.3 Keeper MOSFET

To increase the noise tolerance of dynamic CMOS logic gates is to employ a weak transistor, known as keeper, at the dynamic node as shown in Fig. . The keeper transistor supplies a small amount of current from the power-supply network to the dynamic node of a gate so that the charge stored in the dynamic node is maintained. In the original domino dynamic logic work, the gate of the PMOS keeper is tied to the ground, Therefore, the keeper is always on [6].

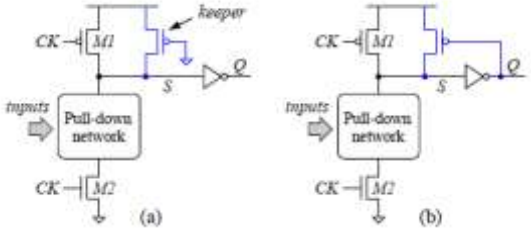

Fig.6: Improving noise immunity of dynamic logic gates using keeper. (a) Weak always-on keeper (b) Feedback keeper

Feedback keepers, illustrated in Fig. (b), are more widely used because they eliminate the potential DC power consumption problem using the always-on keeper in the evaluation phase of domino gates [6].

5. CONCLUSION

In this paper we discussed about Sources of Noises in Digital Integrated Circuits. Dynamic logic circuits have less immune to noise. The noise causes due to charge sharing at nodes that can be eliminating by pre-charging internal node. This improves noise tolerance against both internal and an external noise is to increase the source voltage of the transistors in the pull-down network. Also the noise tolerances of dynamic CMOS circuit are increased by incorporating the feedback keeper circuits.

6. REFERENCES

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