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A Novel Design of Half and Full Adder using Basic QCA Gates

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ABSTRACT

This paper presents the novel design of half adder and full adder using reduced number of QCA gates.This design utilizes the unique characteristics of QCA to design a half and a full adder.The basic component of QCA is a cell consisting of two electrons and four logically interacting quantum dots.Simulation indicates a fast,efficient and very attractive performance(i.e.complexity,area and delay)

Keywords:

QCA, half adder,full adder

1. INTRODUCTION

VLSI technology,although has made remarkable progress in the past,this progress may be slowed down in future.Among the chief technological limitations for this slowdown are the interconnect problem and power dissipation. As more and more devices are packed into the same area, the heat generated can no longer dissipate and may result in damage to the chip. QCA[2, 3, 6, 10, 17] provides a good alternative to the silicon technology.QCA based circuits have the advantage of high speed, high integrity and low power consumption. Also Q QCA circuits have the advantage of high parallel processing.
Adders are basic circuits in digital logic.Conventional transistor based adder circuit requires many wires.Due to the delay caused by these wires,most of the previous adder circuits are limited in speed.Moreover,such complex circuits are difficult to implement in QCA [1, 4, 5, 7, 8, 9, 10, 11, 12, 16, 17, 18, 19, 20].Adder performance can be enhanced by minimizing the carry propagation delay.Many designs of adder using QCA have already been proposed[13, 14, 15]. This paper presents a design of adders that is optimized for implementation in QCA.

2. QCA DESIGN SCHEME

The quantum dot cellular automata use a binary representation of information, by replacing the current switch with a cell having a bistable charge configuration. One configuration of charge represents a binary ”1”, the other a ”0”. The field from the charge configuration of one cell alters the charge configuration of the next cell. Remarkably, this basic device-device interaction is sufficient to support general purpose computing with very low power dissipation.

2.1 QCA Cells

A QCA cell[3] possesses an electric quadrupole which has two stable orientations as shown in Fig.1 . These two orientations are used to represent the two binary digits, ”1” and ”0”.A QCA cell comprise of four quantum-dots arranged in a square pattern. The cells contain two mobile electrons(or holes) which repel each other as a result of their mutual Coulombic interaction and in the ground state tend to occupy the diagonal sites of the cell. These lead to two polarizations of a QCA cell, denoted as P=+1 and P=-1 respectively. Thus logic 0 and logic 1 are encoded in polarization P=+1 and P=-1 respectively. When a second cell is placed near the first cell, the coulomb interaction between the cells removes the degeneracy and determines the ground state of the first cell.

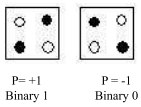

Fig. 1. Basic QCA cell and Two Possible Polarizations

2.2 QCA Wires

In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells .There are four global clocks with phase difference of 90 degree which controls the QCA circuits.During each clock cycle, half of the wire is active for signal propagation, while the other half is unpolarized. During the next clock cycle, half of the previous active clock zone is deactivated and the remaining active zone cells trigger the newly

activated cells to be polarized. Thus, signals propagate from one clock zone to the next.

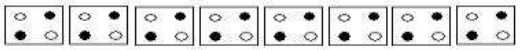

Fig. 2. QCA wire

2.3 QCA Gates

Majority voter gate and inverter acts as the basic gates in QCA. The governing equation of majority voter gate is

$$M(A,B,C) = AB + BC + AC \quad (1)$$

Two input AND and OR gate can be implemented from three input majority voter gate by making one input constant.

$$\begin{aligned} M(A,B,1) &= A + B \\ M(A,B,0) &= AB \end{aligned} \quad (2)$$

Fig 3 and Fig 4 shows the gate symbols and their layout.

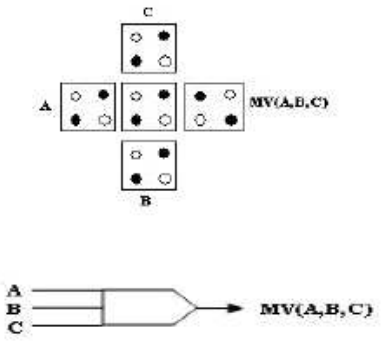

Fig. 3. QCA Majority Voter Gate

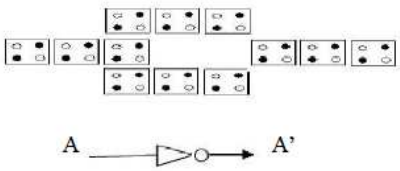

Fig. 4. QCA Inverter Gate

3. ADDER CIRCUITS

A half adder performs the addition of two boolean variables and gives two output,one is the sum and the other is the carry.Let A ad B be two input variables.Then the sum and carry is respectively given by

$$\begin{aligned} S &= A \oplus B \\ C &= AB \end{aligned} \quad (3)$$

The truth table of half adder is given in table1.

Table 1. Truth table of Half Adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The circuit diagram of half adder is given below.

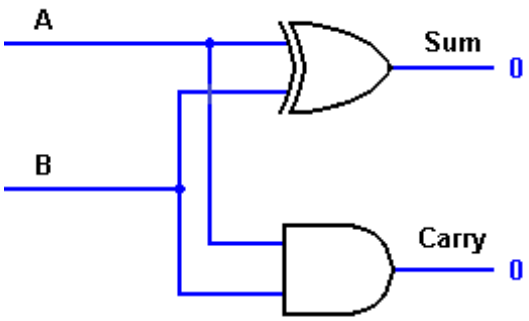

Fig. 5. Circuit Diagram of Half adder

The full adder performs the addition of three boolean variables and produces two outputs,a sum and a carry.Let A,B and C are three variables.Then the sum and carry is respectively given by

$$\begin{aligned} S &= A \oplus B \oplus C \\ C &= AB + BC + CA \end{aligned} \quad (4)$$

The truth table of full adder is given in table2.

Table 2. Truth table of Full Adder

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The circuit diagram of full-adder is given below.

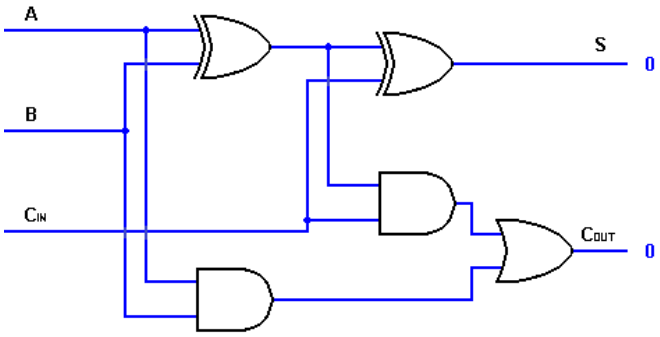

Fig. 6. Circuit Diagram of full adder

3.1 Proposed method

In order to realize half adder using QCA,we need three majority gate and an inverter.The two input A and B are fed simultaneously into two majority gates 1 and 2 ,one of which acts as an AND gate and another acts as an OR gate.The output of the AND gate is fed into an inverter and finally,the outputs of majority gate 1 and that of the inverter are fed into another majority gate 3.The output of majority gate 3 is the sum and that of majority gate 2 is the carry.The circuit diagram and the layout is given in figure 7 and 8.

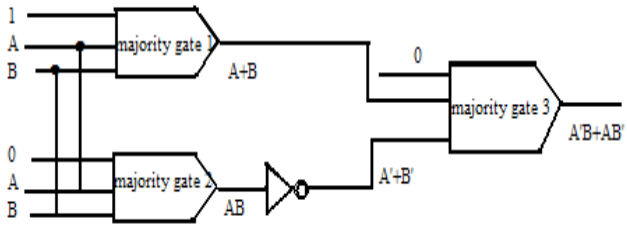

Fig. 7. Circuit Diagram Half adder using QCA gates

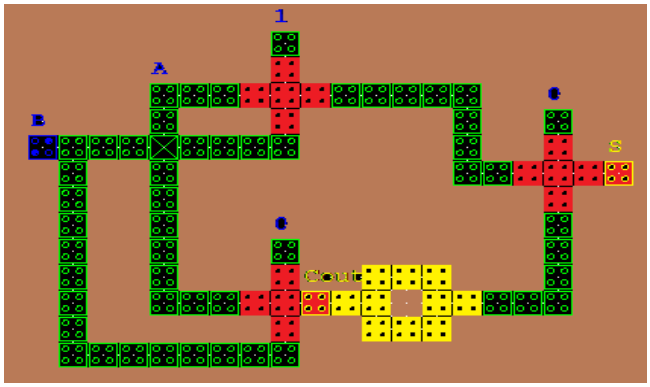

Fig. 8. Layout of Half adder using QCA gates

If one observe carefully,one will see that the half adder circuit is nothing but a XOR gate which is realized using QCA basic gates. Full adder can be implemented using only two majority gate and an inverter.Majority gate 1 is a five input majority gate,whose three inputs are A,B,C and the other two inputs are shorted to the output of the inverter.The output of majority gate 1 is the sum.Majority gate 2 is a three input majority gate.A,B,C acts as the inputs to majority gate 2 and the output is the carry.The output of majority gate 2 is also fed into an inverter whose output goes into majority gate 1 as mentioned above.The circuit diagram and layout is shown in figure 9 and 10.

It is to be noted that in figure 8 and 10,the red portion indicates the QCA majority gates,the yellow portion indicates the inverters and the rest are the QCA wires.The cross symbol indicates the crossover of two wires.

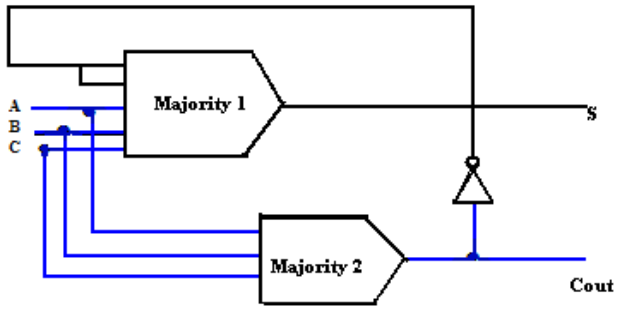

Fig. 9. Circuit Diagram of full adder using QCA gates

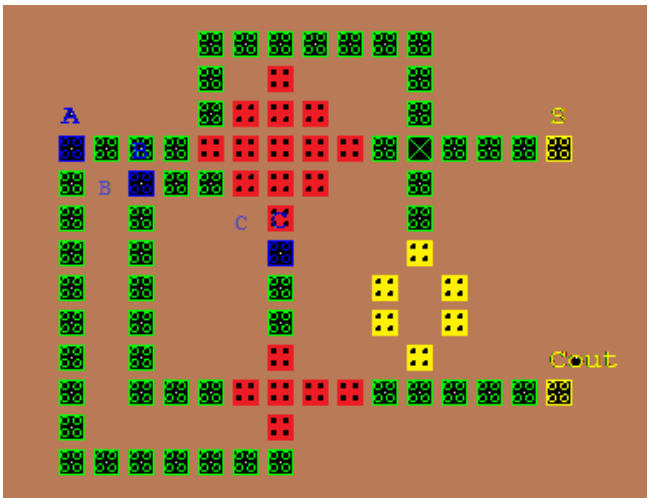

Fig. 10. Layout of full adder using QCA gates

4. RESULT ANALYSIS

The number of gates required to realize half and full adder is minimal.If we compare our results with [1],it will be seen that our proposed method reduces the number of gates required compared to [1].Consequently,the area,complexity and delay of the circuits will also reduce and hence,the performance of the circuit will increase.The simulation result of half adder and full adder obtained by simulation the layouts in QCADesigner is given in figure 11 and 12.

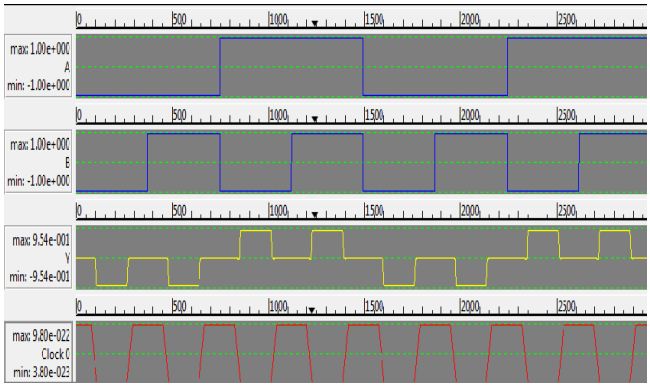

Fig. 11. Simulation result of Half Adder

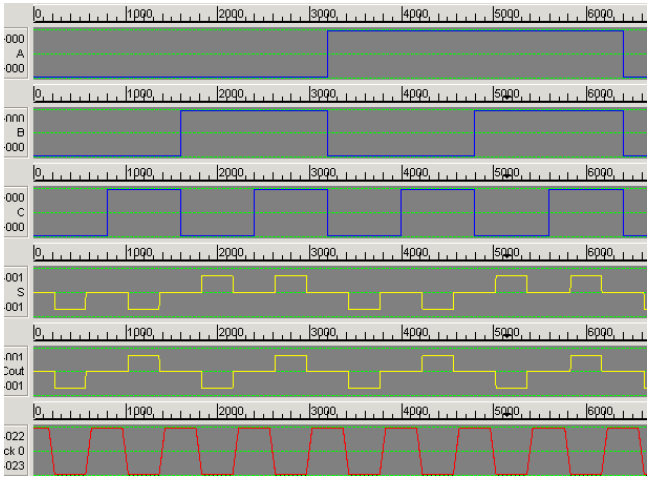

Fig. 12. Simulation result of Full Adder

5. CONCLUSION

Although this method is assumed to be implemented in metal-based QCA implementation,the underlying principles also apply to molecular QCA. There are different clocking schemes such as wave clocking which may be more suitable for molecular QCA. If the manufacturing issues of molecular QCA can be solved, it may be an attractive implementation alternative that mitigates the cryogenic working temperature constraints of metal based QCA. Molecular QCA is considered to be the only feasible implementation method for mass production of QCA devices.

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