Low Power ALU Design considering PVT Variations

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ABSTRACT
ALU is one of the most important components in a microprocessor that carries out the arithmetic and logical operations. This paper highlights the techniques in designing a low power ALU in nanometer CMOS. Different 10 transistor full adders are compared and chosen the Full adder with least power dissipation to obtain low power and area efficient ALU. The power is reduced by 78% when compared to the existing ALU which is designed using XOR based Full adder. The proposed design does not compromise with the performance as the full adder delay is less.

The functionality of the design remains the same despite the temperature and voltage variations.The power dissipation for different temperatures ranging from -50 ^{0}C to +50 ^{0}C has been observed. The ultimate goal is to design an ALU with the least number of transistors thereby decreasing the area and power consumption in the overall circuit that takes shape at the end.

Keywords
ALU, CMOS, power dissipation, full adder

1. INTRODUCTION
In digital electronics, an arithmetic logic unit (ALU) is a digital circuit that performs integer arithmetic and logical operations. The ALU is a fundamental building block of the central processing unit of a computer, and even the simplest microprocessors contain one for purposes such as maintaining timers. The processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs; a single component may contain a number of ALUs. The efficiency of the CPU or microprocessor are determined by the computation efficiency which is based on the ALU design. Arithmetic and Logic unit is one of the major components of the CPU. All arithmetic operations like Addition(+), Subtraction(-), Multiplication(*) and division(/) and logical operations like AND,NAND,OR XOR etc., are carried out inside the ALU.

Power can be minimized at either circuit level or gate level or micro architecture level or architecture level or system level. Here, we attempted to reduce the power at the circuit level. Each design consists of number of micro architectures. Each micro architecture consists of number of gates. For CMOS implementation of the gate, the pull-up and pull-down of the circuit must be realized. A conventional full adder with XOR gates, AND gates and OR gates must be realized with using pull-up and pull-down networks. A conventional CMOS full adder consists of 28 transistors. But, here we have designed a full adder only with only 10 transistors thereby decreasing the area and power consumption.

Variations in process parameters affect the operation of integrated circuits (ICs) and pose a significant threat to the continued scaling of transistor dimensions. Successful design of digital integrated circuits (ICs) has often relied on complicated optimization among various design specifications such as silicon area, speed, testability, design effort, and power dissipation. Such a traditional design approach inherently assumes that the electrical and physical properties of transistors are deterministic and hence, predictable over the device lifetime. However, with the silicon technology entering the sub- 65-nm regime, transistors no longer act deterministically. Fluctuation in device dimensions due to manufacturing process (subwavelength lithography, chemical mechanical polishing, etc.) is a serious issue in nanometer technologies. Until approximately 0.35-um technology node, process variation was inconsequential for the IC industry. Circuits were mostly immune to minute variations because the variations were negligible compared to the nominal device sizes. However, with the growing disparity between feature size and optical wavelengths of lithographic processes at scaled dimensions (below 90 nm), the issue of parameter variation is becoming severe.

Along with process variations supply voltage variations and temperature variations also to be considered while designing Any circuit.

2. FULL ADDER ARCHITECTURES
The full adder performs the computing function of the ALU. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs[2]. Figure 1 shows the logic level diagram of a full adder. The Boolean expressions for the SUM and CARRY bits are as shown below.

SUM=AB'Cin'+A'BCin'+A'B'Cin+ABCin (1)

CARRY=AB+ACin+BCin (2)

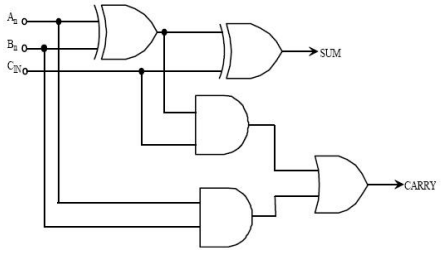


Figure1. Logic level diagram of a full adder.

In this work we have compared various 10 transistor fulladder architectures [4]. and chosen the fulladder which consumes low power for the design of ALU.

SERF (static energy recovery full adder) [10]-[12] is shown in Fig.2 (a). This uses a total of 10 transistors for the implementation of following logic expressions.

Sum = (A⊕B)Cin + (A⊕ B)Cin -------(3)

Cout = (A⊕ B)Cin + (A⊕B)A ---------(4)

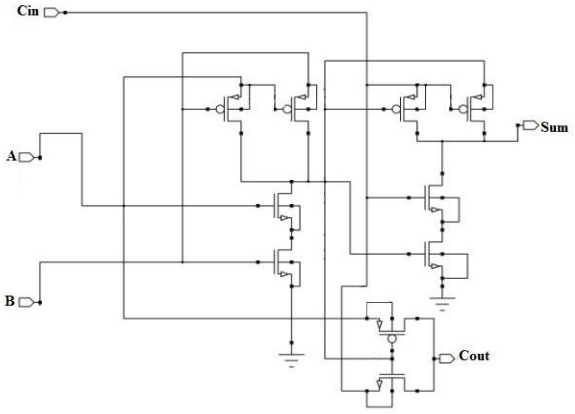
The design is claimed to be extremely low power because it doesn't contain direct path to the ground and it can re-apply charge to the control gate (energy recovery). The combination of low power and low transistor count makes the SERF adder cell a feasible option for low power design. But the disadvantage with this design is relatively slower than peer designs and it cannot be cascaded at low VDD operation due to multiple-threshold loss problem.

The 9A Full adder shown in Fig. 2(b) implements (3) and (4) using 4-transistor SER XNOR, 4-transistor ground less XNOR and 2-to-1 multiplexer [10]-[12].

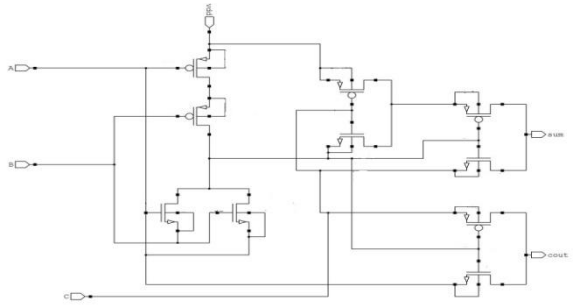
The 9B Full adder has shown in Fig.2(c) implements logic expressions given in (3) and (4) using 4-transistor SER XNOR, 4-transistor ground less XNOR and 2-to-1 multiplexer. Full adder 9B is can be designed from full adder 9A by interchanging the inputs of 4-transistor ground less XNOR [10]-[12].

10 transistors full adder's 13A and 9B have better critical delay than the 10 transistors SERF full adder in all loading condition.

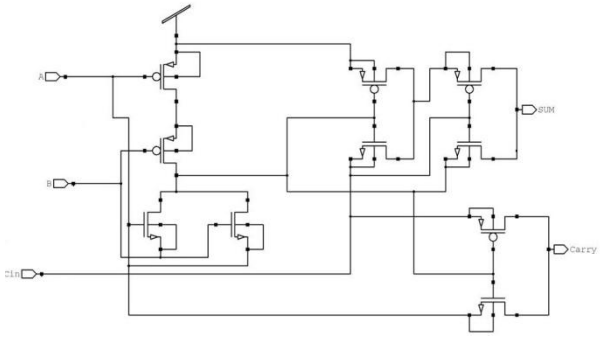
A transistor–level implementation for 10 transistor full adder 13A is shown in Fig.2 (d)



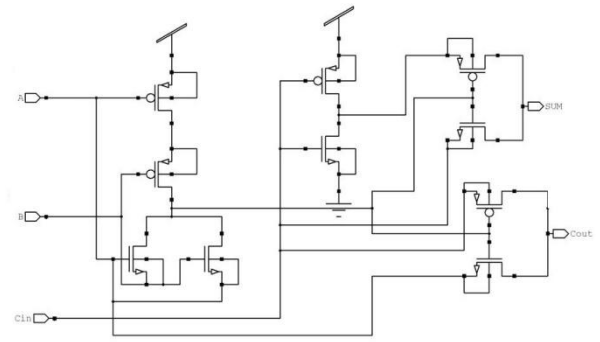
a) **SERF Full Adder**



b) Full adder 9A



C) Full adder 9B



D) Full adder 13A

Fig 2: 10 transistors full adder circuits

We have compared all the fulladders with respect to power and the average power consumed for each fulladder is shown in table.(1) . since the fulladder 9A consumes low power we selected this adder for the ALU design. All the Full adders were given a supply voltage of 2 v and a frequency of 100KHz. The average power consumptions of all the designs above were calculated.

Table 1. Comparison of power dissipations for different architectures of Full Adders

10T Full Adder Designs	Average power consumed
SERF Full Adder	21 uw
Full adder9A	16 uw
Full adder9B	20 uw
Full adder13A	23 uw

3. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic logic unit (ALU) is one of the main components inside a microprocessor. It is responsible for performing arithmetic and logic operations such as addition, subtraction, increment, decrement, logical AND, logical OR, logical XOR and logical XNOR. An ALU is a digital circuit that performs arithmetic and logical operations. The ALU is a fundamental building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors

cont increment, decrement, logical AND, logical OR, logical XOR and logical XNOR. An ALU is a digital circuit that performs arithmetic and logical operations. The ALU is a fundamental building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors contain one. The processors found inside modern CPUs and Graphics Processing Units (GPUs) have inside them very powerful ALUs.

3.1 ALU Design and Operation

We have designed ALU in three different ways by using multiplexers and full adder circuit. The input and output sections consist of 4x1 and 2x1 multiplexers and logic is implemented by using full adder. In the current design the multiplexers are designed with pass transistors and full adder is designed with 10TFA both for minimum area and low power. The pass transistor design reduces the parasitic capacitances and results in fast circuits.

A set of three select signals have been incorporated in the design to determine the operation being performed and the inputs and outputs being selected. Figure 3 shows the block diagram of 4-bit ALU with the CARRY bit cascading all the way from first stage to fourth stage. The ALU consists of eight 4x1 multiplexers, four 2x1 multiplexers and four full adders. The 4-bit ALU is designed in 180nm, n-well CMOS technology. The incrementor operation is carried out by the addition of a '1' bit to the least significant bit of the 4-bit input. The DECREMENT operation is carried out by the addition of '1' bit to all the 4 bit inputs. The complement of B is used for SUBTRACTION operation. The full adder performs the SUBTRACT operation by two's complement method. All the four bits of the subtrahend are complemented and a '1' bit is added to the least significant bit of the resultant. The resultant subtrahend is then added to the minuend to obtain the desired result. The ADDITION operation is carried out by the subsequent addition of the addend and the augend bits respectively.

The outputs from the full adder are fed to the 2:1 mux at the output stage. Based on the condition of the select signals of the multiplexer at the input stage, the choice of addend bits are fed to the full adder. The full adder computes the results. The multiplexer at the output stage selects the appropriate output. Table 2 shows the truth table for the operations performed by the ALU based on the status of the select signals.

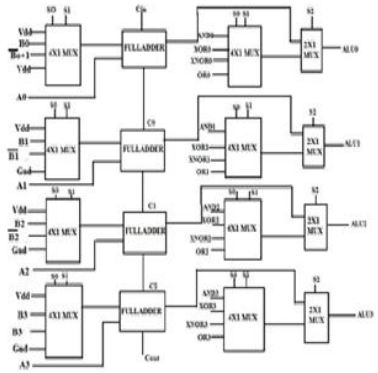


Fig 3: Block diagram of 4-bit ALU

Table2. ALU Truth Table

S2	S1	S0	OPERATION
0	0	0	DECREMENT
0	0	1	ADDITION
0	1	0	SUBTRACTION
0	1	1	INCREMENT
1	0	0	AND
1	0	1	XOR
1	1	0	XOR
1	1	1	OR

3.2 Multiplexer Design

The multiplexers have been used in the ALU design for input and output signals selection. The multiplexer is implemented using pass transistors. This design is simple and efficient in terms of area and timing. Figure6 shows the circuit level diagram of the 2x1 MUX. The output of the 4x1 multiplexer stage is passed as input to the full adder. A combination of the 2x1 MUX and 4x1 MUX at the input and output stage selects the signals depending on the operation being performed.
where S is the select line,I0 and I1 are the 2 inputs of the 2:1 multiplexer. The input and the output stages have a combination of 2x1 multiplexer and 4x1 multiplexers to select one signal from a set of four signals, the select signals being S0, S1 and S2. Signal S2 determines the choice of operation to be performed between arithmetic and logical. The select signals S0 and S1 pick one of the four inputs or output signals and hence determine which of the four arithmetic or logical operations to be performed. For S2=0, one of the four arithmetic operations is performed and for S2=1, one of the four logical operations is performed. Figure 7 and figure 8 represents the block diagram of multiplexer logic at the input and output stage.

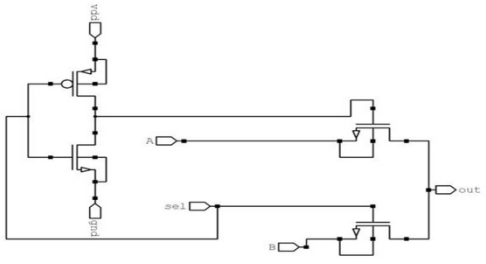


Fig 4. Circuit level diagram 2:1 multiplexer using pass transistor logic

Table 3 . Truth table of a 2x1 multiplexer.

S	I0	I1	OUT
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

A symbol can be used as a building block to simplify the sign of another module at the hierarchical level. It is equivalent to a black box where only input and output pins are seen and this symbol is also used for simulation. The 4-bit ALU consists of two 4-bit inputs, three selecting lines, and one carry input one carry output and 4-output bits. It consists of four outputs and one carryout (out0, out1, out2, out3, cout) and two 4-bit inputs (a0, a1, a2, a3, b0, b1, b2, b3) and three selection lines (S0,S1,S2).If S2=1,an arithmetic operation will be performed else,a logical operation will be performed.The results are observed to be correct for various inputs. The testbench ,output waveform of 4-bit ALU is shown in figure 5, figure 6 respectively.

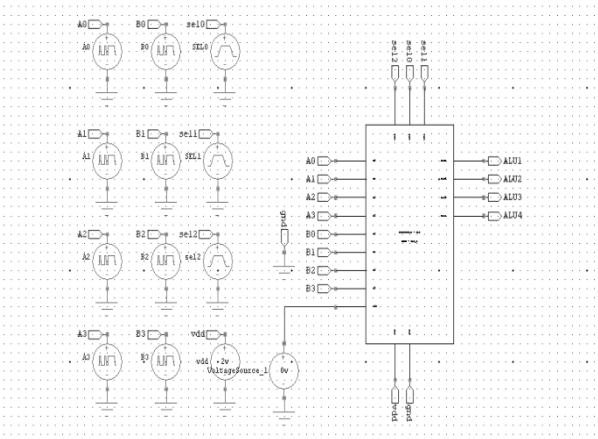


Fig 5. Testbench of ALU

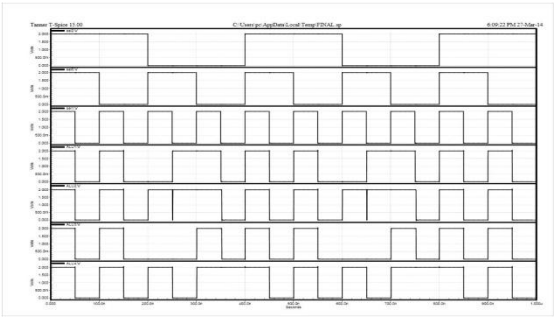


Fig 6. output waveforms of ALU

4. PVT Variations

To check the working of ALU under PVT variations we have operated the ALU under different temperatures ranging from -50 deg to +50 deg and varied the voltage from 2v to 2.3 v and noted the average power dissipation as shown in table4..

Table 4. Power calculations(power in microwatts)

	Temperature(deg)						
Voltage(v)	-50	-30	-10	0	10	30	50
2.0	64.14	62.13	60.86	60.01	59.56	58.34	57.44
2.1	72.62	70.23	68.34	67.23	66.56	65.12	64.08
2.2	80.74	77.68	75.12	74.66	73.88	72.63	70.96
2.3	88.56	85.38	83.61	82.43	81.56	80.06	79.11

The following is the graphical representation of the Power dissipation (uw) taken on y- axis vs different temperatures on X-axis and repated for different voltages.

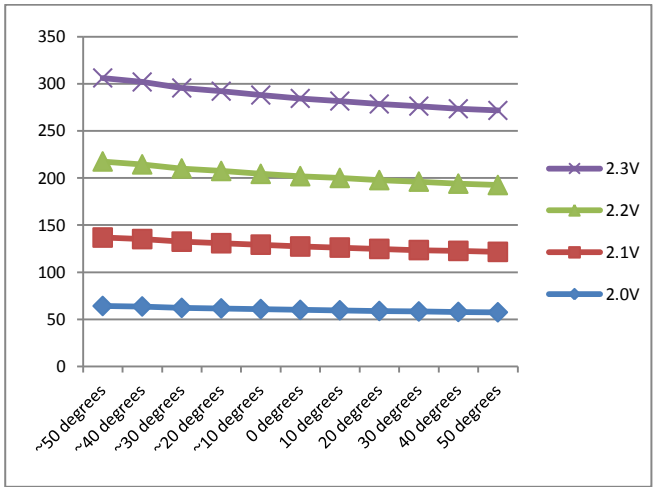


Fig 6. Power dissipation for voltage ,temperature variations

To incorporate the process variations we have decreased the vth by 100 mv(fast cells) and observed the increase in the power dissipation . For a 2v supply voltage at -50 deg temperaturethe power dissipation is 64.14uw for vth=0.4v(NMOS). whereas at vth=0.3v it is observed as 69.72uw.

5. CONCLUSION

In this work, a 4-bit ALU is designed at transistor level for low power and minimum area. In this work much efforts are spent on the design of full adder circuit. Different topologies of full adders are studied and compared. A 1-bit full adder with 10-transistors is chosen for its lowest Power Consumption and minimum possible area. With this full adder, the leakage power is also very less as the number of power supply to ground connections are greatly reduced. The power dissipation of the ALU at different input voltages and temperatures are noted down. Also by changing the process(vth) parameters the power dissipation is observed. The total work is carriedout using tanner tools at 0.13 um.

6. REFERENCES

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