Design and Modeling of Schmitt Trigger-based Sub-Threshold 8T SRAM for Low Power Applications

Mahipal Dargupally
M.Tech (VLSI System Design)
B V Raju Institute Of Technology, Dept.of ECE, (CVD), Narsapur, Medak Dt, Telangana, India

T. Vasudeva Reddy
Assoc. Professor, B V Raju Institute Of Technology, Dept.of ECE, (CVD), Narsapur, Medak Dt, Telangana, India

Udary Gnaneshwara Chary
Assist. Professor, B V Raju Institute Of Technology, Dept.of ECE, (CVD), Narsapur, Medak Dt, Telangana, India

ABSTRACT
This paper presents the design of Schmitt trigger-based 8T SRAM Architecture for low power sub-threshold (or) near-threshold CMOS SRAM for power constrained Applications. Power Consumption, Power Dissipation and Leakage Power are the main factors in the IC Design. Memory unit is the primary block in design of any chip like Micro Processor and Micro Controller. As SRAMs comprise a significant percentage of the area and power for many digital chips and leakage can dominate total chip leakage. The proposed paper used to reduce the leakage power by using High-V_{th} nMOS as pull-down transistors for standard 6T SRAM. This paper demonstrates the Architecture Design and Analysis of 256bitcell 8T SRAM in 45nm technology. The design implementation and analysis is performed using 45nm CMOS technology in CADENCE IDE.

Keywords
8T SRAM, Sub-Threshold, Low power, Low Leakage

1. INTRODUCTION
The Digital sub-threshold circuit design has become a very promising method for ultra-low power applications. Circuits operating in the sub-threshold region utilize a supply voltage (V_{DD}) that is close to or even less than the threshold voltages (V_{th}) of the transistors. This low V_{DD} operation results in ultra low-power dissipation. The circuit operating from strong inversion, moderate inversion regions to weak inversion region can be known as sub-threshold operating region[4].

In Sub-threshold region standard 6T-SRAM shows weak read and write stabilities[5]. the performance depend on static noise margin (SNM). Static Random Access Memory(SRAM) remain to be one of the most paramount and integral memory technologies today mainly because of their robustness and ease at manufacturing. SRAM memory cell better than DRAM as it can perform at low power and can store number of bits .

The rising demand of portable electronics for computing, communication and other applications has necessitated an improved battery life and low power consumption. Sub-threshold SRAM provides an advantage in minimizing total memory energy consumption and providing compatibility with minimum-energy sub-threshold logic[6].

2. SRAM ARCHITECTURE
2.1 Proposed 8T SRAM
The Static random access memory (SRAM) is a type of volatile semiconductor memory to store binary logic '1' and '0' bits. SRAM uses bistable latching circuitry made of Transistors/MOSFETS to store each bit. An SRAM is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption. The design requirement is such that pMOS OFF- state current should be more than the pull-down nMOS transistor leakage current for maintaining data "1" reliably. With increasing process variations and exponential dependence of the sub-threshold current on the threshold voltage, satisfying this de-sign requirement across different process, voltage, and temperature (PVT) conditions may be challenging.

The proposed Architecture is designed using Schmitt trigger-based 8T SRAM bitcell illustrated in Fig.[1]. It is similar to the standard 6T SRAM cell, however it is used High-V_{th} nMOS in this design[4]. Two sleep transistors are used in pull down path to minimize the leakage power[2]. These Transistors used for self correcting feedback to achieve stable operation. This cell also reduces dynamic power in active mode.

A. WRITE OPERATION
In the write operation, WL is enabled to activate the access transistors for data transfer . The proper write operation can be done successfully by consideration of Aspect ratio(W/L) of nMOS and pMOS[6]. In sizing of transistors in SRAM bit cell nMOS should win the ratio fight with pMOS. If we want to write data'1' making the WL=1 and one of the bitline keeping High BL(or)BLB=1 and other is 0.Then the value is been written as '1' at node 'Q' and its complement at node 'QB'.

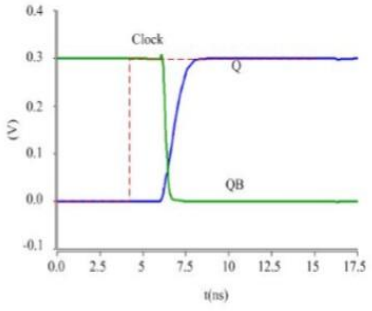

Fig.1 Schmitt Trigger-based 8T SRAM

B. READ OPERATION
In the read operation, BL and BLB are precharged and WL is enabled then one of the Bitline(BL/BLB) is making low . The read value can be observed by enabling the Sense Amplifier.

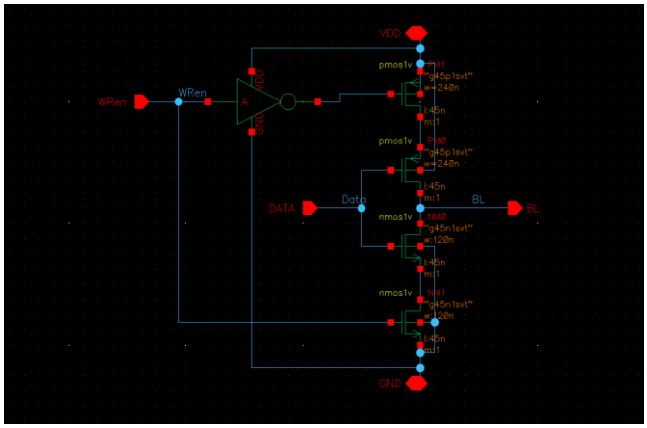

Fig.2 The simulation result of a single cell write operation

The written data can be stored at node 'Q' and its complement at 'QB' in standby mode. this data can be with held at the node till the read operation being accessed. here the leakage has been minimized by using the sleep transistors in pull down path and effectively read by acting as feedback transistors.

2.2 Sense Amplifier

The voltage mode sense amplifier is used for designing. This is the Enhanced Positive Feedback sense amplifier is using to operate the read operation effectively and it can reduces the bit line capacitances by decoupling the nMOS transistors in design shown in Fig.3. The written data can be enhanced effectively here[8]. This design operated at 0.4V and power dissipation is 942.2pW.

SE = 1 , Sense mode

SE = 0 , Standby mode

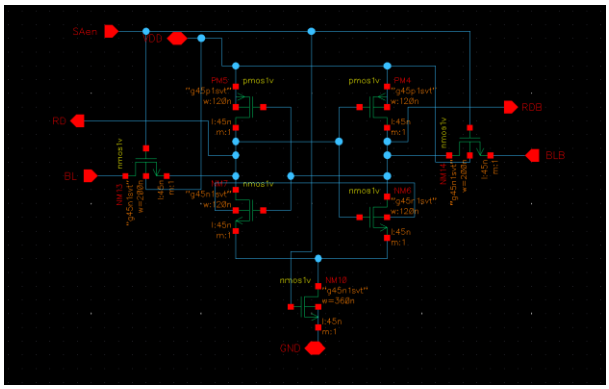

Fig.3 Enhanced Positive Feedback Sense Amplifier

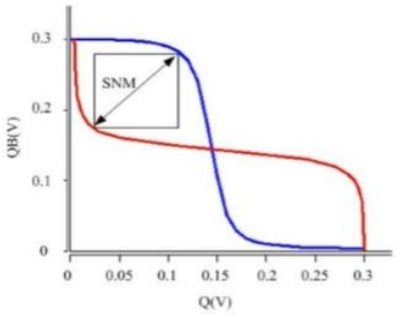

Fig.3 SNM of the proposed SRAM

2.3 Data Write Circuit

Write operation into the memory cell can be done only when the write enable ON. This enable operation can be easily understood by the following circuit Fig.3. Write operation into the memory cell can be done only when the write enable ON. This enable operation can be easily understood by the following circuit. The design being operate at0.4V and observed delay and power 4.79nS,1.38nW respectively.

2.4 Decoder and Multiplexer

The proposed Architecture is also consist of decoder and multiplexers for Memory Array operation designed. The 4to16 Decoder is designed using 4input nor-gate design and multiplexer16x1 is using four 4x1mux with nand-gate based design for minimizing area and power.

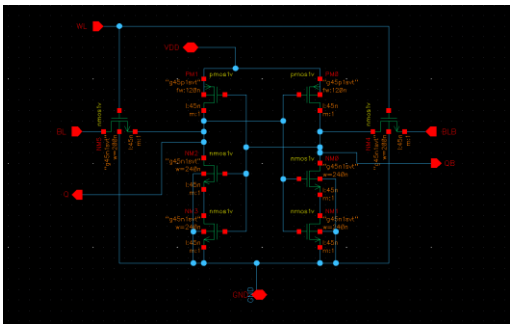

Fig.4 Data Write Circuit

3. ARCITECTURE OF 256BIT SCHMITT TRIGGER-BASED 8T SRAM

The proposed architecture of 256bit ST-based 8T SRAM cells is designed using address decoder, pre-charge circuitry, data write circuitry, sense amplifiers and 16x16 SRAM array in 45nm technology. The Fig.5 shows the design implementation symbol for proposed architecture. The Fig.8 illustrates the implementation of single bit ST-based 8T cell. The block diagram of SRAM memory with all input signals, pre-charge, write enable, sense amplifier enable, 16x16 memory array has illustrated in Fig.8.

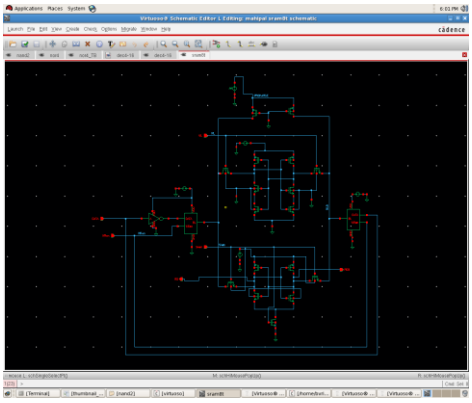

Fig.7 single bit schmitt trigger-based 8T SRAM

4. SIMMULATION RESULT

The Fig.9 illustrating the operation result of proposed Architecture. This paper explores the design of Schmitt trigger-based 8T SRAM bit cell. observation of operations and analysis of different parameters like power consumption(PC), leakage power(LP) and delay in the sub threshold region. The design has manipulated for different voltage supplies measurements have been observed over the range of voltages 0.8V down to the sub threshold region in 45nm technology library. The CADENCE VIRTUOSO SCHEMATIC EDITOR was used for designing and analyzing[10]. The Table.1 shows the operated result.

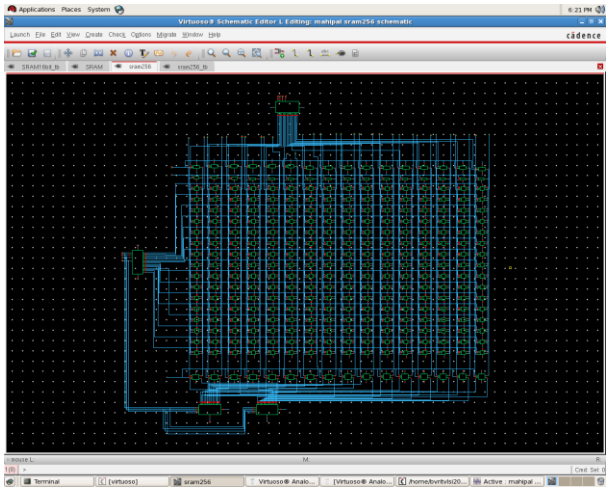

Fig.8 256Bit memory array

Table.1: operation result of SRAM Cell

V_{DD}	Single bit	16bit	256bit
Power Consumption	12.765nW	317.9nW	474.6nW
Leakage Power	0.497nW	4.74nW	7.98nW
DELAY	114.6ns	156.4ns	168.9ns

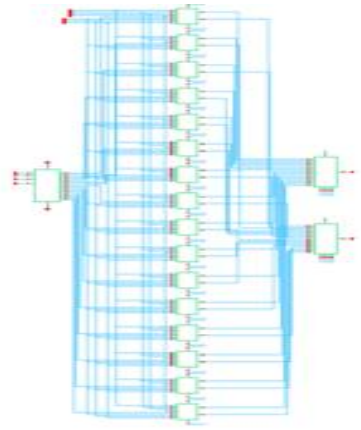

Fig.5 256Bit Cell Architecture Symbol

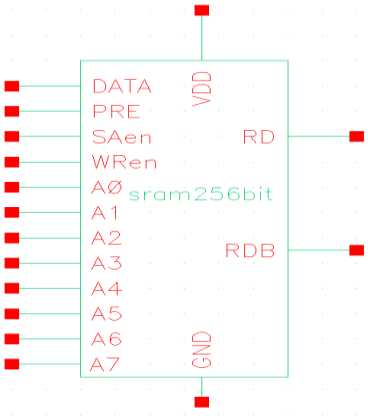

Fig.6 Proposed Architecture

Fig.9 Performance characteristics of operation

5. CONCLUSION

This study implemented a 256b Schmitt Trigger-Based Sub-Threshold 8T SRAM in a 45 nm CMOS technology with a High-Vth nMOS and sleep transistors in pull down path. It has been reduced a leakage power in high rate. architecture design complexity reduced with appropriate Module selection for sixteen ST-based 8T bit cells in bit-interleaving scheme. We simulated the single bit SRAM with a normal Vth NMOS in the Write path observed the power consumption of 1.15nW and in High-Vth nMOS the power consumption reduced to 117.7pW. The simulation results of entire Architecture power

consumption is 474nW with an operation frequency of 6MHz at 400 mV was achieved. The standby power dissipation is 7.98nW. Hence the design has achieved low power operation without degrading the performance.

6. ACKNOWLEDGEMENT

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8. AUTHOR'S PROFILE

Mahipal Dargupally is research student, pursuing M.Tech in VLSI System Design from B.V.Raju Intitute of Technology, completed B.Tech from JNTUH, Hyderabad. His Area of interest is Low power VLSI Design, Memory design and Logic circuits.

T.Vasudeva Reddy was born in 2nd FEB 1979. He received his B.TECH from Madras University, Tamilnadu In 2002. And M.TECH from JNTU Hyderabad, AP, in 2008. He is an Associate Professor, Dept.of Electronics & Communication Engineering in B.V.Raju Institute Of Technology, Narsapur ,Medak Dt,. Presently, he is pursuing PhD on the topic of low power memory cell design. He had 12years of teaching experience. His research interests are Low power VLSI design.

Udary Gnaneshwara Chary obtained M. Tech degree in VLSI System Design from VNR Vignan Jyothi Institute of Technology. Presently, he is pursuing PhD from JNTU Hyderabad. He is an Assistant Professor in B.V.Raju Institute of technology Narsapur, Medak. He had 8years of teaching experience. His research interests include CMOS Analog design.