Analysis of Sub Threshold to above Threshold Leakage Reduction Technique for CMOS At 65nm

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ABSTRACT
In this paper, a dual supply level shifter is designed for robust voltage shifting from sub threshold to above threshold domain using high voltage CMOS technique. High voltage CMOS is an effective circuit level technique that improves the performance and design by utilizing high threshold voltage. In this minimum input voltage attainable while maintaining robust operation is found to be around 180mV, at maximum frequency of 1MHz. The level shifter employs an enable/disable feature, which allowing for power saving when the level shifter is not in use.Power dissipation has become an overriding concern for VLSI circuit designers. Proposed level shifter is compared with the previous work for different values of the supply voltage and when implemented on a 65nm CMOS technology, node capable of converting subthreshold voltage signals to above threshold voltage signals.. All these simulation results are based on 65nm CMOS technology and simulated in cadence tool.

Keywords
Level shifter(LS), High voltage CMOS

1. INTRODUCTION
Variation from constant field scaling due to the non-scaling parameters of the MOS transistors leads to an increase in the power consumption and power density with each new technology[1],[4]. The increased power dissipation degrades the reliability, enhance the cost of the packaging and cooling scheme and lower the battery lifetime in portable electronic device.

In many integrated circuits, such as display drivers, a combination of high-voltage driving capability (an output voltage swing up to lOOV or more) and a digital control by means of standard 5V CMOS logic is required. For this reason, complex level-shifting circuits are needed to convert the 5V control signals into the desired high voltage output waveforms. On the other hand, there is no universal way to avoid tradeoffs between delay ,power, and area, and thus, designers are in demand to choose appropriate techniques that satisfy applications.

Power consumption of CMOS consists of dynamic and static components. Self-motivated power consumption is when transistors are switching and static power consumption is regardless of transistor switching. The main reasons causing the increase in leakage power is the increase of subthreshold leakage power. While technology scales down, supply voltage also scales down concurrently. The Sub threshold leakage power increases exponentially as threshold voltage decreases.

A very interesting research topic, wherever both high-voltage driving capability and extremely low power consumption are required, is the design of driver chips for cholesteric texture LCDs [l]. Rather ,high voltage levels (50V) are necessary to switch this kind of liquid crystal fiom one stable state to another, except its inherent memory function is undoubtedly a major advantage compared to other types of liquid crystals, while it allows us to implement certain display systems with very low image frame rates and a high degree of power efficiency. As a result, the cholesteric texture LCDs are ideal components in battery-operated display systems with slowly or sporadically varying images, other than for the generation of the required waveforms on the display rows and columns, new high-voltage driver circuits with very low power dissipation have to be developed.

2. RELATED WORK
In this paper the conventional level shifter, shown in Figure 1, can be implemented as an interface between two voltage domains as long as the input voltage is above the threshold voltage of MN1 (and MN2). The level shifter has the following operational behavior: When the input goes form a logic low to a logic high, MN1 is turned on and MN2 is turned off. Then, the voltage at node nA is pulled towards ground due to the conducting path established by MN1. If the voltage at node nA reaches (Vdd- VthMP2), the positive feedback is triggered as MP2 turns on and pulls node nB high. The input has then been shifted from as a lower voltage level, to a higher voltage level through the output inverter. The voltage shift can be competed only if the pull-up/pull-down ratio is roughly the same. In other words, the pull-up strength has to be close or equal to the pull-down strength. If the pull-up/pull-down ratio is not close to unity, contention will take place between the pull-up transistors(MP1 and MP2) and pull-down transistors (MN1 and MN2), which will increase delay and increased power consumption. [4] This contention worsens when the input signal approaches subthreshold. For subthreshold voltages on the input, the drive strength of MN1 cannot overcome the drive strength of MP1. Hence, node nA cannot be pulled down, and the positive feedback cannot be triggered, labeling the conventional level shifter impractical for subthreshold conversion. In order to enable subthreshold conversion, the pull-up/pull-down ratio has to be equalized.

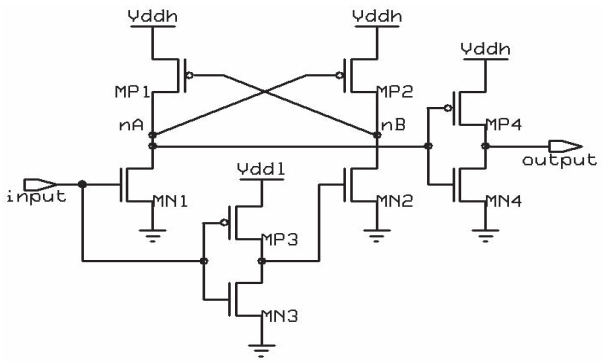

Figure 1: Conventional Level Shifter

3. PROPOSED LEVEL SHIFTER

The proposed multi V_{TH} level shifter is described in this section. This level shifter uses a multi V_{TH} CMOS technology in order to eliminate static dc current. According to Figure 2., the circuit consists of an input inverter, main voltage conversion stage, output inverting buffer and sleepy keeper. To increase the strength of the pull-down network of the main voltage conversion stage, it was also designed by using 1V transistors [1]. The current flowing through the nodes NH and NL at the beginning of their high to low transition could be of concern. Therefore to reduce this cause, two PMOS devices (MP2 and MP3) are adopted. MP4 and MP5 helped in weakening the pull-up networks of the main voltage conversion stage, thus reducing conflict NH and NL nodes. That choice also reduced the leakage current flowing through the pull-up networks when they are turned OFF. At last to acheive reliable voltage conversion, two diode-connected PMOS devices (MP6 and MP7) were placed between the pull-up logics and the supply rail V_{DDH}. These devices limit the pull-up strength, however also reduces power which is static. This section briefly describe the working of the circuit. A high to low transition of the main input causes MP4 being turned ON. Its drain current brings the diode-connected MP6 device into the saturation region.

This creates a voltage drop across MP6 terminal that produce a bulk source voltage drop on MP4. Due to this bulk effect, there is increase in the MP4 threshold voltage and the reduced voltage level (V_{DDH}-V_{TH}, MP6) on the source terminal of MP4 limits its V_{GS}, so further weakening the MP4 action. while MP4 is turned ON, MP5 is therefore turned off. Here in the small leakage current flowing through MP5 is not enough to turn MP7 ON. That's why, MP5 results power gated from the V_{DDH} power rail, foremost to a significant reduction in its sub-threshold current.

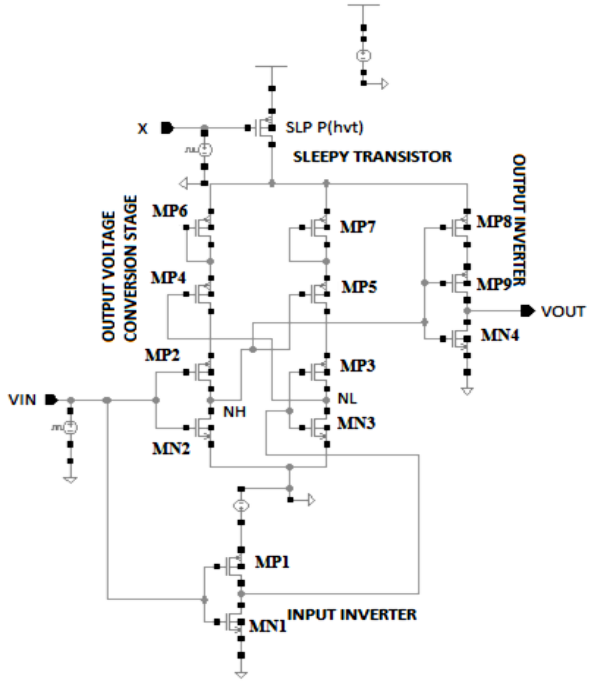

Figure 2: Level Shifter Design

The diode-connected MP7 device minimizes the leakage current and by increasing the threshold voltage of MP5. Actually, MP7 causes the source of transistor MP5 to be at lower voltage than the bulk node and thereby reduces the subthreshold leakage current due to the bulk effect that significantly differs from those adopted in other LS designs Which implemented diode connected transistors [7]. While MP6 limits the output range of the main conversion stage to an output inverter is connected to node NH, as assure a required conversion. Then pull-down of such an inverter uses a MP8, MP9 and MN5 device, where its pull-up is designed by exploiting PMOS transistors stack, so limiting the leakage current flowing through the pull-up network of the output inverter, when NH is high. Reverse and substantial threshold voltage variations on MP6 and MP8-MP9 could cause the latter transistors to go in weak inversion, so increasing the static power dissipation. At this moment sleepy transistor is placed in series with MP6, MP7, MP8 and power supply. The sleep control scheme is used for efficient power supervision. In the active manner, X is set low and SLP P(hvt) is turned ON. While their on-resistances is small and supply voltage almost function as real power line. During the standby manner, X is set high and SLP P(hvt) turned OFF and decreasing the power dissipation.

4. RESULTS AND ANALYSIS

In this section, proposed level shifter is compared to the conventional level shifter for propagation delay and average power consumption. The available gaps in the propagation delay path, the power consumption and delay overhead of the level shifter and the availability of high efficiency power supplies. Availability of a multi-V_{TH} CMOS technology are the important factors affecting the optimum supply voltages in a Multi-V_{DD} system. The wide range of lower supply voltages is considered in this paper since the factors vary with the technology and the application at different values. Simulations are carried out for the following values of VDDL 0.8V, 1.0V and 1.2V for conventional level shifter and then for same voltages LS using sleepy keeper is verified at different levels. Preferred and far better results are obtained using LS with sleepy keeper than conventional Level shifter. That results are listed in Table I. and observed that our approach gave far better results.

Table I - Performance chararterstics and comparisons

Circuits	Voltage	Power delay product (Joule)
Conventional LS	0.8 V	3.11E-15
	1.0 V	2.36E-15
	1.2 V	2.01E-15
Proposed LS	0.8 V	1.218E-15
	1.0 V	1.260E-15
	1.2 V	1.385E-15

Level Shifter has been made to operate on 0.8V. So, It has been observed that level shifter upconverts the output voltage level to 2V.The dynamic power graph is analysed at 0.8 V using cadence virtuoso tool. It has been observed that PDP is 64% improved in this design than conventional level shifter.

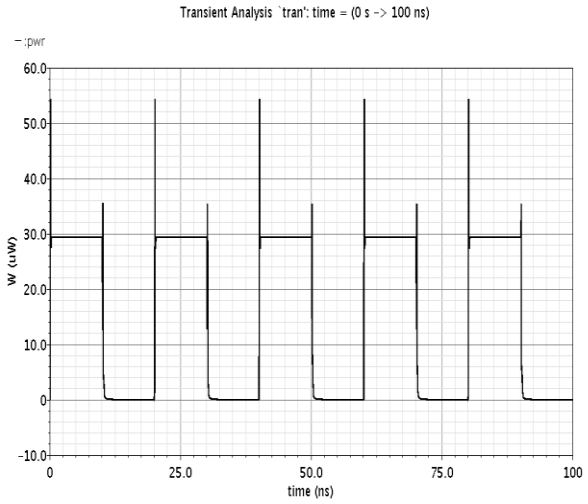

Figure 4: Dynamic power at 0.8 V

Level Shifter has been made to operate on 1.0V. So, It has been observed that level shifter upconverts the output voltage level to 2V.The dynamic power graph Figure 5. is analysed at 1.0V using cadence virtuoso tool. It has been observed that PDP is 50% improved in this design than conventional level shifter.

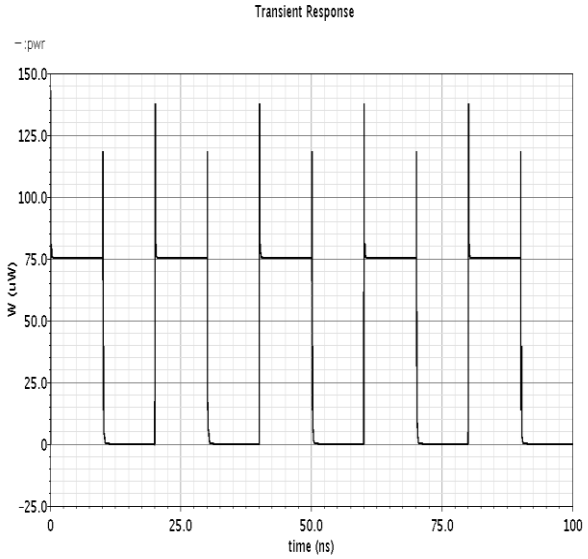

Figure 5: Dynamic power at 1.0 V

Level Shifter has been made to operate on 1.2V. So, It has been observed that level shifter upconverts the output voltage level to 2V.The dynamic power graph Figure 6. is analysed at 1.2V using cadence virtuoso tool. It has been observed that PDP is 36% improved in this design than conventional level shifter.

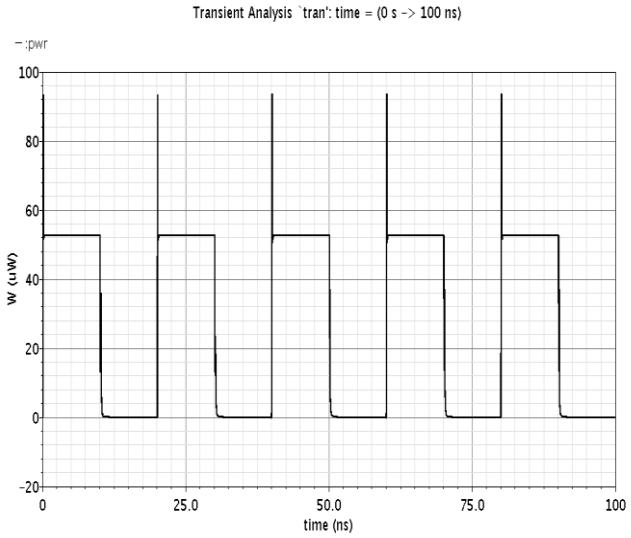

Figure 6: Dynamic power at 1.2 V

Frequency-V_{DDL} graph in different threshold regions is plotted at various frequencies and following characterstics are observed at different threshold regions.

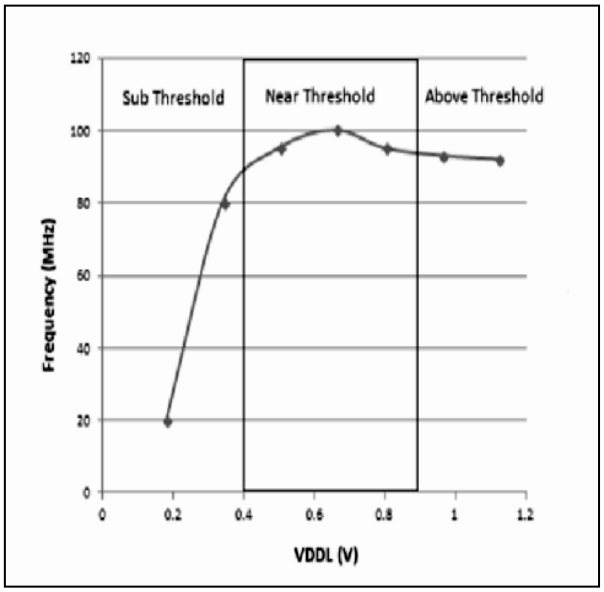

Figure 7: Frequency-VDDL Graph in different threshold regions

5. CONCLUSION

It can be concluded that a proposed low-power LS suitable for robust logic voltage shifting from near/sub-threshold to above threshold domain with reduced power dissipation. Leakage reduction technique plays a key role in VLSI circuit designing. Scaling down the appropriate parameter can reduce the leakage power. This circuit exploits proper design strategies to limit energy and static power consumption. while this circuit used for sub-threshold to above threshold voltage conversion, the proposed design exhibits the lowest static power and energy consumption with respect to previous proposed LSs that used similar design parameters. Besides, even though the new designed LS is optimized for low power consumption, that also reaches high-speed performances and supports a wide voltage conversion range.

6. REFERENCES

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