Comparative Analysis of Metastability with D FLIP FLOP in CMOS Circuits

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ABSTRACT
The appropriate choice of flip-flop topologies is of essential importance in the design of integrated circuits for CMOS VLSI high-performance and high-speed circuits. The understanding of the suitability of the flip-flops and select the best topology for a given application is important to meet the need of the design to meet low power and high performance circuit subject. This work shows a wide area comparison exist in D flip-flop, this provides a wide study of the topologies in terms of power dissipation, delay, and rise delay and fall delay time.

Keywords
Metastability, D Latch, Flip-Flop, Microwind.

1. INTRODUCTION

The scale is an electronic circuit which stores a logical one or more data input signals in response to a clock pulse state. The flip-flops are often used in calculation circuits for operation in the selected sequences for periodic clock intervals to receive and hold data for a limited period of time sufficient to other circuits within a system of other process data.

It is well known that systems are a synchronous data system that with a single movement of the clock signal is easier to design. Any violation of synchronous design style could greatly complicate the design, raise the required analysis, prohibit the use of certain aids to powerful design, make several retirement are unnecessary testability and generally increase design time and risk system failures

In a synchronous system, the operation of the circuit is ensured whenever correct and respected physically establish and maintain restrictions at all scales. The delay must be throughout the combinational logic circuit are essential requirement of the design. This simplifies the design, maintenance and testing of the system. The outputs are predictable, given the inputs in the steady state, simplifying circuit troubleshooting. Finally, there are computer algorithms that analyze accurately the behavior of synchronous systems, which facilitates large models.

Metastability failure synchronization through a binary switching system with logic outputs undecided indefinite proliferation of non-binary signals and digital circuit is detected when it is said to occur. It is expected synchronous system because non-binary state binary states clearly illegal. The synchronization failure of a flop due to metastability occurs in conditions of critical synchronization input when narrow pulses occur on the clock input, or when the inputs change simultaneously [1]. These situations critical time cannot be avoided, as explained above. Furthermore, synchronization failures due to metastability must be eliminated or at least minimized. It is then clear that the solution that effectively treats the metastable operation is required. The key is to create a synchronization device that can solve the metastable state and make it more resistant to operating system metastable. To design such a synchronizer, an understanding of the locking behavior before, during and after the metastable operation is necessary.

2. METASTABILITY CONDITION

Metastability is pervasive and errors may occur in any synchronous circuit, where an input signal can change randomly with respect to a reference signal. Combinational logic circuits can be immunized against the effects of soft errors using two methods. First, the failure probability of a transition occurring in any node in the sensing circuit can be minimized. This approach the soft error problem is addressed in the source by reducing the likelihood of an erroneous pulse SET generated [2]. Selectively hardening the series of gates can be susceptible in the absence of most of the defective pulses in the circuit. Second, the probability of an SET is latched into flip flop can be minimized. This approach to the problem of software errors in the sink goes although it is allowed in sets originate from any node within the logic that allows this type of erroneous rulings to be registered by the sequential element. By carefully designing a flip flop for filtering a large fraction of the incident set on his data port is possible to completely remove a software error occurs in the logic to permeate the architecture or system level. Naturally, the choice of one approach over the other is dictated by the amount of overheads being introduced. It directly modifies the doors inside incurred circuits, in general, large overhead in power, delay and area that can prohibit the convergence of design. By contrast, modification only flip-flop elements present in the limit of a logic circuit incurs little cost in terms of power and area, but can greatly influence the characteristics of the overall design time and also place additional restrictions on network clock trees.

Therefore, it is necessary to consider these SER based approaches to mitigation flop based in the door and flap separately and together, along with their associated costs, while the optimization of logic circuits for improved SER immunity.

2.1 Metastability Measurement

In a timer, if the data input is high sufficiently in advance of the clock edge, the output of the synchronizer always goes high and if it is significantly after the clock will always be low. If both edges are close enough, the high or low result is affected by circuit noise and is not deterministic [4]. Here we define the separation between data and clock that gives a chance just as a result of high or low as the equilibrium point. In the absence of noise, an input exactly at the point of

equilibrium to settle takes an infinite time. The answer synchronizer metastability is generally exponential.

Thus, for inputs a time Δtin away from the balance point, where Δtin is less than the metastability window, the relationship between resolution time t and Δtin is given by

$$t = \tau * \ln \frac{T_w}{\Delta t_{in}} \quad (1)$$

Typically, it is measured from the normal propagation delay a small change in input much time will cause a change in the time of departure.

$$dt = -d\Delta t_{in} . \frac{\tau}{\Delta t_{in}} \quad (2)$$

If the resolution time is longer than the time allowed for synchronization, the synchronizer may fail as a result of an undefined output level. The number of failure events caused by the data edge occurring less than from the balance point in a total time depends on the clock rate and the data rate and is given by [5].

$$\text{Number}_{\text{failure events}} = T^* \Delta tin^* f_c f_d \quad (3)$$

From (3), the mean time between each failure event is [5].

$$MTBF = \frac{1}{\Delta t_{in} f_c f_d} \quad (4)$$

Using (1) and (4), MTBF can also be expressed in terms of known system and circuit parameters:

$$MTBF = \frac{e^{\frac{1}{t}}}{T_w f_c f} \quad (5)$$

3. D FLIP FLOP SIMULATION

A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental component of digital electronics systems used in computers, communications and many other types of building systems.

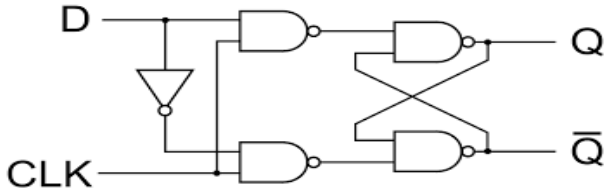

Fig.1 D Flip Flop

D flip-flop is also known as a "data" or "delay" flip flop-. The D flip-flop captures the value of the D input in a defined portion of the clock cycle (such as the rising edge of the clock). This captured value becomes the output Q. In other cases, the Q output does not change. The D flip-flop can be seen as a memory cell a zero-order hold, or delay line. Most type D flip-flops in integrated circuits are capable of being forced to set or reset state (that ignores the D inputs and clock), as well as an SR flip-flop. In general, the S = R = 1 condition is resolved illegal D-type flip-flops.

By setting S = R = 0, the flip-flop can be used as described above. This is the truth table for other possible configurations S and R.

TABLE I
TRUTH TABLE OF D FLIP FLOP

INPUTs			OUTPUTs	
S	**R**	**D**	**Q**	**Q'**
0	**1**	**X**	**0**	**1**
1	**1**	**X**	**1**	**0**
1	**1**	**X**	**1**	**1**

These sandals are very useful, since they are the basis of the shift registers, which are an essential part of many electronic devices. The advantage of flip-flop type D "transparent latch" is that the signal at the input pin D the moment is captured in the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. One exception is that some flip-flops have a "reset" signal input, that Q is reset (to zero), and can be asynchronous or synchronous with the clock. The above circuit record contents moves to a bit position to the right on each active clock transition. The X input is shifted to the position of the left bit. The operation of the D flip flop latch is similar to except that the output of the D flip-flop takes the state of the D input at the time of a rising edge at the clock pin (or negative edge if the clock input is active low) and can delay it by one clock cycle. That is why, which is commonly known as a delay flips flop. The Flip Flop D can be interpreted as a delay line or zero-order hold. The advantage of flip-flop type D "transparent latch" is that the signal at the input pin D the moment is captured in the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next if the clock.

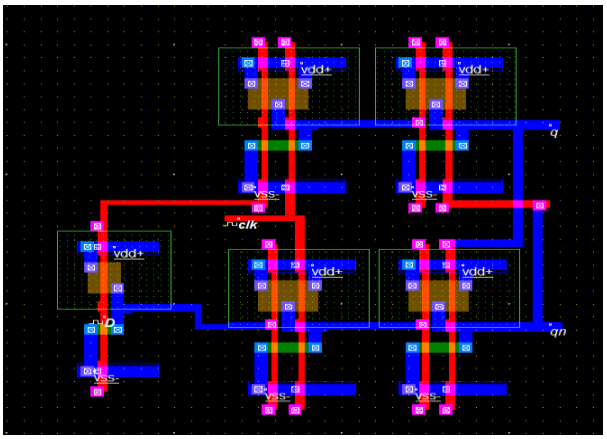

Fig.2 Layout design of D Flip Flop

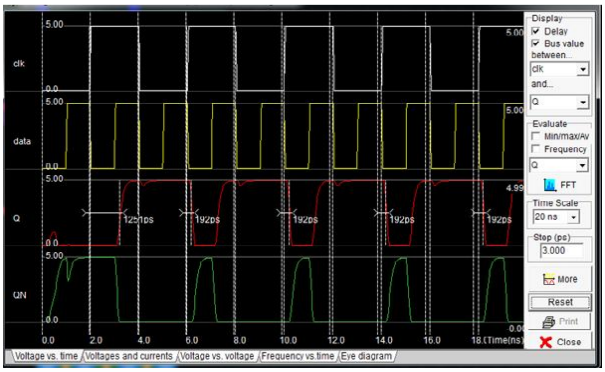

Fig.3 voltage vs. time waveform of D Flip Flop

4. TRANSMISSION GATE BASE D FLIP FLOP

4.1 Simulation of transmission D flip flop

Transmission gate "includes NMOS and PMOS because both NMOS pass good at" 0 "and PMOS good step" 1 ".

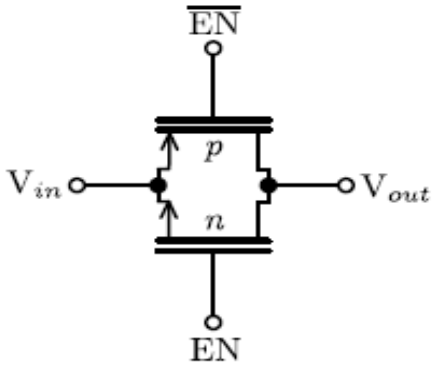

Fig.4 A transmission Gate

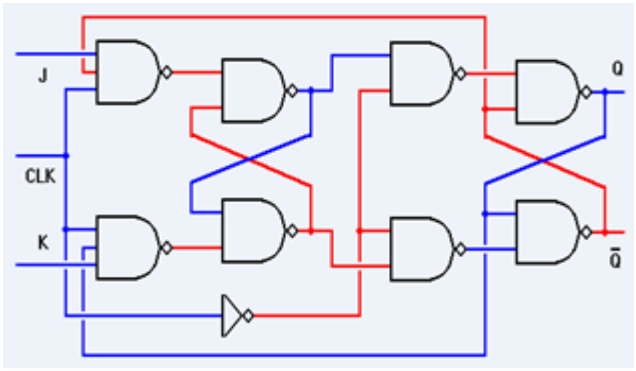

Fig.5 A transmission gate D Flip Flop

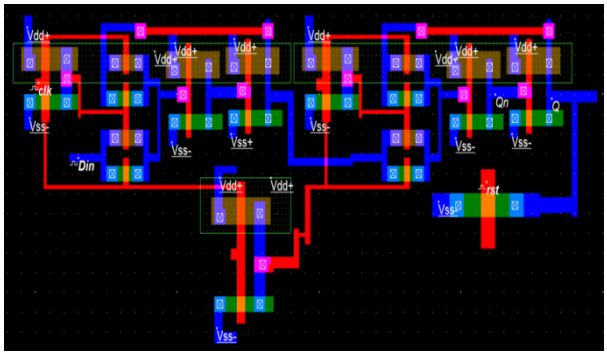

Fig.6 layout design of Transmission gate base D flip-flop

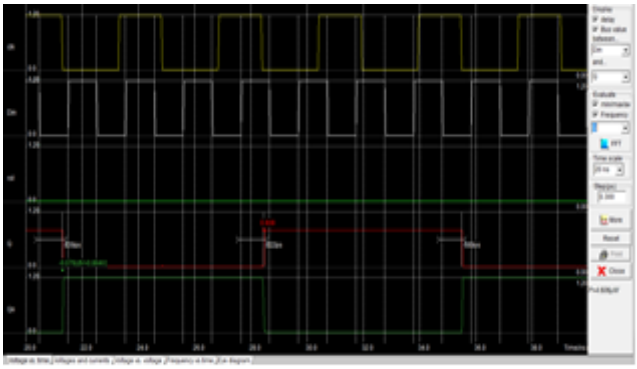

Fig.7 voltage vs. time waveform of transmission D Flip Flop

5. COMPARATIVE ANALYSIS TABLE

TABLE II
COMPARISON BETWEEN D FLIP FLOP AND TRANSMISSION D FLIP FLOP

	Power dissipation	Switching delay	Clock freq.	Number of transistor	Metastable error calculate
D Flip Flop	3.6 to 6.4uW	0.147 to 0.199 ns	1GHz to 10 GHz	14	11 to 49
Transmission D Flip Flop	3.7 uW to 7.21uW	1.46 ps to 4.36 ps	0.5 GHz to 1GHz	48	NA

6. SIMULATION RESULTS OF METASTABLE CONDITION

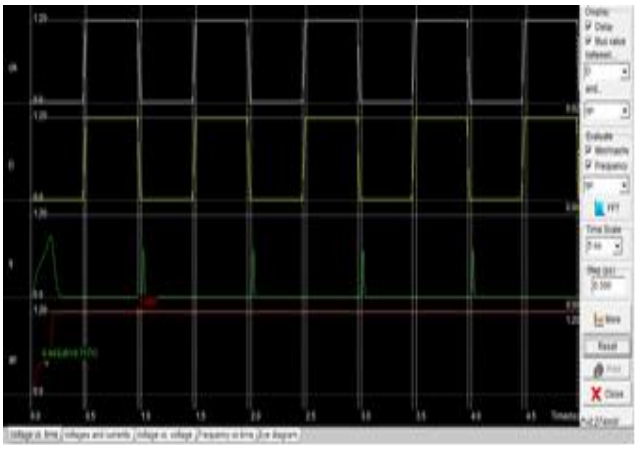

Fig.9 Metastable output of D Flip Flop

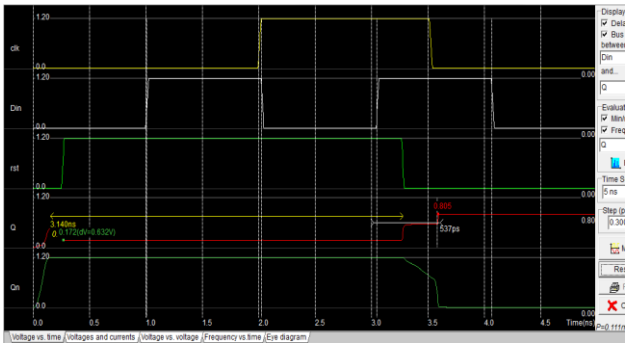

Fig.10 Metastable output of transmission D Flip Flop

7. CONCLUSIONS

Metastability is unavoidable in asynchronous systems. Transmission D flip flop circuits reduces the metastability due to presence of low power, clock frequency. In future this transmission gate can used to reduce the stray capacitances and number of transistors required for the designing of flip-flop circuit. The result shows the power dissipation, delay, rise time delay and fall time delay.

8. ACKNOWLEDGMENTS

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