Vedic ALU using Area Optimised Urdhva Triyambakam Multiplier

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ABSTRACT
Multiplication has some limits and to overcome these limitations a new approach has been describe and designed a Vedic multiplier with proposed unique addition structure, which is used to perform addition of partially generated products. To meet main concern 'area' and 'speed' we have came up with a need particular high speed ALU, the speed of ALU greatly depends upon the speed of multiplication unit used in it. There are numerous multiplication techniques exist now a days at algorithmic and structural level. It is been shown that Vedic multiplication is the fastest multiplication method but there are some other multiplication techniques which are batter then vedic multiplication in terms of chip area. This Proposed work is a unique architecture of 16 bit vedic with combination of 4 bit vedic multiplications and that 4 bit multiplication is been have developed with a unique addition structure. The observed results are been very good and optimised. Later on ALU module is been developed. The tool used for the designing is Xilinx XST and the target platform for validation is Vertex family vertex-4 FPGA, the preferred language is VHDL.

Keywords
Vedic mathematics, Carry save adder, Arithmetic and logical unit, Urdhva Tiryambakam sutra, RTL, User constrain file

1. INTRODUCTION
Now days we are living in digital world, where all operations get performed with more reliably and highest accuracy by digital signal processor. The key element of all the processors like Microprocessor, Microcontroller, DSP processor etc is ALU. Every digital domain based technology depends upon the operations performed by ALU either partially or whole. Speed is the most prominent factor of processor and controllers being used recently. [7], [8] describe the Vedic mathematics from beginning and discuss all operations.

By improving the ALU unit we can develop efficient the Digital Signal Processor, for that proposed Arithmetic unit appears very useful [6]. One of the major purposes of Vedic mathematics is to execute the difficult calculations in simple way, even manageable orally without much use of pen and paper.

2. VEDIC MULTIPLICATION TECHNIQUE
In conventional mathematics Vedic mathematics is used to reduce the complex calculation in the to very simple one. The human mind works on the natural principles on which the Vedic formulae are based. Vedic Mathematics is a method of arithmetic rules which allows much more efficient speed implementation. It also provides few effective algorithms which can be applied to many branches of engineering like computing.

2.1 Urdhva Tiryambakam Sutra
The proposed Vedic multiplier is based on the "Urdhva Tiryambakam" sutra. These formulas are mainly used for multiplication of two decimal numbers[6]. In present paper we apply this algorithm on binary numbers. This multiplication formula can be apply to all cases of multiplication .The term "Urdhva Triyambakam" originated from two Sanskrit words Urdhva and Triyambakam which means "*Vertically" and "Crosswise*" respectively[5]. This method is based on the concept in which all partial products are generated concurrently. This algorithm can be applicable for n x n bit number. All the partial products and their sums are parallely calculated; the multiplier does not dependents on the processors clock frequency. It can be easily layout in microprocessors due to its regular structure, and designers can easily identify these problems to avoid device failures. Processing power of multiplier can be easily enhanced by increasing width of the input and output data bus. It can be easily layout in silicon chip due to its regular structure. The multiplier based on "Urdhva Tiryambakam" sutra has the advantage that in comparison to other multipliers gate delay and area increases very slowly as the number of bits increases. So this multipier is space, time and power efficient.

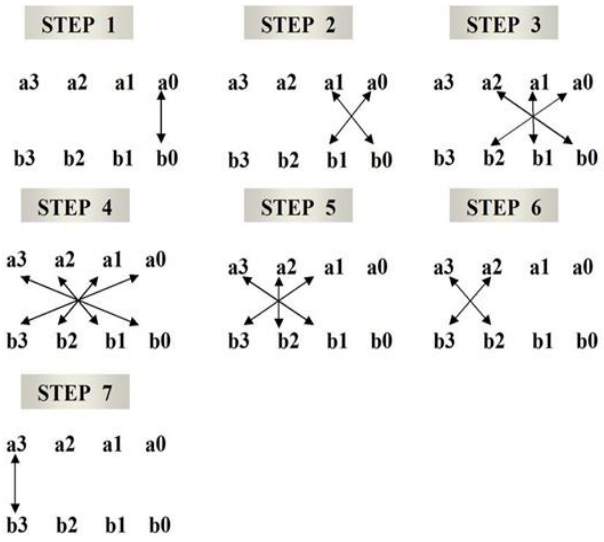

Figure 1: Multiplication of two 4 bit numbers using Urdhva Tiryambakam method

3. PROPOSED ARITHMETIC UNIT

Proposed 16x16 bit Arithmetic Unit is given in the figure 2.

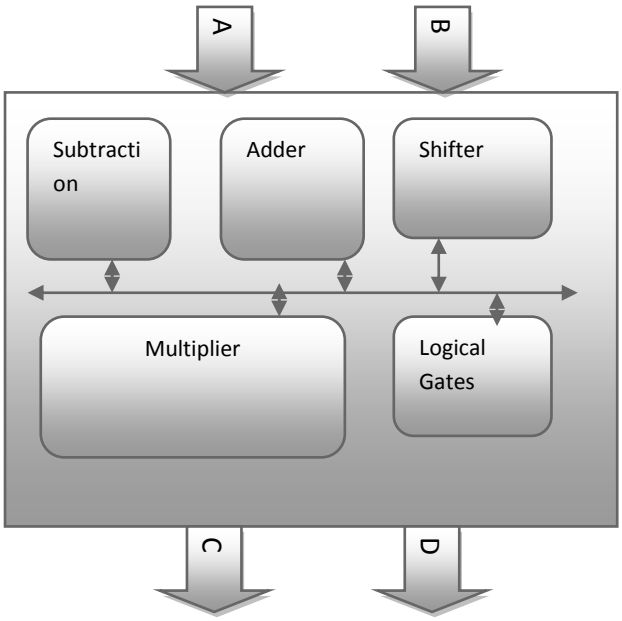

Figure 2: Arithmetic Logic Unit Module

Here the A and B are the two 16 bit inputs of proposed Arithmetic Unit. And other portion of the design includes Adder, Subtractor, Multiplier, and ALU. Product and Accumulated product are 32 bit output while differences, S are 16 bit output. Proposed work did not focus on the designing of the adder and subtractor circuits as these are not consider modules which consumes large amount of area and power in ALU. But after detailed study it is been found that normally, carry ripple adders can be used when it required to meet timing constraints because they are easy to build and compact.

4. RESULTS

Till now we have successfully new design for 4 bit Vedic multiplier with the help of new addition structure and also design 8x8 and 16x16 with help of 4x4 multiplication. Proposed work is a design of ALU with the help of modified new urdhava triyambakam Vedic multiplication method (i. e. proposed multipliers). After successful implementation 4x4, 8x8 and 16x16 an ALU is been design and Figure 3 below shows the simulation results for the ALU design modules and it shows the results for multiplication, addition and subtraction.

Table 1: results observed for design

Family : Vertex 4 FPGA Family	
Observed results for proposed vedic 4x4	
No of Slices	18
No of 4 input LUT	31
No of bounded IOBs	16
Logical Delay	4.891 ns
Observed results for proposed vedic 8x8	
No of Slices	90
No of 4 input LUT	158
No of bounded IOBs	32
Logical Delay	6.448 ns
Observed results for proposed vedic ALU 16x16	
No of Slices	452
No of 4 input LUT	803
No of bounded IOBs	68
Logical Delay	9.007 ns

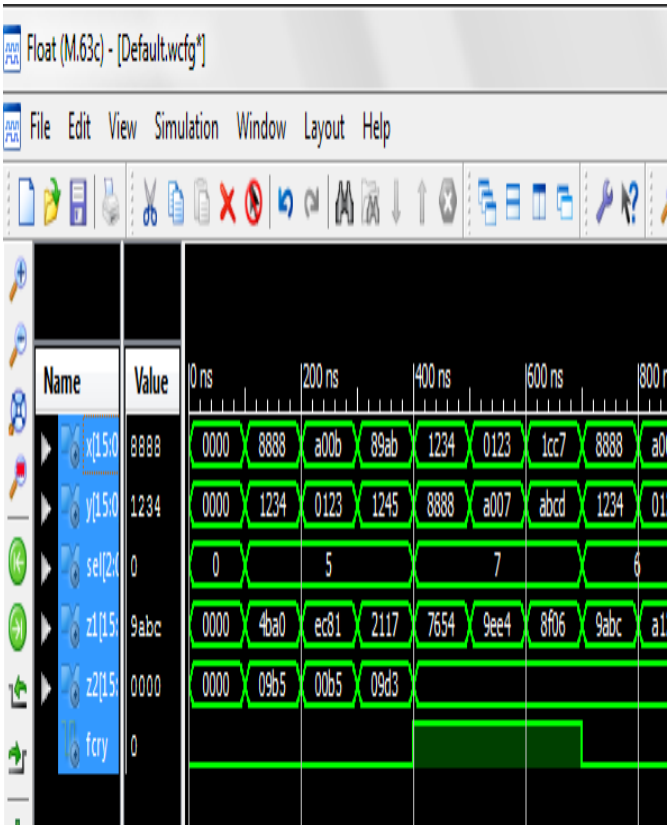

Figure 3: simulation results of ALU

The results are been produced after RTL entry in Xilinx EDA tool. Simulation is done on Xilinx ISE and results are been verified correctly.

Table 2: full comparative results

Platform used is vertex family FPGA			
Design	**Logical Delay**	**Slice**	**LUT**
Proposed Vedic 4 bit	4.891 ns	18	31
Base 1 (4x4)	8.387	19	-
Base 2(4x4)	-	-	-
Proposed Vedic 8 bit	6.448 ns	90	158
Base 1(8x8)	11.886 ns	-	-
Base 2(8x8)	15.685 ns	-	-
Proposed 16 bit	9.007 ns	452	803
Base (16x16)	15.718 ns	-	-
Base 2 (16x16)	23.064 ns	-	-
	Combinational path delay		
Proposed Vedic 8 bit	13.753 ns	90	158
Base 3(8x8)	13.753	-	-

Above it can observe that proposed work has batter results in aspect of area (i.e. less number of Slices) and speed (i.e. logical delay) in 4 bit multiplication as compare to base 3 paper.

Above one can easily observe that proposed work is batter in aspect of speed (i.e. logical delay) in 8 bit as compare to base1, base2 & base3 papers.

Proposed is a design of 4 bit Vedic multiplier (our actual research work) and use it to design 16 bit ALU. So one should make comparison with 4 bit Vedic only, rest of comparison are also been made.

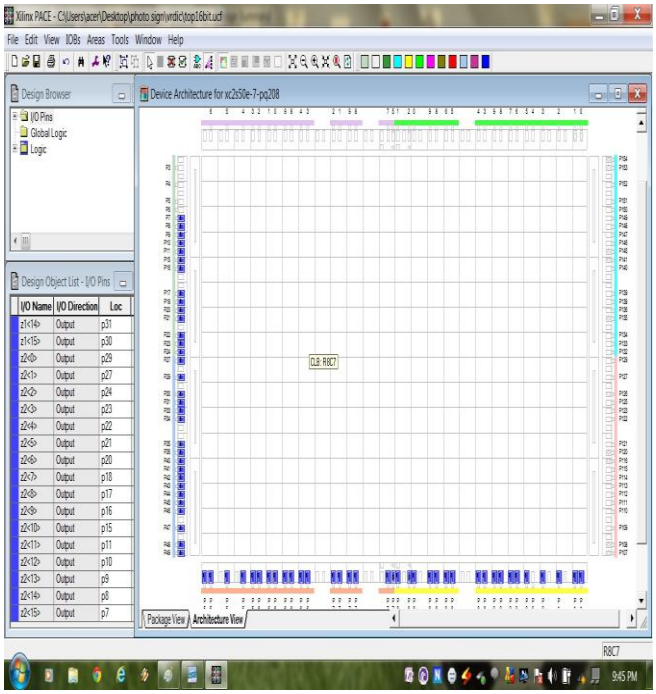

Figure 4: FPGA floor plan of proposed work

Figure 4 above is the floor plan of proposed work which is designed for generation UCF (user constrain file) for final validation of design on FPGA.

5. CONCLUSION

In this paper we proposed a novel architecture for the 16x16 bit Multiplier and a 16 bit ALU which provides somewhat better results as compare to the available Vedic multiplier or all other Multiplier. Proposed design can also be used for optimizing the multiply and accumulate unit of DSP. And so the optimum designs can be used for FFT, DFT, IIR, and FIR whose performance is dependent on the speed of ALU unit. There are so many applications where speed is more concerns than any other things like signal processing in satellite GPS based systems disaster management system etc. Proposed work give a solution for highly speed ALU and as know ALU is the key element part of software based embedded or general (i.e. computer) systems. The Future scope of this work can be extending for 32 bit, 64bit etc.

6. ACKNOWLEDGMENTS

The authors would like to thank faculties of ECE Department of IES College of Technology, Bhopal for their kind guidance and support.

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