Performance Analysis of Full Adder Circuit using Improved Feed through Logic

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ABSTRACT
In this paper performance analysis of full adder circuit has been carried out using improved feedthrough logic design technique which is a novel design technique. This technique is an improvement over already existing FTL. The circuit has been designed using existing high speed feedthrough logic and improved feedthrough logic in both 90nm and 180nm technology using cadence tools and a comparison has been done for power and delay. full adder circuit using improved FTL dissipates 37.9% less than full adder using high speed FTL but delay is increased by 15.13% but the overall power delay product is reduced by 28.5%.

Keywords
Feedthrough logic, high performance, logic design techniques.

1. INTRODUCTION
With the continuous decrease in feature size the transistor density is increasing day by day. Due to this power density in chip also increases which causes several problems and makes the power dissipation a major concern for the designers. Also with the increasing functionality and portability, speed of circuit is a main constraint[1][2]. To design a circuit with these constraints choice of logic design technique is very important. There are different logic design techniques available to designers. Different techniques have their merits and demerits. Static logic have low power dissipation but for complex logic its delay is high and area is large. Dynamic circuits have high performance as compared to static logic but there power dissipation is high. Domino logic is the most popular dynamic logic. It has high performance but also suffers from many problems such as charge sharing and use of inverter at every stage during cascading[2][3]. Feedthrough logic (FTL) solves the problem of domino logic but its power dissipation increases. In next sections feedthrough logic is explained and then full adder circuit is designed and analysed with high speed FTL and improved FTL.

2. FEEDTHROUGH LOGIC
Feedthrough logic is the logic design technique of the dynamic logic family. It was designed to overcome the demerits of domino logic such as charge sharing and use of inverter at every stage while cascading[4]. Conventional FTL is shown in figure 1. In this when clock is high then Tn is ON and Tp is OFF and output is discharged to zero. When clock is low then Tn is OFF and Tp is ON and output is either charged or discharged according to the inputs applied to PDN block. So in this unlike domino there is no transition from 1 to 0.

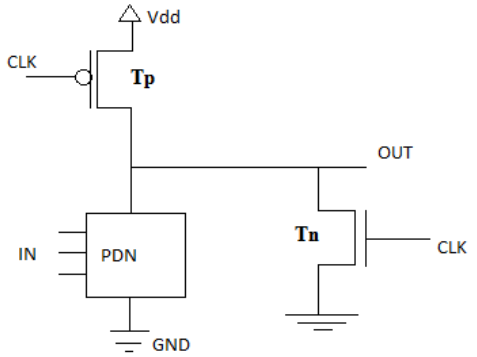

Figure 1: Conventional FTL

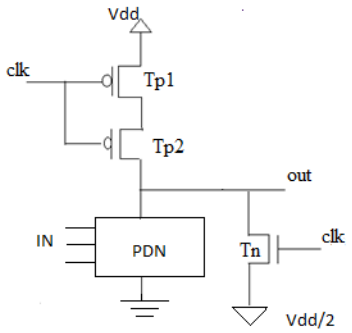

Figure 2 High speed FTL

Figure 2 shows the high speed FTL in which source of transistor Tn is connected to half of Vdd instead of ground. So when clock is high Tp1 and Tp2 are OFF and Tn is ON and output is charged to Vdd/2. When clock goes low then Tp1 and Tp2 are ON and Tn is OFF and output makes transition from Vdd/2 to low level or high level according to the inputs applied to PDN. In this technique transition is from Vdd/2 and not from zero so its speed is higher than conventional FTL[5,6].

3. IMPROVED FEEDTHROUGH LOGIC
Improved FTL structure is shown in figure 3. In this an additional transistor Tn2 is added between PDN and ground. In above high speed FTL when different stages are cascaded and clock is high then output node of each stage is at Vdd/2 which causes the transistors of next stage partially ON to which it is connected which causes power dissipation. Transistor Tn2 in improved FTL structure reduces this power dissipation.

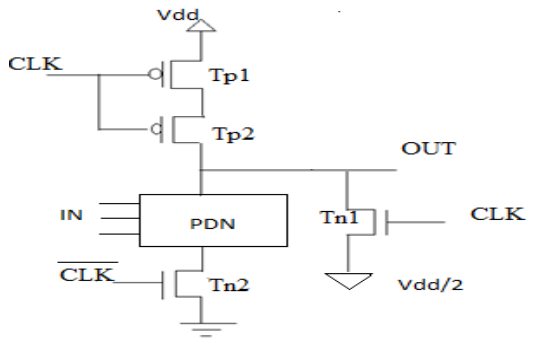

Figure 3 Improved feedthrough logic

4. SIMULATION RESULTS AND COMPARISON

A full adder circuit has been designed using high speed FTL and improved FTL in both 180nm and 90nm technology and is compared for power and delay. Figure 4shows 1-bit full adder circuit. Figure 5 shows the output waveform of full adder using high speed FTL in 180nm, figure 6 shows the output waveform of full adder using high speed FTL in 90nm, figure 7 shows the output waveform of full adder using improved FTL in 180nm and figure 8 shows the output waveform of full adder using improved FTL in 90nm technology respectively.

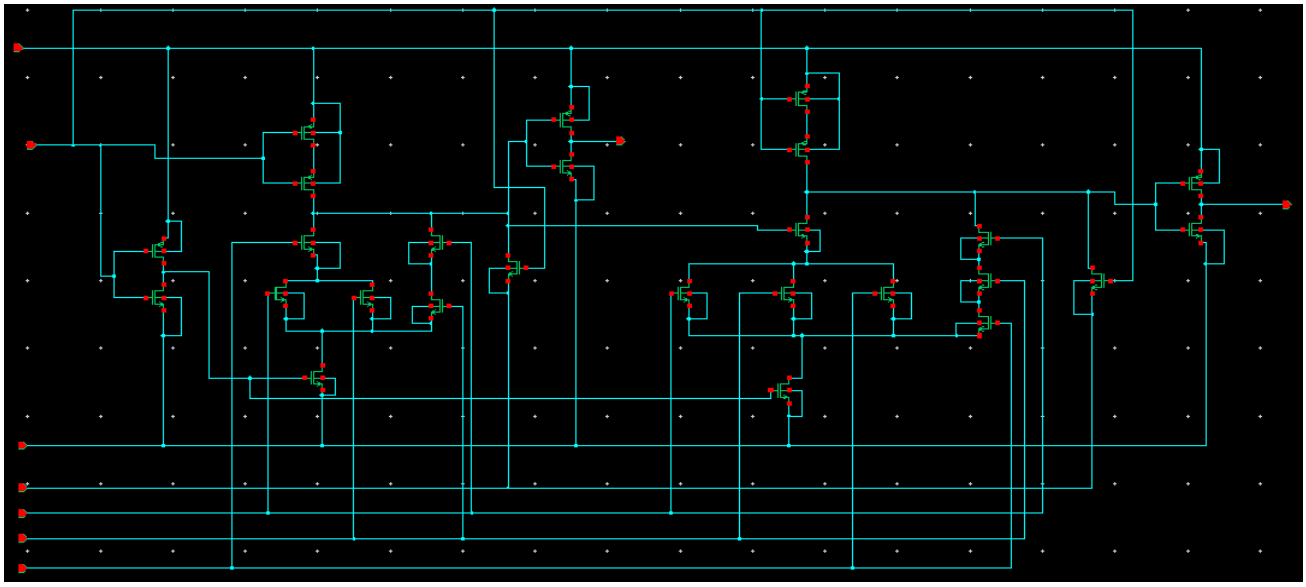

Figure 4 1-Bit Full Adder

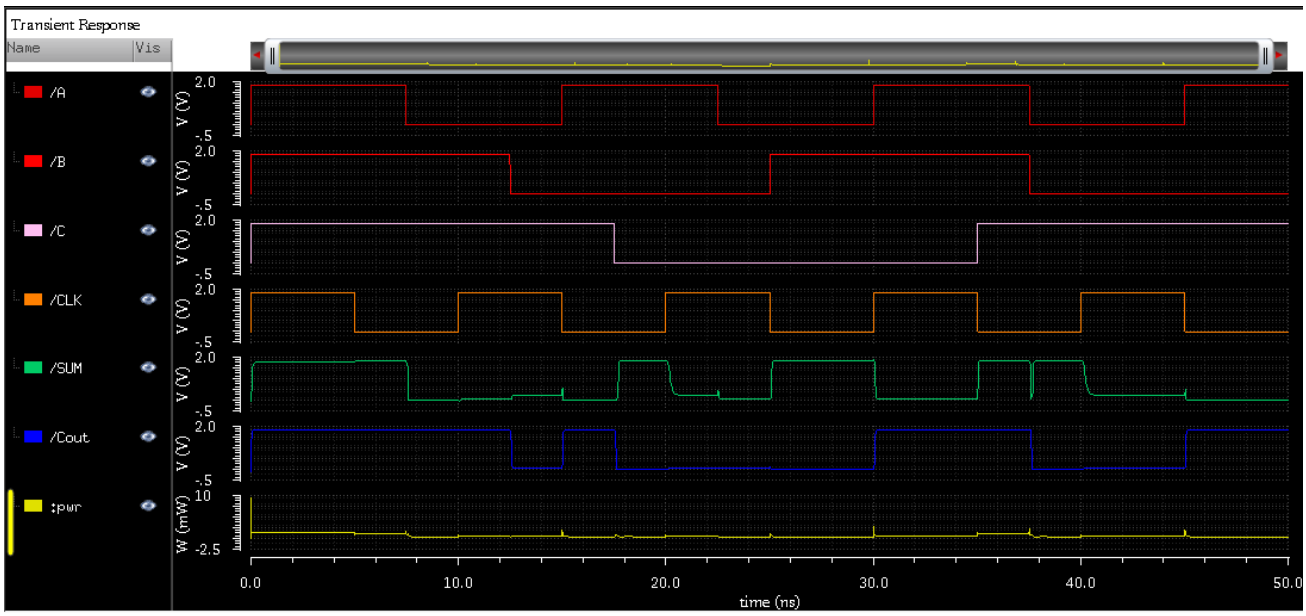

Figure 5 Output waveform for 1-Bit Full Adder using high speed FTL(180nm)

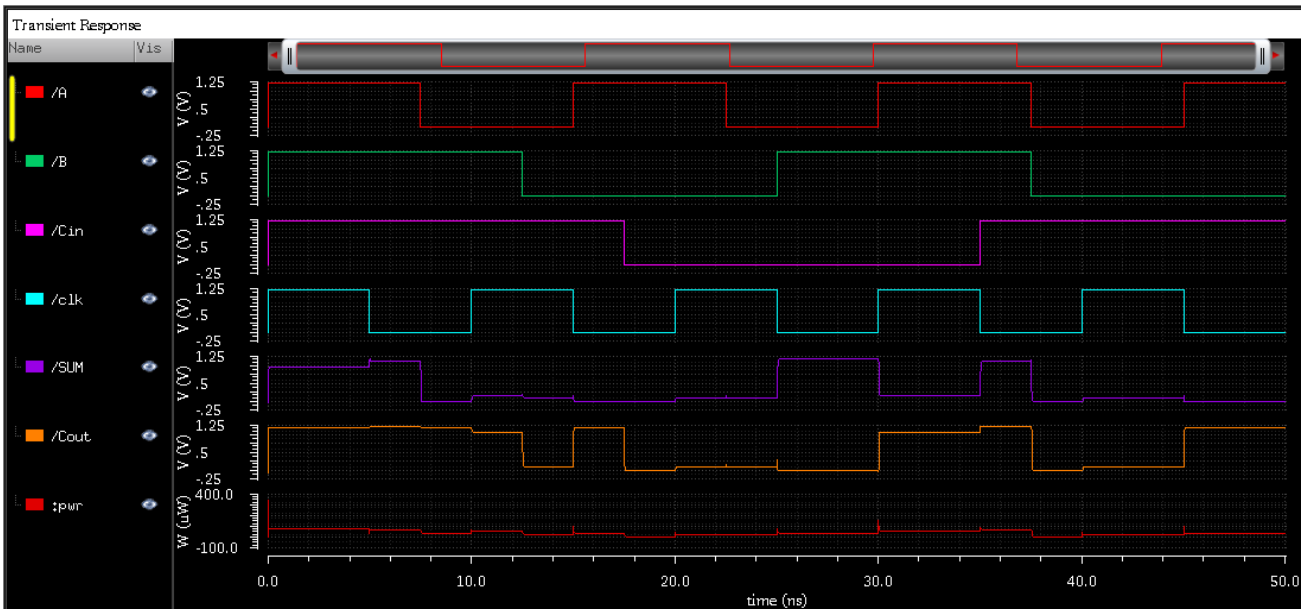

Figure 6 Output waveform for Full adder using high speed FTL (90nm)

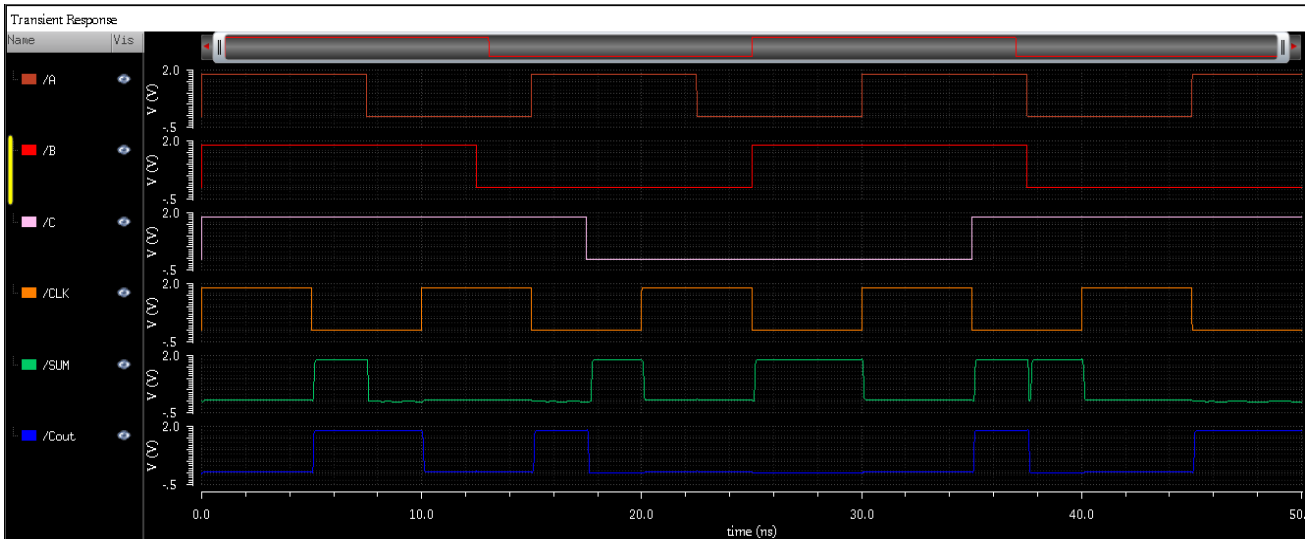

Figure 7 Output waveform for Full adder design using improved FTL(180nm)

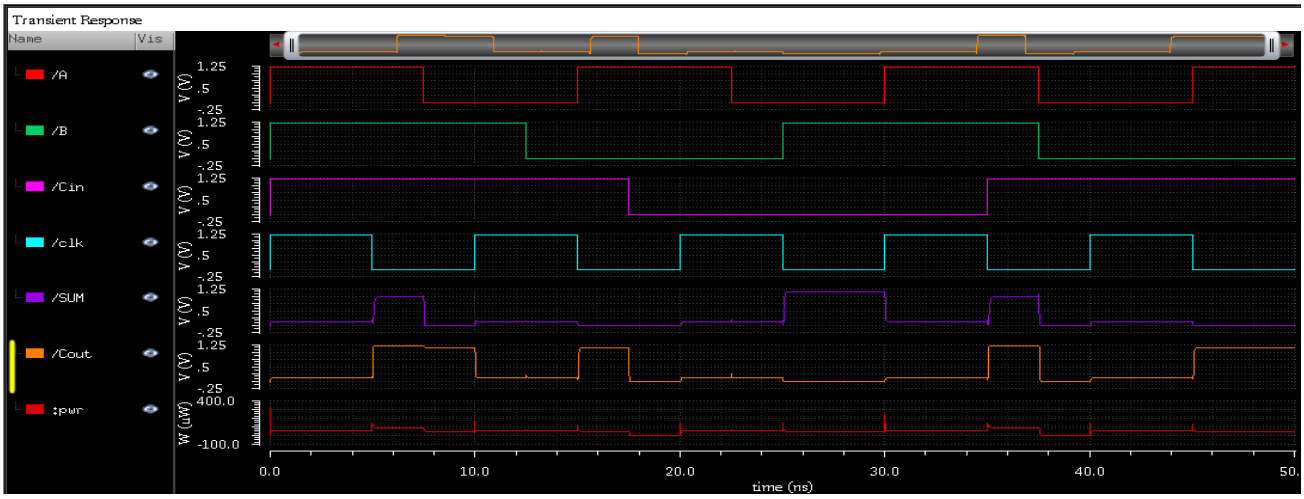

Figure 8 Output waveform for Full adder design using improved FTL(90nm)

Table 1 Comparison based on Simulation results for full adder (180nm)

Logic Family	Power (µw)	Delay (ns)	Power-Delay Product (PDP)(µw*ns)
High Speed FTL	684.8	0.2127	145.65
Improved FTL	424.8	0.2449	104.033

From table 1 we can see that for 1-bit full adder the improved FTL structure reduces the power dissipation of the existing high speed FTL by 37.9%. Delay is increased by 15.13% due to insertion of extra transistor. But the overall power delay product is reduced by 28.5%. So the improved FTL design technique is better than the existing high speed FTL.

Table 2 Comparison based on Simulation results for full adder (90nm)

Logic Family	Power (µw)	Delay (ns)	Power-Delay Product (PDP)(µw*ns)
High Speed FTL	41.96	0.015	0.667
Improved FTL	34	0.018	0.632

From table 2 we can see that power dissipation and PDP of full adder using improved FTL is less as compared to adder using existing high speed FTL. Adder using improved FTL has better performance than existing high speed FTL in both 180nm and 90nm technology.

5. CONCLUSION

We can conclude from the simulation results that the full adder circuit using improved FTL dissipates 37.9% less than full adder using high speed FTLbut delay is increased by 15.13% but the overall power-delay product is reduced by 28.5%. Performance of the improved FTL remain unchanged with change in technology also.

6. REFERENCES

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