

# Dynamic Current Mode Logic Realization of Digital Arithmetic Circuits

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## ABSTRACT

In this paper, we realize a high performance arithmetic circuits which is faster and have lower power consumption using a new dynamic logic family of CMOS and to analyze its performance for arithmetic circuits. This new dynamic logic family is known as Dynamic Current Mode Logic (DyCML). DyCML circuits combine the advantages of MOS current mode logic (MCML) circuits with those of dynamic logic families to achieve high performance at a low-supply voltage with low-power dissipation. A major advantage of the DyCML is the dynamic current source, which achieves smaller delays compared to the basic MCML circuits. Other advantages inherited from MCML are high performance and robustness to supply voltage scaling. DyCML gates reduce power dissipation by reducing the output voltage swing. We compare a set of arithmetic circuits implemented in Dynamic Current Mode Logic with the other dynamic logic styles. Simulation and test results show that DyCML circuits are superior to DDCVS logic styles in terms of power dissipation. A 2-bit multiplier, full adder & xor/xnor gate in DyCML style is fabricated in 180nm CMOS technology. 2-bit multiplier and a full adder dissipate 145.1  $\mu$ W and 55.14  $\mu$ W respectively at 40 MHz for a voltage swing of 1.2V in DyCML style.

## General Terms

Dynamic current mode logic, DDCVS and low power design.

## Keywords

CMOS integrated circuits, current mode logic, digital circuits, low-power integrated circuits and logic design.

## 1. INTRODUCTION

In VLSI design, low power design has become a critical issue, especially in high-density systems. In most digital systems switching power dominates the power dissipation. Switching power is calculated using the following equation:

$$P_{\text{switching}} = F_{\text{switching}} * V_{\text{dd}} * V_{\text{swing}} * C_L \quad (1)$$

Where  $F_{\text{switching}}$  is the switching rate of the logic gate output,  $V_{\text{dd}}$  is the supply voltage, and  $V_{\text{swing}}$  is the output voltage swing and  $C_L$  is the load capacitance including interconnect parasitic.

It is clear from equation (1) that if we reduce the supply voltage then switching power dissipation decreases most effectively. However, low supply voltage also results in performance degradation of the circuit. Another method to reduce switching power dissipation is to reduce the voltage swing, which is normally equals to the supply voltage.

Moreover in reduced swing logic circuits output swing voltage is lower than that of supply voltage. Thus we are able to reduce the dynamic power dissipation in more effective way, but the design of reduced swing logic circuits is more complex than full swing logic circuits because in reduced swing circuits some of the transistors are ON while the others are partially ON.

In this paper we realize the various arithmetic circuits using a novel logic family called Dynamic Current Mode Logic (DyCML) family. It combines both the noise-immunity and speed advantages of MCML circuits and dynamic logic families. DyCML achieves low power dissipation and high performance at low voltage. Dynamic current mode logic is an upgrade version of static MOS current mode logic (MCML) [1]. At the expense of reduced logic swing, MCML logic family is able to provide faster circuit with low power dissipation. However MCML logic circuits have static power dissipation due to the constant current source, which limits its use in digital circuits. MCML designs need to include a reference voltage distribution tree to control the current source of each gate, leading to larger chip area and more complex routing.

This paper is organized as follows. The next section outlines the architecture of DyCML circuits. Then its operation is introduced in section 3. Section 4 describes the implementation of DyCML logic & DDCVS logic to various arithmetic circuits and the simulation results. The following section presents the conclusion.

## 2. ARCHITECTURE OF DYNAMIC CURRENT MODE LOGIC

Dynamic current-mode logic (DyCML) was originally proposed by Allam and Elmasry as an upgrade version of static MOS current-mode logic (MCML). MCML logic family has the advantage of providing faster circuits at the expense of reduced logic swings. The differential pairs in the circuit are able to detect small input voltage variations. Since in general gate delays depend on the load capacitance, low swing operation is a suitable approach to reduce charge/discharge times. Moreover, the charging and discharging ability of MCML gates depend on different factors: charging the load capacitance is accomplished by the differential stage loads, while the load capacitance discharging will depend on the tail current source biasing the gate [2]. Thus, there is a power-delay tradeoff to take into consideration. Also, these gates present static power consumption, since one of the differential branches will be conducting.

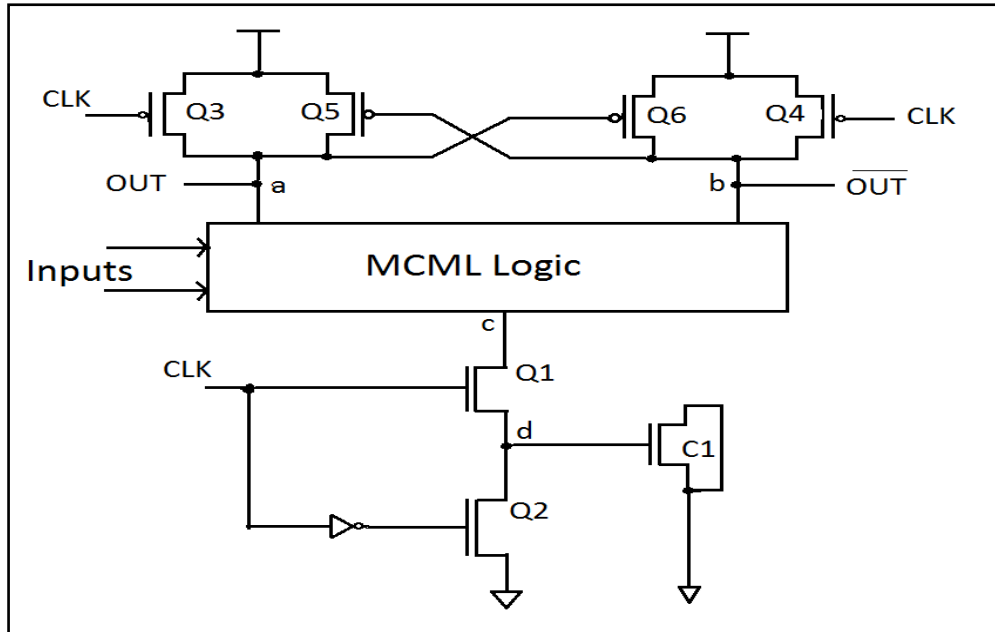


Fig 1 : Basic Architecture of DyCML

DyCML employs dynamic consumption and retain the fast response characteristics of MCML [3]. Since their introduction in 2000 as an US patent, there has not been significant work related to DyCML. DyCML is a reduced swing logic style, which was first proposed in order to decrease propagation delay in high performance circuit designs [4] and has, subsequently, been implemented successfully in various applications [5,6]. To achieve the high-speed characteristics of MCML, but exclude its drawbacks, the current source and load resistors of the MCML gate should be redesigned. Dynamic Current Mode Logic (DyCML) employs a dynamic current source with a virtual ground to eliminate the static power and other side effects associated with the conventional static current source [7]. The new architecture also utilizes active loads, instead of the traditional load resistors to reduce power dissipation. Figure 1 shows the basic architecture of a DyCML logic gate. It consists of the following: an MCML block for logic function evaluation, precharge circuit (Q2, Q3, Q4), dynamic current source (Q1, C1), and a latch to preserve logic value after evaluation (Q5, Q6). The operation of the DyCML is described as follows: during the low phase of the clock, the precharge transistors turn ON to charge the output nodes to  $V_{dd}$ , while transistor Q2 turns ON to discharge capacitor C1 to Gnd. Meanwhile, transistor Q1 is OFF, eliminating the dc path from  $V_{dd}$  to Gnd. During the high clock phase, the precharge transistors Q2, Q3, and Q4 turns OFF, while transistor Q1 switches ON creating a current path from the two precharged output nodes to the capacitor C1. The latter acts as a virtual ground. These two paths have different impedances depending on the logic function and inputs; therefore, one of the output nodes drops faster than the other node. The cross-connected transistors Q5 and Q6 speed up the evaluation and maintain the logic levels after evaluation. During the evaluation phase, when one of the output nodes voltage drops less than  $V_{dd} - |V_{TP}|$ , the transistor whose gate is connected to this node turns ON, charging the other output node back to  $V_{dd}$  [8]. Transistor C1 is used as a capacitor. It acts as a virtual ground to limit the amount of charge transferred from the output node(s).

The value of this capacitor is dependent on the value of the load capacitance (fan out), and the required output voltage swing. Since the charge stored on transistor C1 equals the charge drained from the output nodes, the following equations are used to calculate the size of transistor C1:

$$V_{swing} * C_L = W_{C1} * L_{C1} * C_{OX} * (V_{dd} - V_{swing}) \quad (2)$$

Where  $V_{swing}$  is the output voltage swing,  $W_{C1}$  and  $L_{C1}$  are the width and length of transistor C1 respectively,  $C_{OX}$  is the gate oxide capacitance per unit area, and  $C_L$  is the load capacitance per output node. The parasitic capacitances of the MCML block are included in  $C_L$ , as well as the gate capacitance of transistors Q5 and Q6, and the parasitic capacitances of the precharge transistors Q3 and Q4. Although the voltage of only one output node drops, a small current (charge) flows from the other output node to C1, until the latch switches ON. Thus, transistor C1 should be sized up to accommodate this extra charge.

Unfortunately, in Deep Sub Micron technologies (DSM), the interconnect capacitance grows up rapidly leading to higher load and, consequently, larger capacitor size. However, the increase in the interconnect capacitance is fairly compensated for by the increase in gate capacitance per unit area, which leads to smaller capacitor sizes. Therefore, the percentage increase in the capacitor size in DSM technologies is limited and is not expected to have a major effect on the logic gate size.

### 3. OPERATION OF DYNAMIC CURRENT LOGIC

Transistor Q1 and C1 construct a dynamic current source, which enhances the performance of the DyCML gates dramatically. The operation of the current source is described as follows: at the beginning of the evaluation phase, transistor Q1 acts as a current source with its gate biased with  $V_{dd}$ , driving a large current from the MCML block. As the current charges the capacitor, node d voltage starts to rise, limiting the current flowing through Q1 until it eventually turns OFF when it becomes zero. This large instantaneous current speeds up evaluation leading to a smaller delay. In DyCML circuits,

due to reduced output swing, dynamic power dissipation is small as compared to others differential logic circuits. Subthreshold leakage problem is eliminated by the latch connected transistors Q5 & Q6. DyCML circuit does not suffer from static power dissipation. Dynamic power is independent on the input combinations because after each precharge evaluation cycle, the voltage at one of the output node is  $V_{dd}$  while at other is  $V_{dd} - V_{swing}$ .

### 3.1 Cascading of DyCML gates

Cascading of DyCML gates can be done in two different ways:

- Clock delay (CD) mechanism where the clock signal is buffered from one gate to another
- Self-timing scheme where a gate generates the clock signal for the gates in the following logic level.

### 3.2 Clock delay scheme

Clock delay is a well-known scheme in dynamic circuits. The clock signal is delayed between cascaded gates by adding a buffer. A single clock buffer may be used to generate the clock signal feeding more than one gate. This is possible as long as the gates have equal logic depths. This scheme is the simplest and gives the best power and delay results. However, it must be clear that the CD should be larger than the gate delay.

### 3.3 Self-timed scheme

Self-timing requires each gate to generate a completion signal for the following logic level. In DyCML, this signal may be the voltage on the transistor/capacitor (node d in the DyCML gate schematic). A special buffer is used to convert this signal to a full swing signal to be used as the clock signal for the next block. Figure 2 shows the architecture of this buffer.

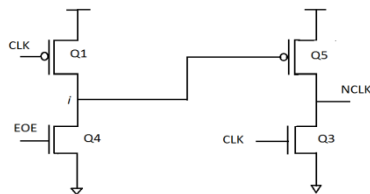


Fig 2 : Self-timed Scheme

It consists of a cascade of two clocked inverters. The PMOS transistor of the second buffer is removed to reduce the delay of the generated clock signal. The input to the first inverter EOE (the End of the Evaluation) is the voltage on the transistor C1 from the previous logic level. The buffer operates as follows: when the clock (CLK) is low, transistor Q1 turns ON, charging node  $i$  to  $V_{dd}$  which turns transistor Q5 OFF. Transistor Q3 turns ON and discharges the output node to "0." Since the transistor C1's gate is discharged to "0" and the clock is low, transistor Q4 turns OFF during this clock phase. When the clock signal becomes high, transistor Q1 turns OFF while transistor Q3 turns OFF. Until EOE input starts to rise, no current will pass from node  $i$  to the ground, keeping transistor Q5 OFF. When the input starts to rise, transistor Q4 switches on, discharging the node  $i$  to "0". Consequently, transistor Q5 turns ON to charge the output node to  $V_{dd}$ . Figure 3 shows the waveform for the self-timing buffer.

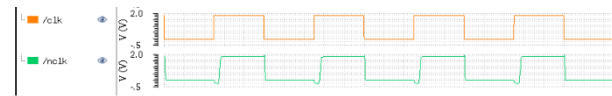


Fig 3 : Waveform for self-timed scheme

The ST clocking scheme is more appropriate for circuits with large variations in the operating conditions like supply voltage, temperature, etc. The reason is that each logic level will not start evaluation until the previous level has already evaluated, unlike the CD technique where the gate will start evaluation as soon as the delayed clock signal arrives. The price for the increased stability is higher delay, and power dissipation because of the buffers.

### 3.4 DyCML – CMOS interfacing

DyCML gates may be used in conjunction with CMOS gates in the same design. Inputs of DyCML logic may be connected directly to CMOS gates outputs. No buffering or interfacing circuits are required to connect the outputs of DyCML gates to the inputs of CMOS gates. A special buffer is required to convert the reduced swing signal to a full swing signal. Many differential single-ended buffers exist. Unfortunately, most of them are complex and they rely on a dc current bias. To take advantage of the presence of a clock signal in DyCML logic, a new conversion circuit is designed as shown in figure 4. It consists of a clocked inverter followed by a regular CMOS inverter.

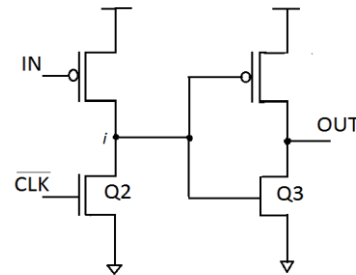


Fig 4 : Differential single-ended buffer

The operation of the buffer is as follows: when the clock is "0," transistor Q2 is ON, discharging node  $i$  to ground, and therefore, the output node becomes high. Since the DyCML gate outputs are precharged to  $V_{dd}$  when the clock is low, transistor Q2 is OFF. When the clock becomes high, transistor Q2 turns OFF. Depending on the input signal (the output of the DyCML gate), transistor Q1 will either turn ON, leading to a "0" output, or stay OFF, keeping the output at "1." To speed up the interfacing circuit, the voltage swing of the DyCML needs to be increased. This increase is required only at the gates driving the CMOS logic gates.

## 4. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

Now in this section, the designs of different arithmetic & logical circuits have been presented by way of their simulation results using DyCML. Further logic styles have been compared with DDCVS logic style. The parameter which is compared is the power dissipation at different clock frequency. For comparison, following circuits have been considered – xor/xnor, full adder and two bit multiplier. The simulations have been carried out using 180nm CMOS process flow in cadence virtuoso.

In the simulated waveform of XOR/XNOR in DDCVS logic style in figure 5, when the clock is low i.e. in precharge phase

the output waveform is low due to the inverter gate present at each output node. When clock is high, in the evaluation phase, the waveforms of XOR/XNOR verify the functionality of the gate. In the simulated waveform of XOR/XNOR gate in DyCML style in figure 6, when clock is low, in precharge

phase, output waveforms are high. When the clock is high, in evaluation phase, waveforms of XOR/XNOR verify the functionality of the gate. Figure 7 & figure 8 shows the simulation waveform of full adder in DDCVS & DyCML.

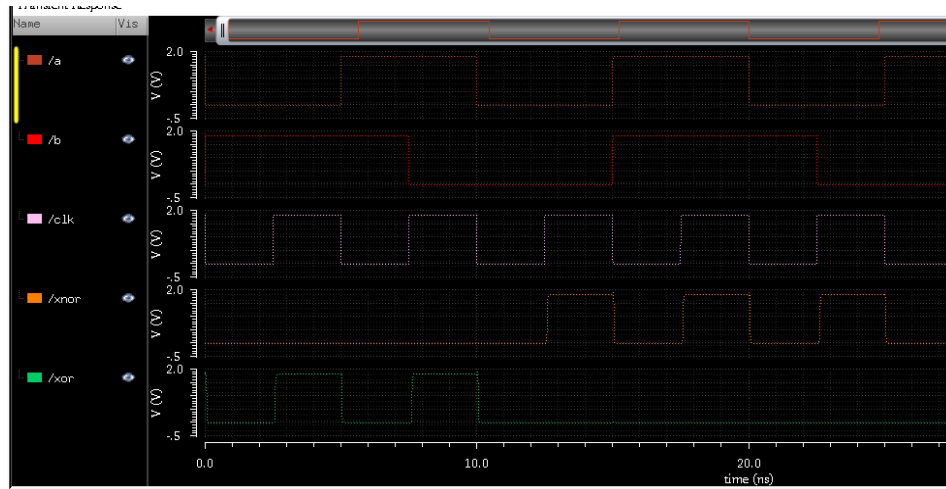


Fig 5 : Simulation waveform of xor/xnor gate in DDCVS logic

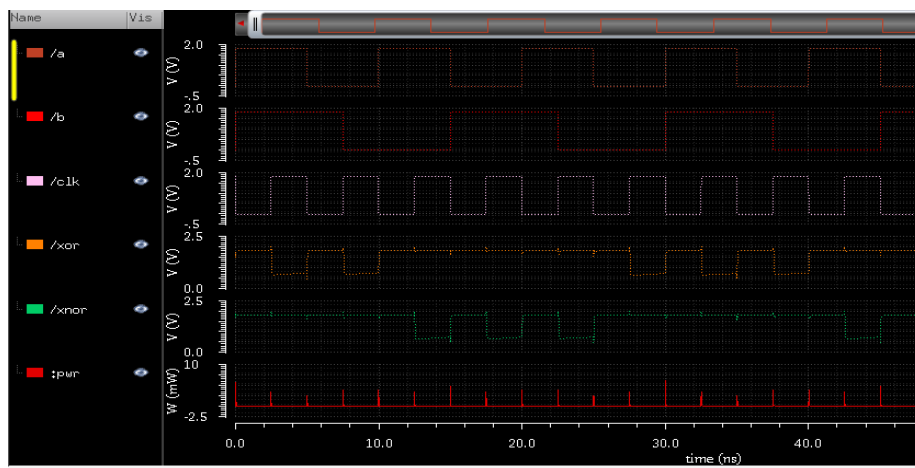


Fig 6: Simulation waveform of xor/xnor gate in DyCML.

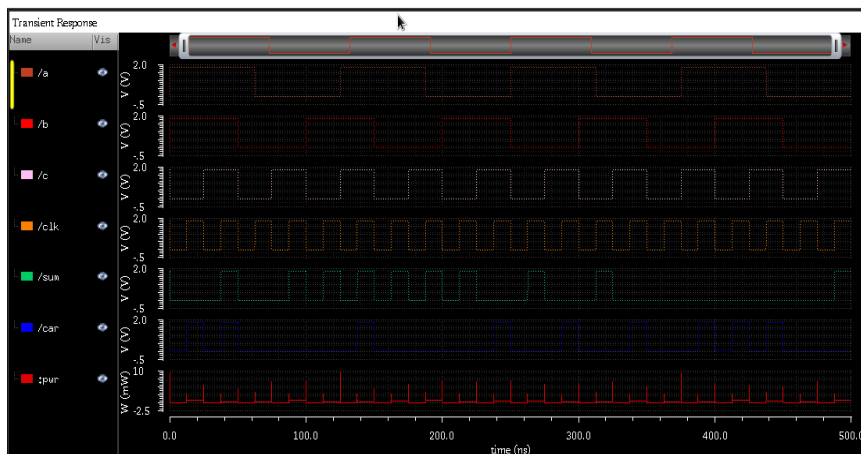


Fig 7: Simulation waveform of Full Adder in DDCVS logic.

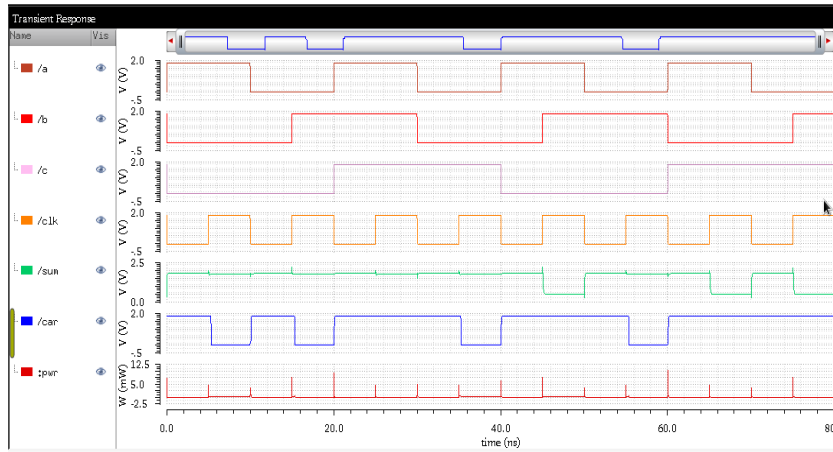


Fig 8: Simulation waveform of Full Adder in DyCML.

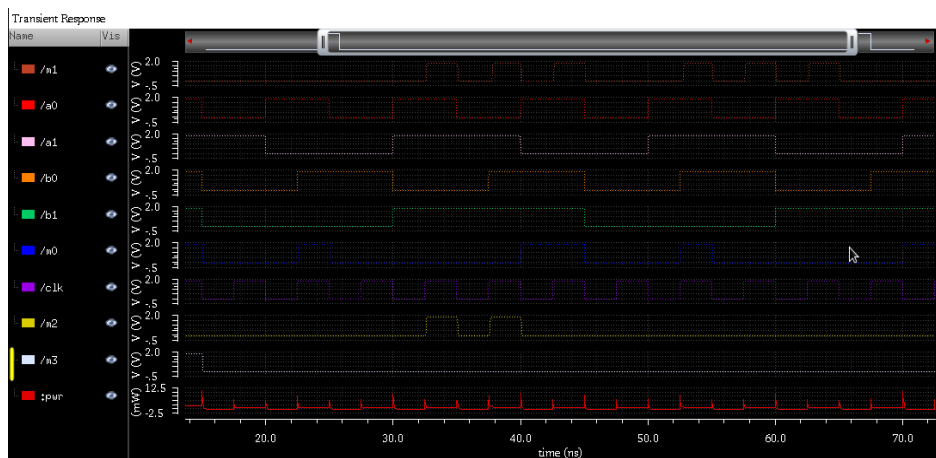


Figure 9 : Simulated Waveform of two-bit multiplier in DDCVS logic.

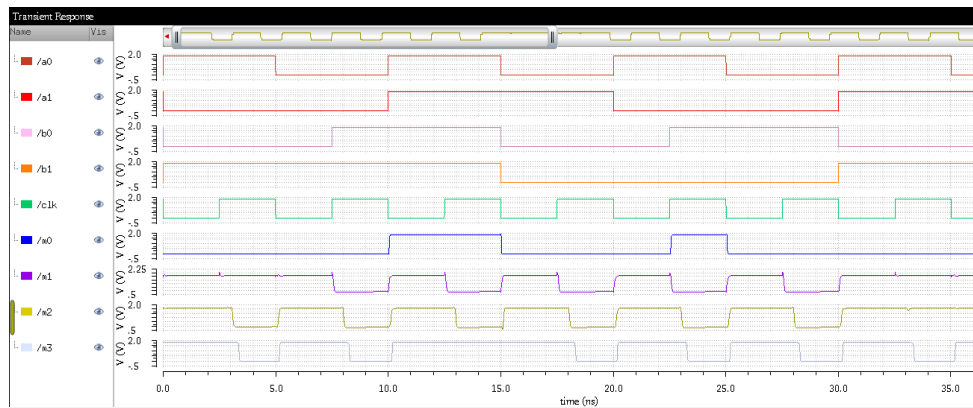


Fig 10: Simulation waveform of two-bit multiplier in DyCML style.

Similarly the waveforms of 2-bit multiplier in DDCVS logic & DyCML as shown in figure 9 & figure 10, respectively, verified the functionality of each gate. From the simulation results, total power dissipation of various arithmetic circuits at different clock frequency is presented in table 1. The simulations were executed at different frequency while the voltage supply was 1.8 V.

Table 1. Total power dissipation in various arithmetic circuits

Circuit	Clock frequency (MHz)	DyCML ( $\mu$ W)	DDCVS ( $\mu$ W)
Full adder	200	134.0	333.0
	40	55.14	307.3
	20	44.99	301.2

2-bit multiplier	200	367.8	584.2
	40	145.1	538.4
	20	123.2	527.8
Xor/xnor gate	200	33.75	34.68
	40	3.831	7.199
	20	3.635	3.704

From the simulation results, it is clear that DyCML achieves reasonable power dissipation at different frequency.

## 5. CONCLUSION

DyCML family combines the advantages of both MCML family and dynamic logic styles. A major advantage of the DyCML is the dynamic current source, which achieves smaller delays compared to the basic MCML circuits. Other advantages inherited from MCML are high performance, noise immunity, and robustness to supply voltage scaling. DyCML gates reduce power dissipation by reducing the output voltage swing. Simulation results show that DyCML circuits have low total power dissipation compared to the DDCVS logic styles. A full adder circuit in DyCML style has 82% and 85% less power dissipation at a clock frequency of 40MHz and 20MHz respectively as compared to DDCVS logic. Two bit multiplier in DyCML style has 73% and 76.6% less power dissipation at a clock frequency of 40MHz and 20MHz respectively as compared to DDCVS logic style. A 2-bit multiplier, xor/xnor gate & a full adder is simulated in Cadence Virtuoso (implemented using 180nm technology) to validate the simulation results. Simulation results show that DyCML circuits achieve low-power dissipation as compared to DDCVS logic.

## 6. REFERENCES

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