

# Design of 0.13um CMOS Two Stage Low Noise Amplifier

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## ABSTRACT

A Low Noise amplifier is one of the most commonly used components in analog and digital circuit designs. Low voltage and low power Low Noise amplifier design has become an increasingly interesting subject as many applications switch to portable battery powered operations. An electronic amplifier is an electronic device that increases the power of a signal. This design techniques is needed to allow amplifiers to maintain an acceptable level of performance when the supply voltages are decreased is immense for maintain low noise with high gain. The low-noise amplifier is a special type of electronic amplifier used to amplify very weak signals captured by an antenna. This paper presents a technique for substantially reducing the noise of a CMOS low noise amplifier implemented in the cascade inductive source degeneration topology. This 2.4 GHz Two Stage CMOS 130nm RF Low Noise Amplifier is optimize for low noise at low current with very low power consumption. In this proposed design work the two stage cascade low noise amplifier is used to achieve noise < 2dB with the high gain up to > 28 dB, input return loss of >10 and output return loss of > -10 at 1.3 supply voltage.

## Keywords

CMOS, two stage, cascode low noise amplifier, noise, gain and power.

## 1. INTRODUCTION

LNA is a key component, which is placed at the front-end of a radio receiver circuit whose noise performance decides the noise of entire receiver. Using an LNA, the noise of all subsequent stages reduces by the gain of LNA, while noise of LNA itself is injected into the received signal. So, it is necessary to boost the signal power while adding as little noise and distortion. Wireless applications are also define as battery powered devices. Power consumption is therefore a more important concern for the LNA. Various CMOS LNA topologies have been studied. Each topology has distinct advantages and limitations. There are several topologies for narrow band single ended LNA design; an appropriate Topology should be selected for low power and low voltage optimized LNA design. For Common gate topology, the gain is less with very low power consumption. For shunt series feedback common source topology, it is difficult to trade off among gain, less noise figure and good input/output matching with low power consumption. The topology which adds noise to the LNA because of the resistor thermal noise is resistor termination common source topology. Inductive degeneration common source topology achieves the specification in very low power consumption, but the isolation is not good enough compared to the cascade inductor source degeneration topology. With cascade inductor source degeneration topology

achieves similar low noise amplifier performance with very low power consumption. Compared to the above topologies the cascade inductor source degeneration topology provides higher gain with a low noise figure. However, since the achievable performances of the LNA is mainly limited by the CMOS transistors parameters and operating conditions, the selection and implementation of a design methodology, leading to the solution of several design problems. For LNA design, the gain, power, noise figure (NF), impedance matching, reverse isolation, stability, distortion and Power consumption has been derived to verify the design methodology.

## 2. LNA DESIGN OBJECTIVES

The objectives of our project are to develop a thorough understanding of low-power Low Noise Amplifier. In LNA design presents considerable challenge because of its simulations requirement for high gain, low noise figure, good input and output matching and unconditional stability at lowest possible current drawn from amplifier. This 2.4 GHz Two Stage CMOS 130nm RF Low Noise Amplifier is optimize for low noise at low current with very low power consumption. The LNA is capable of decreasing most of the incoming noise and amplifying a desired signal within a certain frequency range to increase the signal to noise ratio (SNR) of the communication system and improve the quality of received signal as well so that this design is widely applicable for Bluetooth, WI-FI, ISM band, Mobile phones and handset.

## 3. TECHNIQUES FOR LOW NOISE AMPLIFIER DESIGN

There were number of works are present on LNA design which shows how to achieve the as low as possible noise figure with higher gain. In this propose design we use inductive source degeneration common source topology; it helps to give very low noise figure and high gain. Following examples shows the previous work done on LNA design.

### 3.1 Low Noise Amplifier with utilizing $\pi$ -match and capacitive feedback input network

In this paper, an ultra low-power CMOS low noise amplifier (LNA) with a new input matching topology will be proposed and analyzed. The LNA design is based on the capacitive feedback in conjunction with a  $\pi$ -match network. The proposed LNA saves on chip area by using only one inductor for the input matching. The  $\pi$ -match network introduces an additional degree of design freedom and allows the LNA to achieve higher gain [1].

This paper proposed a new low power LNA scheme which reduced the number of inductor needed for input matching when compared to the L-CSLNA. The input matching is realized by the capacitive feedback scheme and  $\pi$ -match network. The LNA is designed for 2.4 GHz ISM band in a 130 nm RF-CMOS process. It achieves a gain of 25.2 Db with an S11 of -14 dB while consuming only 0.6 mW. The noise figure (NF) is 3.8 dB [1].

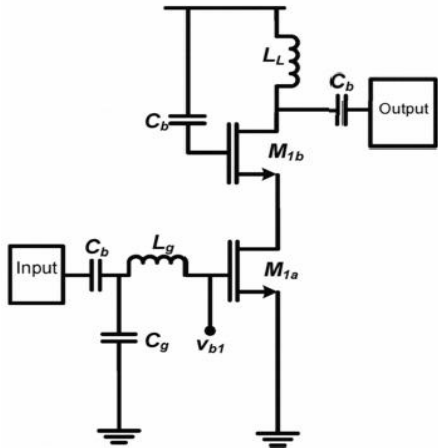


Fig 1 (a)

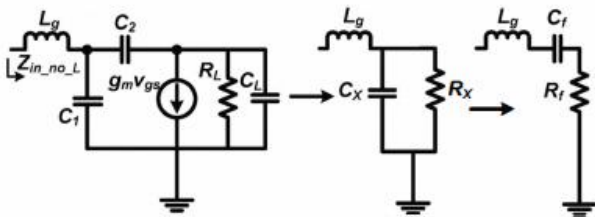


Fig 1 (b)

Figure 1 (a) Schematic of the proposed LNA (b) Equivalent small signal circuit of the capacitive feedback LNA [1]

### 3.2 A CMOS Low Noise Amplifier at 2.4 GHz with Active Inductor Load

A two stage cascode CMOS low noise amplifier (LNA) with an active inductor load is presented. On-chip active inductors require 90% less silicon area at a higher quality-factor. Comparison of measurement and simulation of an active inductor shows the high quality factor. Simulations of the low noise amplifier show the advantages of active inductors with similar performance even in regard to the noise figure [3].

This paper compares two LNA designs, one with spiral inductors only and the other one applying an active inductor load which resulted in a reduction of 25% of the required chip area without deteriorating significantly the performance.

The cascode stage with the transistor T3 is increasing the output resistance and therefore the lower cut-off-frequency is decreasing. To control the quality factor the transistor T4 is used in a regulated cascode structure. The disadvantage of active inductors is their poor noise performance compared with the passive counterparts because of the channel noise of the

transistors and their limited dynamic range. The simulated gain and noise figure are 19 dB and 2 dB respectively [3].

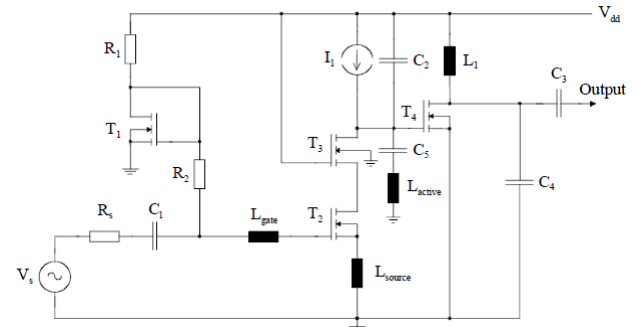


Fig 2 (a)

The first stage is a cascode stage. Figure 4 shows the noise and impedance matching of the input achieved with the two input inductors Lgate and Lsource [3].

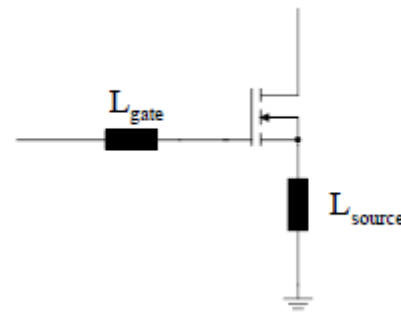


Fig 2 (b)

Figure 2 (a) Two stage low noise amplifier with active inductor (b) Noise and impedance matching with the input inductors Lgate and Lsource.

### 3.3 Low Noise Amplifier without Inductor Shunt-Shunt Topology

A common-source topology with resistive feedback in a shunt-shunt configuration as represented in Fig.4(a) is a compromise. For frequencies at which  $sCgs$  is negligible in comparison with  $gm$ , the input impedance is almost real and equal to  $1/gm$  and if  $gm$  is high enough it is possible to have the voltage gain and the input impedance dimensioned almost independently[8].

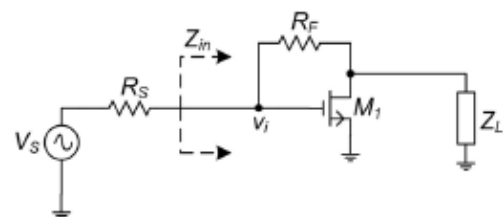


Fig 4 (a)

The LNA designed is the shunt-shunt topology represented in Fig.4 (b); it is a single-ended version of the LNA proposed in It can be divided in two main blocks: the amplifying block (M1, M4 and RD) and the feedback block (M2 and Rfb). M3 and M5 are used for biasing and to give extra circuit design variables, respectively. The amplifier block is a cascode stage with a resistance load, where both transistors M1 and M4 must operate in the saturation region. The gain of this stage depends mainly on gm1 and RD. A Cascode stage is used, to allow an extra degree of freedom in the design, together with M5 (the current in M1 can be increased without having a higher voltage drop in RD, which could put M4 out of the saturation region). The cascode also has other advantages such as higher gain, higher input output isolation and larger bandwidth. The feedback block is used to achieve the 50 Ω input matching. M3 is used to permit adequate biasing of M2 [8].

The result shows that a NF (Noise Figure) at high gain (16.5 dB) is 2.66 dB, the input referenced 1dB compression point (IP1dB) is about -21.8 dBm. This LNA consumes about 2.68mA current from 1.2 V power supply [8].

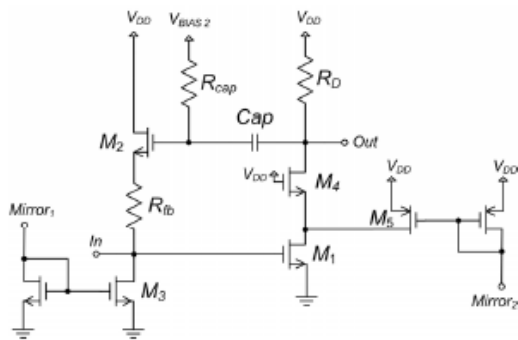


Fig 4 (b)

Figure 4 (a) LNA with resistive feedback (b) LNA Schematic

### 3.4 Proposed LNA with cascode inductive source degeneration topology

In this proposed design the two stage low noise amplifier (LNA) design with cascode inductive source degeneration topology presented.

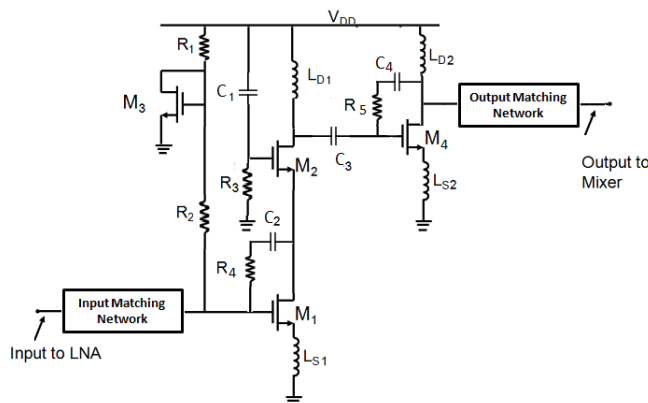
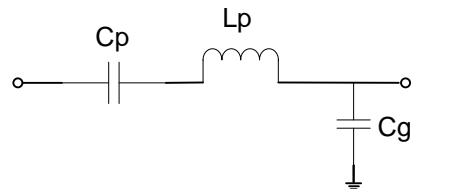


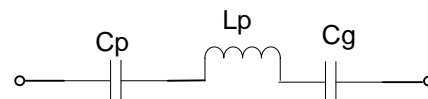
Fig 3 (a)

Now a day's all are looking for the low power consumption and to achieve the low power consumption CMOS is the best technology. Another advantage using CMOS technology is, it can be used for both analog and digital integration and it the cheaper technology. This Low noise amplifier is design on CMOS process. The important parameter will have to calculate are Gain (S21), Input return loss (S11), Output return loss (S22), Isolation (S12), Noise figure (NF) and linearity. Here the methodology followed is two stage LNA design. First stage is inductive source degeneration cascode topology and second stage is common source topology. For biasing of transistor (M1) use constant current source circuit and ratio of transistor are maintain to achieve the power consumption. Since the stability is the important parameter so, to maintain this in band and out of band stability voltage shunt feedback topology used here. The proposed LNA is for 2.4GHz, it was an narrow band response and to achieve narrow band response the inductive source degeneration cascode is used, this topology is also used to achieve the low noise and low power consumption. The first stage is basically for low noise figure and second stage is design for higher gain. The second stage is connected to the first stage by using the coupling capacitor (C3) there is not any inter stage matching is present and second stage the is stable with the help of same voltage shunt feedback topology. To make the narrow band response the low pass filter matching is used at the input and output side shown in fig 3 (b).

The proposed two stage Low Noise CMOS amplifier design with the help of complementary metal oxide semiconductor process on 130nm technology. Supply voltage is 1.3V which consumes power less than 5mW. This two stage cascode LNA has to achieved noise figure is less than 2dB and achieves a gain >28dB at the frequency of 2.4GHz. It is also having the good input and output return losses with the help of matching circuit.



(A)



(B)

Fig 3 (b)

Figure 3 (a) LNA architecture (b) Matching circuit

#### 4. COMPARISON AND DISCUSSION

Table 1

Parameters	Ref.Paper 1	Ref.Paper 2	Ref.Paper 3	Proposed Work
Technology	0.13um	0.5um	0.18um	0.13um
Supply Voltage	1V	3V	1.5V	1.3V
Frequency	2.4GHz	2.4GHz	2.4GHz	2.4GHz
Gain	25.2dB	19dB	19dB	> 28dB
NF	3.8dB	2.4dB	2dB	< 2dB
S11	-14dB	-10dB	NA	> -10dB
S22	NA	NA	NA	> -10dB
Power Consumption	0.6mW	NA	40.8 mW	< 5 mW

As we can see from the above comparison table the proposed 0.13um Two Stage Low Noise Amplifier provides high gain and low noise figure as compared to [1],[2],[3] LNA.

#### 5. CONCLUSION

Different methodologies for Low Noise Amplifier design has been seen above. It shows that 'Low Noise Amplifier has a differential pair' [1] and 'Low Noise Amplifier with Capacitive Feedback with  $\pi$ -matching Technique' [3] has better gain and noise. Proposed Low Noise Amplifier Circuit less power consumption than rest of the techniques. The proposed Low Noise Amplifier can provides high gain > 28dB and less Noise figure < 2dB at the expense of low power consumption

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