Comparative Analysis of Small Signal and Large Signal Parameters in Heterostructure Field Effect Transistors

Birinderjit Singh Kalyan
SVIET, Banur

Abstract
Heterostructure field effect transistors (HFETs) are based on AlGaN/GaN heterostructures which offer excellent electronic properties for the development of faster, heat-resistant , energy efficient transistors and application in microwave-power amplifiers [1,2]. The outstanding device performance in cut-off frequency, breakdown voltage, and device output power [3,4]. However, the comparatively analysis of small signal and large signal parameters which are seldom found in this paper.

Keywords
HFETs, organic chemical vapor deposition (MOCVD), two-dimensional electron gas (2DEG), E-Mode (Enhancement Mode), D-Mode (Depletion Mode)

Introduction
The basis for the development of a fast switch-mode GaN HFET is the semiconductor technology. On this level the fundamental properties of the transistor devices are determined. The whole technology process can be separated into three functional main parts: the epitaxy, the active device processing, and the technology for passives. These steps will be shortly described in the next sections with regard to their individual impact and restrictions on the final device properties and performance.

1. Epitaxy of the Heterostructure
The epitaxy was done on 3-inch semi-insulating SiC substrates by using metal organic chemical vapor deposition (MOCVD). The schematic cross section of the deposited layers for a full HFET epitaxy is depicted in Fig. 1. A thick buffer layer is necessary to reduce the defect and dislocation density and finally to realize an epitaxial layer with insulating properties. Afterwards an AlGaN barrier layer is grown, often followed by a thin surface protecting and surface stabilizing GaN cap layer on top of the final structure.

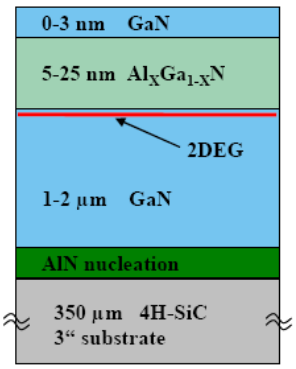

Fig 1: Schematic cross section of a conventional AlGaN/GaN heterostructure for HFETs

The inherent piezoelectric and spontaneous polarization and the band offset between AlGaN and GaN cause a triangular quantum well at the AlGaN/GaN interface in the GaN with a high electron concentration sheet charge (in the order of 1013 cm-2), the so-called two-dimensional electron gas (2DEG) [5]. The resulting band diagram for the conduction band and the electron distribution in the AlGaN/GaN heterostructure (including a GaN cap layer) is illustrated in Fig.1. GaN forms the channel layer, due to the electron distribution illustrated in Fig. 1. The electrical properties of the 2DEG, e.g., the sheet carrier density nS and mobility µ, are mainly influenced and adjusted by the thickness (dAlGaN) and Al content (xAl) of the AlGaN barrier layer. While the sheet carrier density is approximately increasing linearly with increasing Al content, the behavior of the sheet carrier density on the barrier thickness is nonlinear [6,7] is shown by equation below.

$$n_s(x_{Al}, d_{AlGaN}) = \frac{\sigma(x_{Al})}{q} - \left(\frac{\varepsilon_0 \varepsilon_r(x_{Al})}{q^2 d_{AlGaN}}\right)(\varphi_B + E_F - \Delta E_c + V_{ext})$$

2. HFET Small-Signal Equivalent Circuit
The model is based on two-port small-signal scattering parameter measurements (S-parameter, see appendix A1). A simplified small-signal model (Fig. 2) is used, which is derived from a more complex small-signal model for HFETs in common-source configuration shown by [8,9] The advantage of the simplified model is a direct calculation of the parasitic elements from the measured S-parameters.

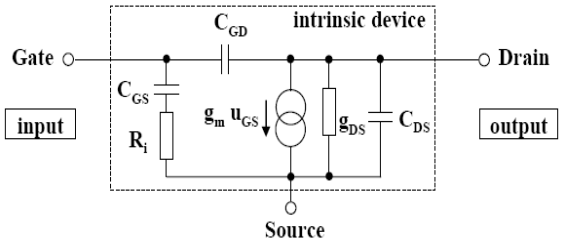

Fig 2: Simplified HFET small-signal equivalent circuit

The equivalent circuit of the model represents the physical parts of the transistor. Those are the output or drain-source capacitance CDS, the gate capacitance CG, which consists of the gate-source capacitance CGS and the gate-drain capacitance CGD, the gate series charging resistance Ri, which results from ohmic losses in the metal connections of the intrinsic gate capacitance, the channel/output conductance gDS, the transconductance of the current source gm and the gate delay time τi, which describes a frequency dependency of gm in the range of CGS. Ri.

The resistances of the source-gate RS and drain-gate RD access region (contact and semiconductor resistance) are additional parameters taken from DC measurements. They are in series connected externally to the drain and source contacts shown in Fig. 2. A sample of all model parameters with calculated current gain cut-off frequency fT is given in Table 1.

Table 1: Measured example of small-signal equivalent circuit parameters for a GaN HFET with a gate length of 0.25 µm and a gate width of 0.44 mm at a drain-source voltage of 7 V (at maximum gm).

f_T	g_m	g_{DS}	C_{GS}	C_{GD}	C_{DS}	τ_i	Ri
GHz	mS/mm	mS/mm	pF/mm	pF/mm	pF/mm	ps	Ω.mm
31	330	10.5	1.4	0.31	0.28	6.0	1.6

3. DC Measurement Results

In Fig. 3 shows the increase of the maximum transconductance gm_peak by the increased threshold voltage caused by gate-recess etching. The data point at the lowest threshold voltage for each curve represents the reference device without recess etching. The Enhancement mode behavior with Vth ≥ 0 V was found for both Al contents (22% and 18%), while the most positive values of Vth have be realized for an Al content of 18% in the AlGaN barrier. Here a very high maximum gm_peak of about 600 mS/mm was achieved at a threshold voltage of +0.5 V. While gm_peak was increased between 50% and 100% by the reduction of barrier thickness under the gate, the available drain current (at VGS = 2 V) is slightly degraded by about 15% at Vth = 0 V (Fig. 2).

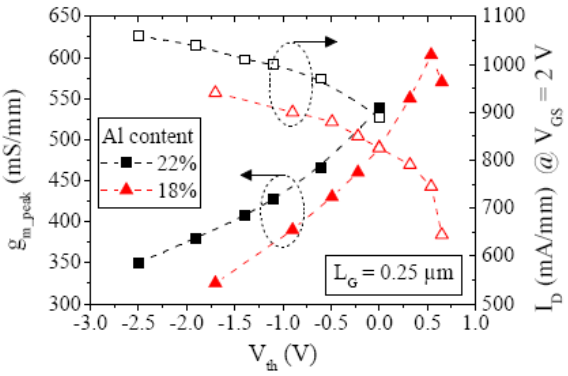

Fig 3: Measured impact of gate-recess shifted threshold voltage (Vth) on the peak transconductance (gm_peak) and maximum available drain current (ID at VGS = 2 V).

Nevertheless, the achieved current values are still very high. The required input voltage swing is decreased by a factor of 2 , an almost similar output current can be switched with this device. The origin of the high external transconductance for the gate-recess devices is the stable device on-resistance (Ron). The source and drain access regions are not influenced by the recess etching and remain in a low resistive condition given by epitaxy. The graph shows the behavior of Ron versus drain current (ID) for GaN HFETs with gate-recess (Vth = 0 V) and without gate-recess. The curves are derived from the output characteristics of both transistors.

For Vth > 0.5 V a strong deterioration of the maximum drain current and gm_peak occurs (see Fig. 2). The origin of this effect is the increasing gate leakage current in forward bias direction of the gate Schottky-diode. In principle this current is caused by the thin barrier layer itself, due to electron tunneling and thermally induced field emission of electrons. However, due to the trap assisted tunneling effect [10,11], the total current is amplified by defects in the barrier and at the barrier surface, which are always present and additionally caused by the etching process. By crossing Vth = 0 V from negative to positive Vth, the gate forward current increases dramatically. For Vth < 0 V no noticeable difference was observed between the recessed and non-recessed devices. However, for Vth > 0.5V the gate current becomes too high for a stable and safe device operation. Further measures have to be taken to improve the forward gate current issue for E-mode HFETs. The Fig. 4 shows the output characteristics of a typical device. However, depending on the application, the high gate leakage current in forward direction has to be reduced or the maximal available drain current has to be limited by the application circuit targeting an effectively low gate current.

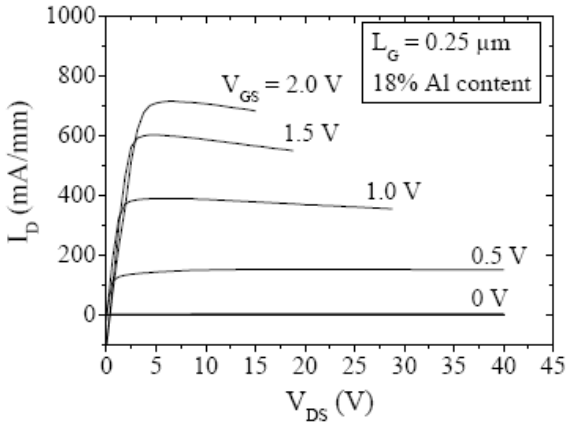

Fig.4: Measured output characteristics of a gate-recessed E-mode HFET with a gate length of 0.25 µm and an Al content of 18% in the AlGaN barrier.

Beside the forward gate current, the influence of the thin barrier and the etching process also deteriorates the reverse gate leakage currents. Therefore the breakdown voltage of the devices is reduced from a typical value of > 160 V for non-recessed devices, to about 80 V for the gate-recess HFET of the same gate length (0.25 µm).

4. Small-Signal Measurement Results

The reduction of the gate-to-channel distance by gate-recess etching improves the device speed due to an improved ratio between the intrinsic and parasitic HFET properties [14]. An improved intrinsic component leads to an increased device speed in general, which, e.g., increases the device speed scalability of the technology for reduced gate lengths. Measurement results showing this influence, based on recessed HFETs with an AlGaN barrier composition of 18% Al, are given in Fig. 5.

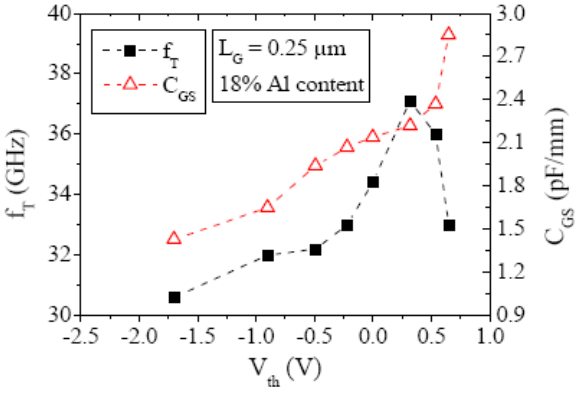

Fig. 5: Influence of threshold voltage shifted by gate-recess etching on the current-gain cut-off frequency (fT) and gate-source capacitance (CGS), measured at VDS = 7 V.

The reduced barrier thickness under the gate, which causes the positive threshold voltage shift, leads to an increase in the gate-source capacitance CGS. The impact of the parasitic gate capacitance is therefore effectively reduced, e.g., to < 30% for a CGS of 2.15 pF/mm at Vth = 0 V. Due to the simultaneously increasing transconductance, the current-gain cut-off frequency fT increases with increasing threshold voltage from 31 GHz to a maximum value of 37 GHz at Vth = 0.3 V. The maximum of fT occurs slightly below the maximum of gm_peak. The capacitance increases more than the transconductance, which is limited by the gate leakage. Beside the increase in fT, the transconductance improved by gate-recess also causes an increased small-signal gain MSG. Extracted from a device with a gate width of 2x250 µm and a gate length of 0.25 µm at VDS = 28 V, MSG increases constantly versus frequency (with k < 1) by about 1.8 dB for the gate-recessed HFET with Vth = 0 V compared to a non-recessed transistor.

5. Large-Signal Properties

To assess the large-signal power performance, large-signal continuous-wave power measurements were performed using a simulations are done at 2 GHz on transistor devices based on an AlGaN barrier with an Al content of 22%, a LG of 0.5 µm and a WG of 2x250 µm (Fig. 6). The transistors were biased at VDS = 28 V. For similar measurement conditions the gate voltage of the gate-recessed E-mode HFET (Vth = 0 V) was kept at 0 V, whereas the D-mode reference device was biased at VGS of -2.9 V. A linear gain of 22.5 dB (21 dB), a maximum power-added efficiency (PAE) of 68 % (70 %) and a maximum output power density of 4.6 W/mm (4.6 W/mm) were obtained for Enhancement mode (Depletion -mode).

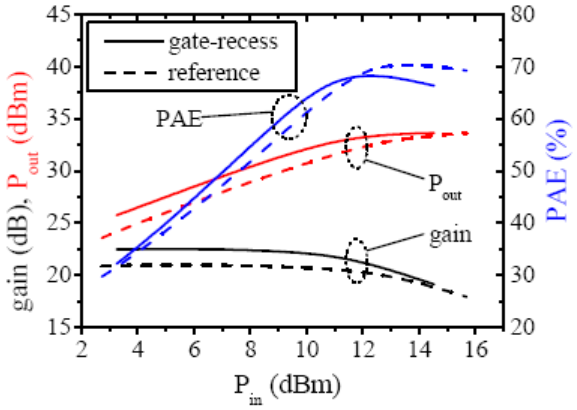

Fig. 6: Large-signal measurement at 2 GHz of a gate-recessed GaN HFET and a non-recessed reference device with gate width of 2x250 µm and a gate length of 0.5 µm (VDS = 28 V).

A gain increase of about 1.5 dB was observed for the E-mode transistor, similar as deduced from the small-signal measurements. The maximum Pout and maximum PAE of the recess-devices are not decreased because of the increased gm and gain. Further investigations on the forward gate current limitation have been done for devices with a more positive threshold voltage.

6. Results:

Table 2 summarizes these results. Two devices are compared with a threshold voltage of 0 V and 0.5 V, representing a high performance recess device and a device strongly affected by high forward gate leakage, respectively.

Table 2: Results of large-signal measurements of gate-recessed HFETs with different threshold voltages at 2 GHz.

V_{th}	V_{DS}	Gain	P_{OUT}	PAE
0 V	28 V	20.9 dB	4.8 W/mm	68 %
0.5 V	28 V	21.9 dB	3.5 W/mm	68 %
0 V	50 V	22.7 dB	8.0 W/mm	66 %
0.5 V	50 V	24.1 dB	6.0 W/mm	68 %

The measurements shown that the device with Vth = 0 V achieves a high output power density up to 8 W/mm at a bias of 50 V. The device with a deeper recess (Vth = 0.5 V) shows an improvement in linear gain of about 1 dB, independent of the output bias voltage VDS. However, the maximum available output power is considerably decreased, limited by the forwards current flow through the gate. High maximum power added efficiency is obtained for all devices. The large-signal properties achieved in this work are well comparable to the state of the arts shown by Liu et al. [12,13].

7. References

[1] R. Quay, *Gallium Nitride Electronics*, Berlin Heidelberg: Springer-Verlag, 2008.

[2] R. Quay, S. Maroldt, C. Haupt, M. van Heijningen, and A. Tessmann, "Gallium Nitride MMICs for mm-Wave Power Operation", *Frequenz*, vol. 63, pp. 51-54, 2009.

[3] M. Higashiwaki, T. Mimura, and T. Matsui, "AlGaN/GaN heterostructure field-effect transistors on 4HSiC substrates with current-gain cutoff frequency of 190 GHz", *Applied Physics Express*, vol. 1, p. 021103, 2008.

[4] E. Mitani, M. Aojima, and S. Sano, "A kW-class AlGaN/GaN HEMT Pallet Amplifier for S-band high power application", *European Microwave Integrated Circuits Conference (EuMIC)*, Munich, 2007, pp. 217-220.

[5] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures", *Journal of Applied Physics*, vol. 85, pp. 3222-3233, 1999.

[6] O. Ambacher, J. A. Majewski, C. Miskys, A. Link, M. Hermann, M. Eickhoff, M. Stutzmann, F. Bernardini, V. Fiorentini, V. Tilak, B. Schaff, and L. F. Eastman, "Pyroelectric properties of Al(In)GaN/GaN hetero- and quantum well structures", *Journal of Physics: Condensed Matter*, vol. 14, p. 3399, 2002.

[7] S. Maroldt, "Charakterisierung und Optimierung von AlGaN/GaN-Heterostrukturen für elektronische Bauelemente", Diploma Thesis, TU Ilmenau, Germany, 2006.

[8] M. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit", *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, pp. 891-895, 1990.

[9] B. Hughes and P. J. Tasker, "Bias dependence of the MODFET intrinsic model elements values at microwave frequencies", *IEEE Transactions on Electron Devices*, vol. 36, pp. 2267-2273, 1989.

[10] E. J. Miller, E. T. Yu, P. Waltereit, and J. S. Speck, "Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy", *Applied Physics Letters*, vol. 84, pp. 535-537, 2004.

[11] D. M. Sathaiya and S. Karmalkar, "A closed-form model for thermionic trap-assisted tunneling", *IEEE Transactions on Electron Devices*, vol. 55, pp. 557-564, 2008.

[12] J. Liu, Y. G. Zhou, J. Zhu, Y. Cai, K. M. Lau, and K. J. Chen, "DC and RF characteristics of AlGaN/InGaN/GaN double-heterojunction HEMTs", *IEEE Transactions on Electron Devices*, vol. 54, pp. 2-10, 2007.

[13] O. Toshihiro, K. Toshihide, K. Masahito, I. Kenji, M. Kozo, O. Naoya, J. Kazukiyo, and H. Naoki, "An over 100 W AlGaN/GaN enhancement-mode HEMT power amplifier with piezoelectric-induced cap structure", *physica status solidi (c)*, vol. 6, pp. 1365-1368, 2009.

[14] F. Schwierz and J. J. Liou, "RF transistors: Recent developments and roadmap toward terahertz applications", *Solid-State Electronics*, vol. 51, pp. 1079-1091, 2007.

Birinderjit Singh Kalyan is a completed Master in Technology (M.Tech) Microelectronics from University Centre for instrumentation and microelectronics (UCIM), Panjab University in 2009. He has worked in the area of ferroelectric memory modeling and design in post graduation and has published seven research articles in national and international journals and conferences. He had 4 year of experience in teaching and research work in the field of Microelectronics. Currently working at SVIET, Banur.