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A Study and Comparison of Low Voltage CMOS Current Multiplier

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ABSTRACT
A study and comparison between current mode CMOS analog multiplier, CMOS current mode multiplier/divider and high frequency four quadrant current multiplier has been carried out in this paper. Current multiplier has been simulated in SPICE with 0.35µm, 0.5µm. Simulation have been done with supply voltage of 3.3V, 1.5V and 1.55V respectively. The simulated results show that characteristic of multipliers are linear with 10µA, 10µA and 30µA input range respectively. These circuits are widely used for analog signal processing application.

1. INTRODUCTION
Multiplication of two signals is one of the most important operations in analog signal processing. The multiplier is not only used as a computational building block but also as a programming element in system such as filters, mixers, synthesizers, converter and modulators in communication systems. These are also important for non-linear analog signal processing functions finding application in adaptive filtering, modulation, fuzzy integrated system, frequency translation, automatic gain controlling and neural network [6]. Current multiplier can be designed either using transistor in linear region, in saturation region.

Main feature of standard CMOS fabrications are simplicity, low voltage operation, low power consumption and wide dynamic current range. In addition it is insensitive to temperature and process variation [7].

2. CIRCUIT DESCRIPTION

A. Low voltage current mode CMOS analog multiplier:

The principle of operation of the multiplier is based on the square-difference identity. There are three steps as shown in fig.1. and described as below:

Sum and subtraction both inputs.

Take the square of terms of first step and divided it by a constant current i.e. 4I.

Subtraction of second step with each other that output can be expressed as [5].

$$\frac{(X+Y)^2}{4I} - \frac{(X-Y)^2}{4I} = \frac{XY}{I} \qquad (1)$$

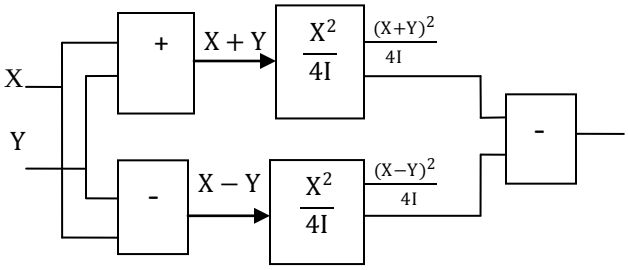

Figure 1: Current –Mode analog multiplier circuit

Current-mode squarer circuit based on the dual translinear loop. The circuit consists of two dual translinear loops. The first loop transistor Mp1 to Mp4 provides a (X-Y) input function to the squarer circuit provides output (X-Y) 2. The second loop transistor Mp6 to Mp9 provides a (X+Y) input function to the squarer circuit provides output (X+Y) 2 [6].

$$I_{01} = \frac{(I_x - I_y)^2}{4I_b} \qquad (2)$$

$$I_{02} = \frac{(I_x + I_y)^2}{4I_b} \qquad (3)$$

$$I_{out} = I_{02} - I_{01} \qquad (4)$$

Solving these equations we get:

$$I_{out} = \frac{I_x I_y}{I_b} \qquad (5)$$

Thus output current is directly proportional to Ix and Iy and inversely proportional to Ib. In this Ib is constant equal to 10µA [6].

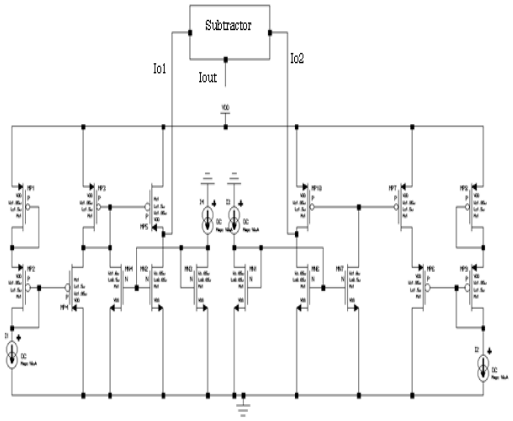

Figure 2: Current mode analog multiplier

B. Low voltage CMOS current-mode multiplier/divider:

The approach followed to implement the current mode multiplier will be the combination of geometric mean circuit and a squarer/divider circuit. Consider the following expression [7]:

$$I_z = \frac{I_x I_y}{I_w} \quad (6)$$

Where Ix, Iy, Iw and Iz being the current signals.

As shown in fig.3 output of squarer/divider circuit is

$$I_{out} = \frac{k\sqrt{I_x I_y}}{k^2 I_y} \quad (7)$$

I_z is output current so we can write as:

$$I_{out} = \frac{Iin^2}{k^2 Iw} \quad (8)$$

Hence output current is:

$$I_{out} = \frac{I_x I_y}{I_w} \quad (9)$$

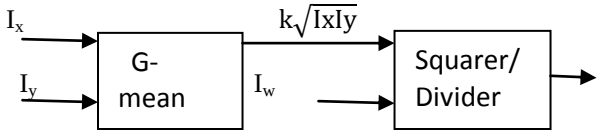

Figure 3: Current-mode multiplier/divider

Fig.4. shows the circuit implementation of current-mode multiplier/divider. It is based on forcing transition from triode region to saturation region and vice versa in transistor MN4, MN6, MN10 and MN12.Transistor MN2, MN8, MN10 and MN16 always operates in saturation, which can be done by properly choosing the cascade bias voltage Vcn. It will be assumed that the threshold voltage Vth of all NMOS transistor is same and that transistor MN2, MN8, MN10, MN16, MN4, MN6, MN12 and MN14 are matched, having the same transconductance factor β. Transistor MN1, MN3, MN5, MN7, MN9, MN11, MN13 and MN15 are also matched. Aspect ratio of MN1, MN3, MN5, MN7, MN9, MN11, MN13 and MN15 is n2 times larger than the aspect ratio of transistor MN2, MN4, MN6, MN8, MN10, MN12, MN14 and MN16, n being an integer greater than one [7].

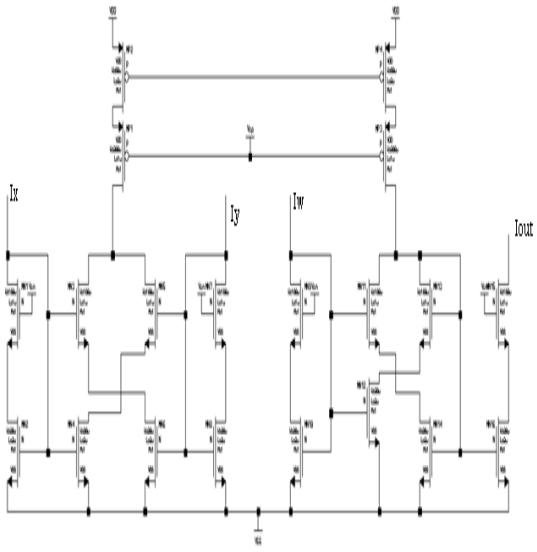

Figure 4: Current-mode multiplier/divider

C. High frequency four quadrant current multiplier:

Four quadrant CMOS current multiplier categorized into two groups: i.e. switched-capacitor approach and continuous time approach [4]. The multiplier based on switched capacitor approach has many disadvantages such as band limited signals and aliasing. So we will implement the circuit using continuous time approach. In this approach transistor could be biased in weak or strong inversion region. Generally transistor operates in saturation region because the square-algebraic identity can be easily realized [4].

Fig. 5. shows the four quadrant current multiplier. By using quadratic relation between the input and output currents we can find [4]:

$$I_2 = K[(b + a(I_x + I_y)]^2 \quad (10)$$

$$I_3 = K[(b - a(I_x + I_y)]^2 \quad (11)$$

$$I_9 = K[(b + a(I_x + I_y)]^2 \quad (12)$$

$$I_{10} = K[(b - a(I_x + I_y)]^2 \quad (13)$$

I2 is current across transistor Mn2, I3 is current across transistor Mn3, I9 is current across transistor Mn9, I10 is current across transistor Mn10.

I01 is combination of I2 and I3 and I02 is combination of I9 and I10

$$I_{01} = K\,[(2b^2 + 2a^2(I_x + I_y)\,2] \qquad (14)$$

$$I_{02} = K\,[(2b^2 + 2a^2(I_x - I_y)\,2] \qquad (15)$$

Output current is difference between the I01 and I02 and is given by

$$I\ out = I\ 01 - I\ 02 = 8Ka2IxIy \qquad (16)$$

Thus output current is multiplication of current Ix and Iy with multiplication gain factor determined by the transconductance parameter and the supply dependent parameter [4].

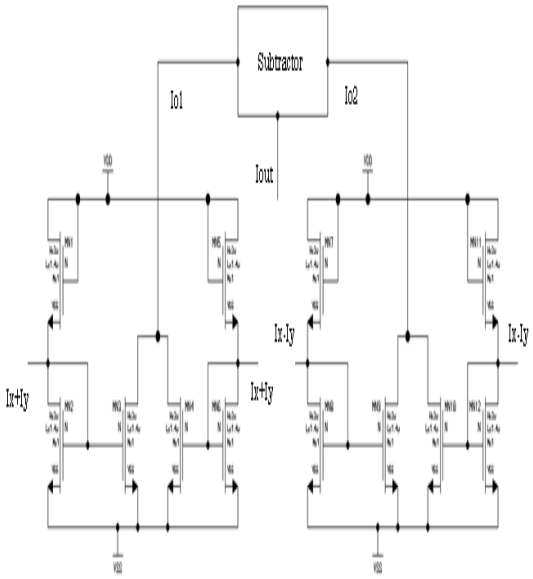

Figure 5: Four quadrant current multiplier

3. RESULTS AND DISCUSSION

The low voltage CMOS analog multiplier, current-mode multiplier/divider, high frequency four quadrant current multiplier have been simulated in SPICE with 0.35µm, 0.5µm and 0.5µm technology with supply voltage of 3.3V, 1.5V and 1.55V respectively. Table 1. shows the result of power dissipation, biasing current and current range of these multipliers. Table1. shows that power dissipation of low voltage CMOS current mode multiplier is less as compared to other circuit. Fig.6. shows that d.c. transfer characteristics of analog multiplier are linear with 10µA input range and input voltage is 3.5V. Fig.7. shows that d.c. transfer characteristics of current-mode multiplier/divider also linear with 10µA input range and input voltage is 1.5V. Fig.8. shows that d.c. transfer characteristics of high frequency four quadrant current multiplier is linear with 30µA input range and input voltage is 1.55V.

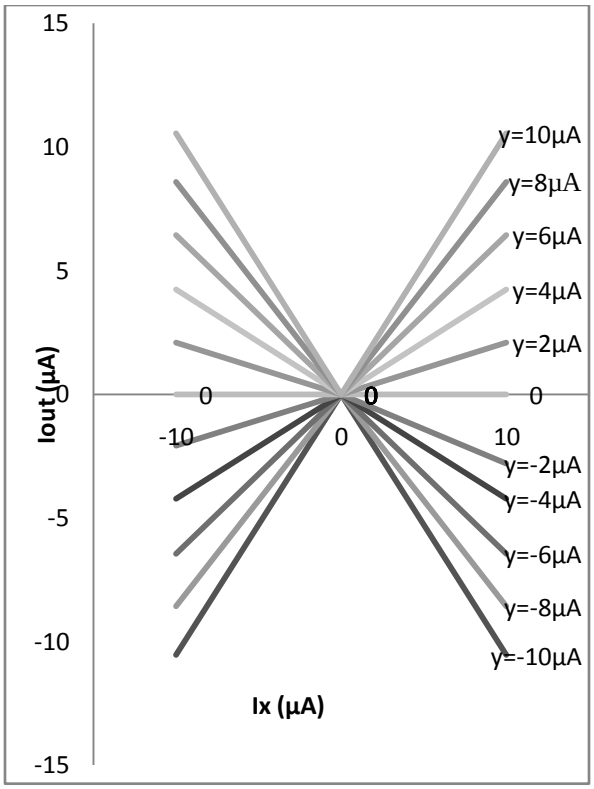

Figure 6: DC transfer characteristic of low voltage CMOS analog multiplier

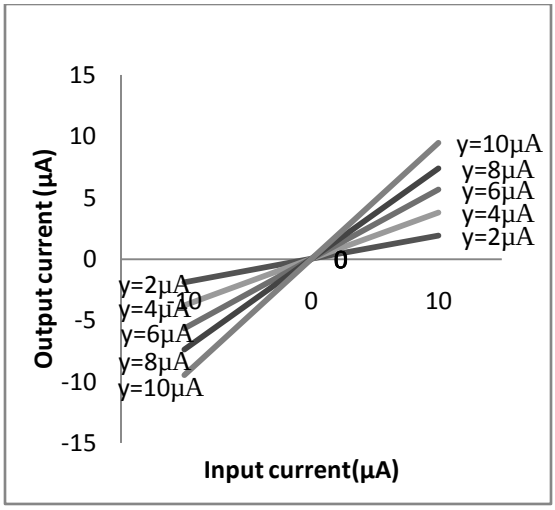

Figure 7: DC transfer characteristic of low voltage current mode analog multiplier/divider

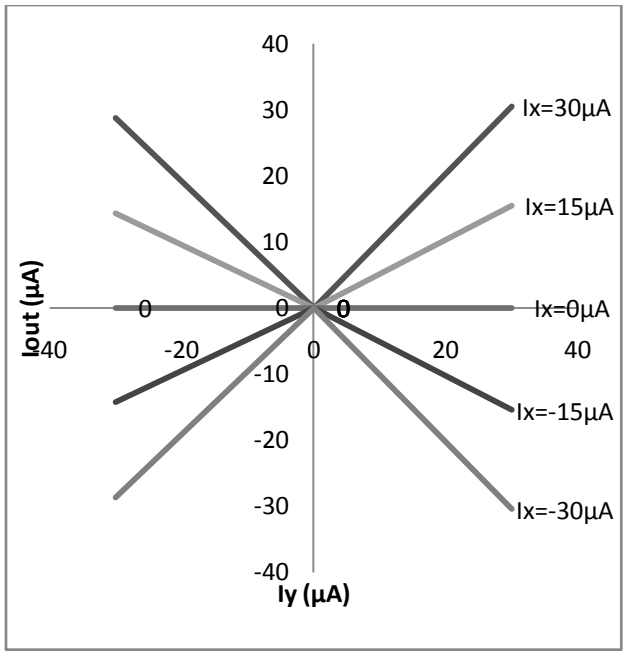

Figure 8: DC transfer characteristic of high frequency four quadrant current multiplier

Table 1: Comparison between multipliers

	Power Supply (V)	Bias Current (µA)	Power Consumption (µW)	Technology (µm)	Input Range (µA)
[6]	3.3	10	462.73	0.35	10
[7]	1.5	10	62.29	0.5	10
[4]	1.55	_	303.82	0.5	30

4. CONCLUSION

The low voltage CMOS analog multiplier, current-mode multiplier/divider, high frequency four quadrant current multiplier has been studied and simulated in SPICE with 0.35µm, 0.5µm technology with supply voltage 3.3V, 1.5Vand 1.55V. The d.c. transfer characteristics of analog multiplier are linear with 10µA input range and input. The d.c. transfer characteristics of current-mode multiplier/divider also linear with 10µA input range. The d.c. transfer characteristic of high frequency four quadrant current multiplier is linear with 30µA input range. It has been observed from the result that high frequency four quadrant current multiplier operates with higher input range and less input voltage as compared to the other circuits and from table it has been observed that power dissipation of current mode-multiplier/divider is less as compared to other circuits.

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