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Study and Simulation of CMOS Non-Sequential Phase Detector

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ABSTRACT
This paper presents the design of non-sequential phase detector using different XOR gates and compares the results with conventional circuit. Phase detector circuit has been modified using transmission gate logic XOR gate and 4T XNOR gate. The simulation results are focused on accounting the frequency operation and power dissipation of these phase detectors. The results shown in this paper are obtained using 0.35µm CMOS technology on SPICE simulator with 3.3V supply voltage.

1. INTRODUCTION
Phase locked loops (PLL) are most widely used for synchronization of clock phase, digital circuits and high performance microprocessor system [1]. The phase detector is the main part of the PLL and there is an increasing demand of high frequency operation PLL. The action of phase detector enables the phase differences in the loop to be detected and the resultant error voltage to be produced. A phase detector can monitor the difference between input data frequency and the voltage controlled oscillator output and generate an up signal if input data leads the clock output of VCO and a down if input data lags the clock [2]. The most desirable feature of a phase detector is to have zero dead zone, which is responsible for increasing phase noise. Dead zone occurs when the phase detector will not able to detect any phase error when the phase error is present. Various types of phase detector described in literature which are applicable for random data applications. The Hogge's [3] and Alexander [4] phase detectors have been most widely used. There are some performance limitations in these sequential phase detectors. Here, in this paper modification in non-sequential circuits has been done with transmission gate logic XOR gate and 4T XNOR gate. Further, different phase detectors are compared with its phase characteristics and power dissipation. Rest of paper is

organized as: In section II the structure and operation of phase detector with complementary pass transistor logic (CPL) is explained. In section III the modifications have been proposed with XOR and XNOR gates. In section IV the results have been described. Finally the conclusions have been drawn in section V.

2. STRUCTURE AND OPERATION
Number of stages in the VCO determines the structure of phase detector. Phase detector with even number of stages [5] in VCO is shown in figure 1. A ring oscillator type VCO is used with even number of delay cells, whose clock mid signal is taken directly in phase detector as shown in figure 1.

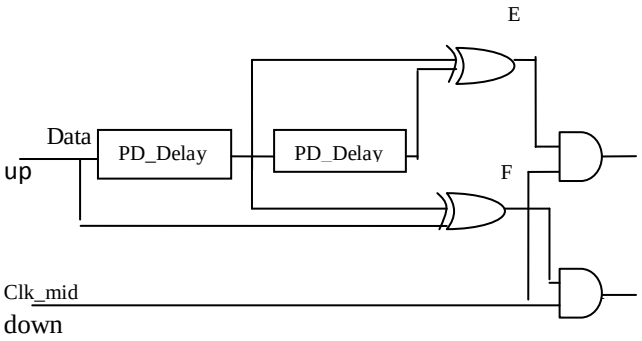


Figure 1: Phase Detector based on VCO even number of stages.

The phase detector operates with non-sequential circuits and uses only 2 XOR gates, 2 delays and 2 AND gates [5]. The phase detector operates by generating two references from the data, E and F. Reference E is generated by the XOR operation of the data and data_delay1, reference F is generated by the XOR operation of data_delay1 and data_delay2 [7]. After generating E and F, an "AND" operation is applied between E, F and A. A is the clk_mid signal taken from the even stage of VCO. Result of the "AND" operation gives the UP and DOWN signals which are required to drive the charge pump.

2.1 Delay Cell
Two delay cells have been used in the phase detector [5]. Simply, delay is provided by using a number of inverters connected in series. Delay time requirement can be easily varied and controlled by using this configuration of delay. Figure 2 shows the delay cell using six inverters.

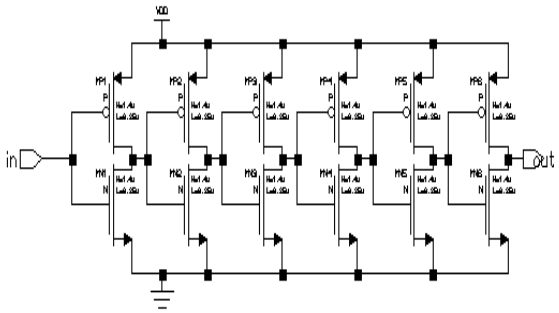
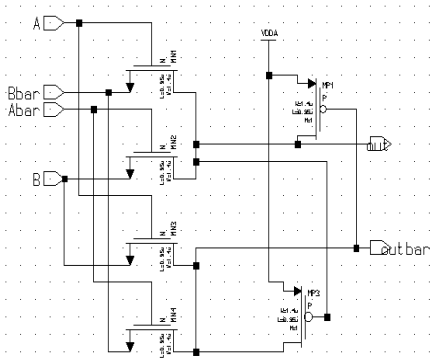


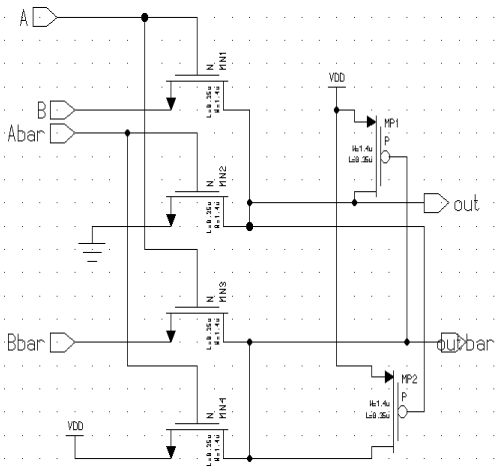
Figure 2: Delay Cell

2.2 CPL Gates

To implement CPL XOR and AND gate there are six transistor used in each, 4 NMOS and 2 PMOS transistors [5]. Complementary signals are present at the both input and output of each logic gates. The use of complementary pass transistor gives the reduction in the parasitic capacitances. Figure 3(a) & (b) shows the CPL XOR and CPL AND gates.



(a)



(b)

Figure 3 (a): CPL XOR (b) CPL AND gates

2.3 Implementation of Phase detector using CPL

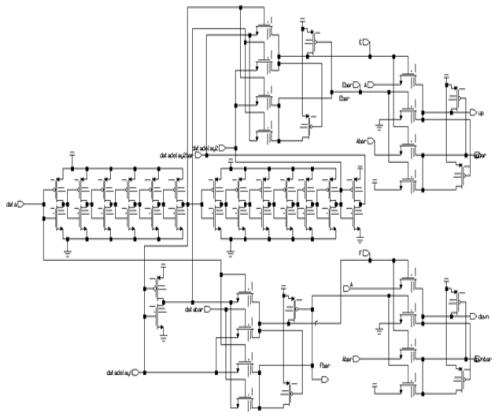


Figure: P: Phase detector using CPL

3. IMPLEMENTATION OF MODIFIED PHASE DETECTOR

To achieve the good speed of operation, the selectivity of XOR and AND gates should be impressive. To implement the phase detector in two different forms, we use here XOR gate using transmission gate logic (TGL) and 4T XNOR [8] gate. In both types the structure of "AND" gate is implemented by CPL.

3.1 Tgl Xor Gate

The process complexity of transmission gate logic is less as compare to complementary pass transistor logic. Figure 4 shows the schematic of TGL XOR gate.

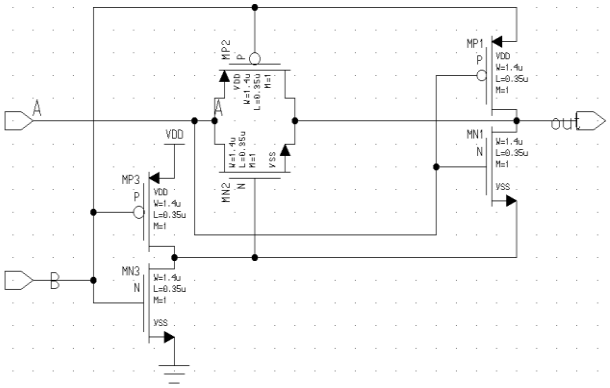


Figure 5: TGL XOR gate

3.2 4T XNOR Gate

To reduce the number of transistors, 4T XNOR gate has been used. XNOR gate uses only 4 transistors [8]. Figure 5 shows the schematic of 4T XNOR gate.

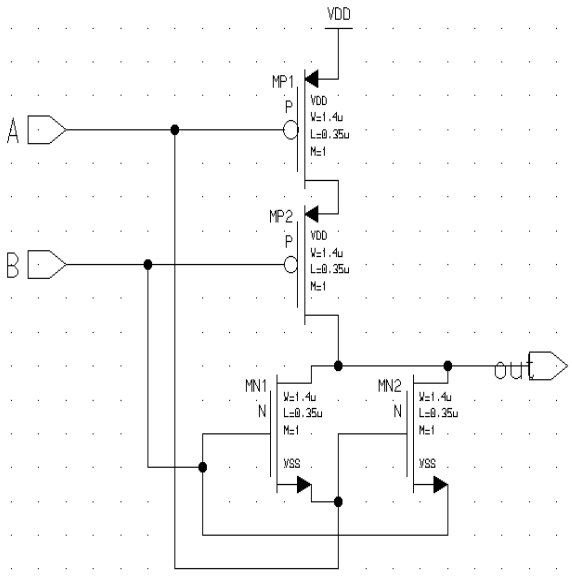


Figure 6: 4T XNOR gate

3.3 Implementation of Phase detector using TGL

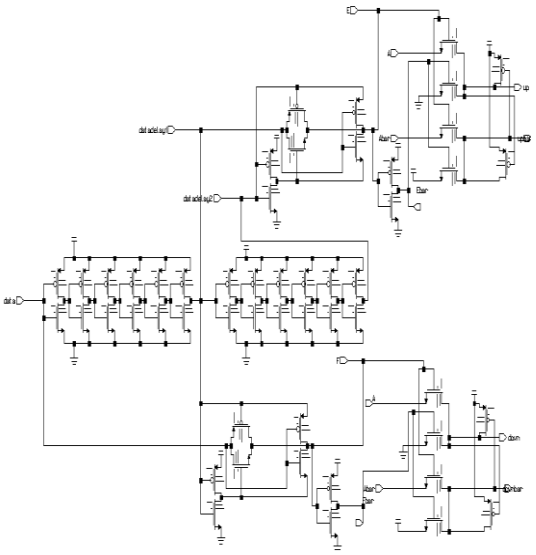


Figure 7: Phase detector using TGL

3.4 Implementation of Phase detector using 4T XNOR gate

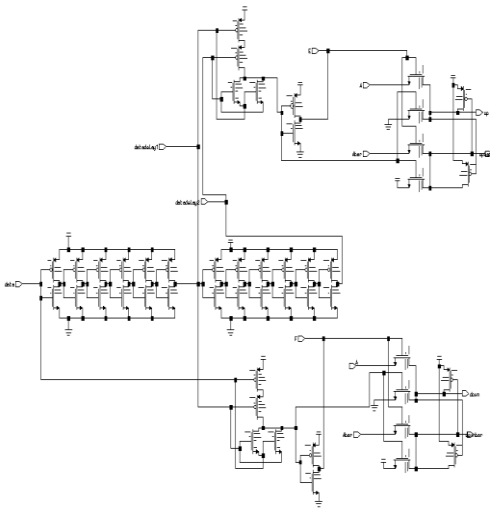
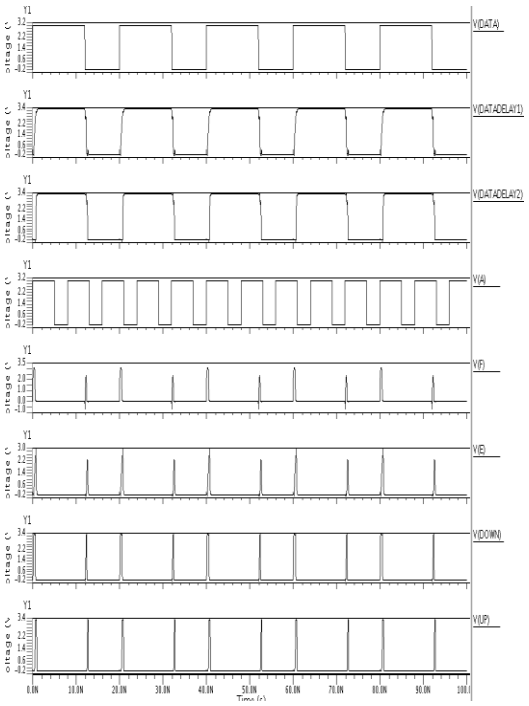


Figure 8: Phase detector using 4T XNOR

4. SIMULATION RESULTS

Phase detector using three different logic circuits has been simulated and studied in 0.35µm standard digital CMOS technology. The output waveform of each phase detector is shown in figure 9. In each waveform input data pattern "110110…." is given with frequency of 45 MHz. Maximum operating frequency for CPL_PD, TGL_PD and 4T XNOR_PD when VDD = 3.3V are observed as 2 GHz, 1 GHz and 1 GHz.

(a)



(b)

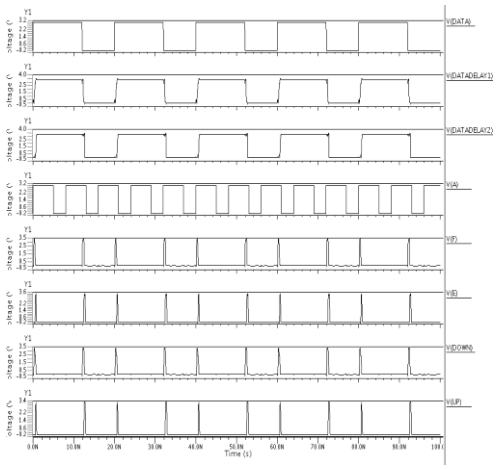
(c)

Figure 9: Output waveforms of phase detectors (a) PD_CPL OUTPUT (b) PD_TGL OUTPUT (c) PD_4T XNOR OUTPUT

Table 1: PD's Performance Summary

PHASE DETECTOR	***CPL_PD[5]***	***TGL_PD (Present work)***	***4T XNOR_PD (Present work)***
Power Consumption (nW)	4.7856	4.3337	0.5055
Maximum frequency (GHz)	2.0	1.0	1.0

Table 1. summarizes the power consumption and maximum frequency of three phase detector. Results of power consumption are obtained with reference frequency of 45 MHz. Phase detector with transmission gate XOR show power consumption of 4.3337 nW and detect the signal of maximum frequency upto 1GHz. Phase detector with 4T XNOR shows power consumption of 0.5055nW and detect the signal of maximum frequency upto 1GHz. The 4T XNOR_PD consumes the least power due to less number of transistors.



5. CONCLUSION

For low power PLL, two different types of phase detectors have been proposed and result has been compared. First circuit is based on TGL XOR with six transistor and second is based on 4 transistor XNOR gate The simulation results are focused on the generation of the UP and DOWN signals with lesser power consumption. Modified circuit shows less power consumption than conventional circuit with CPL

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