Partitioning VLSI Circuits

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ABSTRACT

Partitioning is a critical area of VLSI CAD.
In order to build complex digital logic circuits it is often essential to sub-divide a circuit into smaller parts.Circuit partitioning plays an important role in physical design automation of very large scale integration(VLSI)chips.In VLSI.In VLSI circuit partitioning the problem of obtaining minimum cut is of prime importance.To enhance other criteria like power,delay and area in addition to miminum cit is included.

Keywords

VLSI, circuit partitioning,delay,cut size.

1.Introduction

Partitioning is a technique to divide a circuit or system into a collection of smaller parts (components).[1] It is a design task to break a large system into pieces to be implemented on separate interacting components and on the

other hand it serves as an algorithmic method to solve difficult and complex combinatorial optimization problems as in logic or layout synthesis. The main reason that partitioning has become a central and sometimes critical

design task today is the enormous increase of system complexity in the past and the expected further advances of microelectronic system design and fabrication. The main goal of this paper is to design a class of iterative algorithms for VLSI multiobjective partitioning such that circuit delay,power dissipation and interconnect cut set are minimized under the balanced constraint. The main search algorithms used are Genetic Algorithm(GA),Tabu Search(TS).These algorithms are used to find a solution that minimize these costs while satisfying balance constraints.

2.VLSI Partitioning

VLSI design is a complex process and is therefore it is broken down into no of intermediate steps. Moreover partitioning is considered to be an NP Complete problem which means polynomial time algorithm exists for solving the problem.
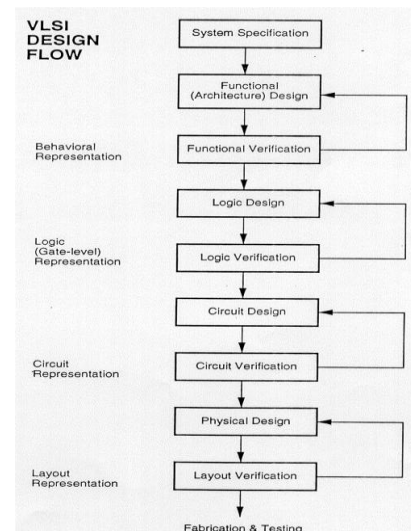

Figure 1: VLSI design flow

VLSI circuit partitioning is a vital part of physical design stage. The essence of circuit partitioning is to divide the circuit into a number of sub-circuits with minimum interconnections between them. This can be accomplished by recursively partitioning a circuit into two parts until we reach desired level of complexity. Thus two way partitioning is basic problem in circuit partitioning, which can be described as [2].This paper proposes a different approach to solve circuit partitioning problem. We made use of evolutionary algorithm & clustering approach.
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The main algorithms Included in this approach are-

- Kernighan-Lin (KL) algorithm [3]
- Fiducccia-Mattheyses(FM)
- Algorithm [4]
- Simulated Annealing
- Genetic Algorithm
- Tabu Search

2.1 Kernighan-Lin(KL)

- The most basic approaches to the partitioning problem are to treat the circuit as a graph. This is true for the first, and most famous partitioning algorithm, called the Kernighan-Lin algorithm. This algorithm was originally designed for graph partitioning rather than circuit partitioning, so to apply the algorithm, one must first convert the circuit into a graph. To do this, each gate is treated as a vertex of the graph. If two gates are directly connected by a net, then an edge is placed between the corresponding vertices of the

graph. Limitation: It needs a predefined subset size to start with.

2.2 Fiduccia Mattheyeses(FM)

It is the modification of KL group method
For circuit partitioning. The original KL heuristic is an improvement procedure where the current partition is improved by swapping pair of nodes belonging to the two subset of the current partition.
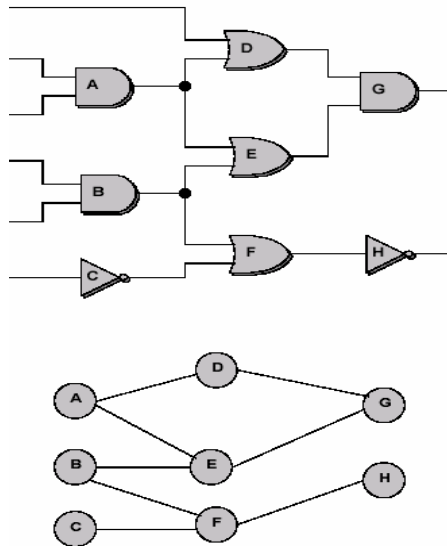

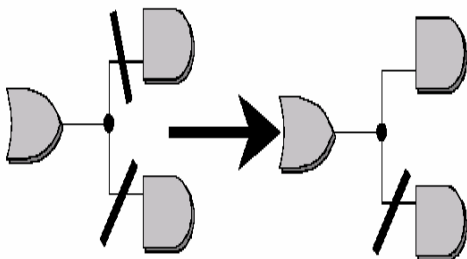**Figure 2: Converting Circuits to Graphs**

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Figure 3: Figure showing difference in F-M & K-L approach

2.3 Simulated Annealing

The principal of stimulated annealing algorithm is that a system is put in a high temperature environment .At this temperature is applied a sufficiently long sequence of random elementary transformations to reach at this equilibrium. Limitation: It is of sequential nature. And its parallelization is quite difficult.

2.4Genetic algorithm

Genetic algorithm is a search algorithm based on the principals of evolution of natural genetics. There are several key concepts involved with genetic based algorithm (GA)[5].they are initial population creation, offspring creation, successive generation selection and generation run control.
 The effectiveness of the GA depends on appropriate mix of exploration and exploitation. Three operators are used for this are selection, mutation and crossover. Selection according to fitness is the source of exploitation. The mutation and crossover operators are source of exploration. . Limitation: Their effectiveness is greatly dependent on the representation of the solution space.

2.5Tabu Search

Tabu search has been applying for solving the problem of partitioning with single objective (cutest) graph bisection. Tabu Search is an iterative heuristic that has been applied for solving a range of combinatorial optimization problems in different fields.

3.Partitioning Formulation

Given a set of modules V= {v1,v2.....vn)
The purpose of partitioning is to assign the modules to a specified no of clusters K satisfying prescribed properties.

Definition:

A K Way Partitioning
Pk={c1,c2.......ck}consists of K clusters(subset of V),c1,c2.......ck such that c1∪c2...........∪ck=V .and Ci∩Cj=ϕ for i={1......k}and j={1......k}and j≠i.
Our task is to divide V into 2 subsets Vo and V1 in such a way that the objectives are optimized.
We aim at minimizing the following objectives.

1. Cutsize

The cardinality of the set containing the net cut by the cluster is called cutsize.

2. Delay

The delay of the circuit is optimized by optimizing the delay between the input cell to the output cell,input cell to the internal cell and vice versa and internal cell to the output cell.By doing this the delay of the total system will be minimized.

3. Power dissipation

The power should be evenly disrtributed throughout the system hence it should be verified that total power of each module sis almost same.

4. Network Area

Area is an important constraint .it should be kept small.

4.   CONCLUSION   AND   FUTURE DIRECTIONS

 We   have   studied   about   various   algorithms for partitioning VLSI circuits.The results obtained of these algorithms differ on the basis of the parameters used.The presented partitioning techniques can be extended to perform the optimization of other steps for
VLSI physical design.

5. REFRENCES

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