Revolution of Integrated Circuit in the Era of 2020

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ABSTRACT

There are 12 reasons 2020 will be an awesome year in the field of chips. By the using of chip Japan will build a robotic morn base,(build a robotic lunar outpost by 2020), China will connect Beijing to London via high speed rail, cars will derive themselves, bio-fuels will be cost –competitive with fossil fuels ,the flying car will be air borne, we will control device via microchips implanted in our brains ,all new screens will be ultra –thin ,OLEDS ,commercial space will take us to the moon and asteroids(and we will be mining them). A $ 1000 computer will have to the processing power of the human brain some decent AR glasses developed, universal translation will be common place in mobile device, and we will create a synthetic brain that function like the real deal.

Keywords

INTEGRATED CIRCUIT, NANOELECTRONICS, FEMTOELECTRONICS

1. INTRODUCTION

1.1 2020 world with chips

At the future 1 day at a time we have seen all the world move around the chips. The new commitment has to be towards sustainable nano electronics ,guided by creating sensing, computing, memory and communication function which moves just a fewer operation , each operation consumed energy less than one or a few femto joule, less than any of the 1014 Synapses in our brains. The expected 6 billion user of these chip in 2020,through mobile ,intelligent companies, will be benefit from global and largely equal access to information, education , knowledge, skill and care.

1.2 From Microelectronics to Femtoelectronics

In the year 2000 the first microchip was produced with gate length <100 nm ,and microelectronics received the new label nanoelectronics. The derive in the industry along the nano road map toward shorten transmitter continued in order to build faster processor and to pack more memory bits on each chip . By the year 2010,the planned 32nm milestone(node) had been reached, including most of the expected chip specifications but with the twist since 2005. The 3D integration of many thin chip on top of each other, connected through TSVS (through silicon via), to enhance the program on the road map. But the year 2010 was also marked by the rapidly growing consensus that the end or read map is near at 15nm (2016) or 10nm (2018) at best, and that none of the new quantum-nano devices will have any economic impact before 2025-2030.

2. The future of six chip technology

The six silicon chip technology will play significant roles in decade 2010-2020 for the development of high performance low energy chip in 2020 and beyond. After the completion of 25 year working style and their performance all are the methodology demonstrated and some in fact are worth revisiting at the nanometer scale.
[1]We lightning the future of eight chip generation evolution and their role and potential with four milestones.

- First prototype
- First product
- First killer product
- Market dominance

Our six candidates are explained one by one in series.

2.1 The bipolar transistor

The bipolar transistor first prototyped in 1950 under J .Besuard in Bell labs. It has the T/R type of choice for the first IC in the technology era. The control of two types of S/C for its operation and it can be used as amplifier switches or as oscillator. Its operation performing by the involvement of holes and electrons. Its killer product, the operational amplifier and T/R-T/R logic brought an ICS market share for this type of ICS of over 95% in 1970. Ti had lost its lead by 1980and bipolar ICS are today on the basis of hetero junction Bipolar transistor (kftbts) with maximum frequencies of 600 GHz. The BJT that can handle of very high frequencies. It is common in modern ultrafast circuit mostly based on RF system two commonly used HBTS are silicon-germanium and Aluminium–germanium –arsenide through a wide variety of s/c may be used for the HBT structure. . HBT structure grown by epitaxy techniques likes MOVCVD and MBE. It provided the better trance conductance, bandwidth and the complementary cross-coupled nano pair can because the best ultra low energy signal generator.

2.2 MOS Integrated Circuit

In the MOS field-effect –transistor IC appeared in 1960 by DAWORKAKNG and J.MARTIN JOHN at bell labs earned some limited recognition as controller and random –access memories (RAMS) BY 1968 and began their march to the top in 1972 with microprocessor and dynamics RAMS on killer product which leads to pass bipolar ICS in 1980. The future of upcoming technology will be based upon this IC circuit and it dominant at all other field.

2.3 CMOS and BI-CMOS Integrated Circuit

This type of ICs were first presented in 1965 by using of p and n channel as building blocks. It reduced the power consumption because no current flow (ideally) and then no power is consumed except when the logic gates are being switched.
MOS and CMOS circuit are most effective solution for giant-scale integration in silicon on insulator technology increases the capability ,reduced the complexity of the circuit .The end of progress just scaling down transistor dimension is near this is not a matter of technology capability ,but one of the atomic variance in 10 nm transistor .once only approx 6 atoms are responsible for their threshold voltage gain and best means 95% of these transistors would have between 1 and 9 such atom .which shows at their dimensions, not a transistor but the cross-coupled pair is CMOS invert the elementary and necessary s/g regenerator at the hearts of ultra-low voltage differential.

2.4 3d CMOS Integrated Circuit

A three dimensional (3-D) CMOS integrated circuit fabricated based on the CMOS SOI technology .The first layer of transistor has formed on SOI. The second layer of transistor been built on large grain poly silicon on insulator(LPSOI).The crystallized film has been formed by the amorphous silicon using metal-induced lateral crystallization(MILC).The device from the lower and the upper layer were characterized and the result indicated that the SOI are 4PSOI device have similar electrical characteristics. The 3D circuit design and layout consideration will be introduced .The 3D CMOS inverters were demonstrated with p-channel device starting over the n-channel ones. The ring oscillator show that the 3D circuit has 30% reduction in the layout area and it operated at power supply as low as an 0.5V.The low propagation delay load capacitance suggest that 3D circuit has higher performance their the conventional two-Dimension (2-D) circuit.

2.5 SOI CMOS Integrated Circuit

Silicon on insulator (SOI) CMOS integrated circuit used for high voltage SOI CMOS IC technology for driving plasma display panels. In this way developed a new high voltage CMOS (HV-CMOS) IC technology by using 5 um-thick SOI . In this technology, trench isolation and a 0.5 um role CMOS process are also adopted. This seven series HV-CMOS fabrication process in different voltage rating (In which the maximum voltage rating hears 250v) and optimized their characteristics respectively. The HV-CMOS IC with full CMOS type level shifter transmitter suited to low power consumption color plasma display panels (C-PQPs) and high –speed switching has been confirmed. The chip size of the developed PDP scan driver IC could be reduced by 40% compared with the conventional chip. The main attribute of SOI CMOS is the insulting layer of Sio2 isolating the integrated circuit transmitter from the bulk substrate . The feature has a number of benefits.

- Low leakage current to substrate enables greatly improved circuit operation to 225° c continuous and excursions to 300°c
- Reduced capacitance for faster and lower power circuit.
- Greatly reduced noise with isolation from the bulk silicon for sensitive mixed circuit.

2.6 Different MOS Logic

In IC design, dynamic logic (or sometimes clocked logic) is a design methodology in combinational logic particularly those implemented in MOS technology .It is distinguished from the so-called static logic by exploiting temporary storage of information in stray and gate capacitances. It has popular in the 1970 and has seen a recent resurgence in the design of high speed digital electronics particularly computer CPUS. Dynamic logic circuit are usually faster than static counterparts, and DYNAMIC required less surface area ,but are more difficult to design. Dynamic logic has a higher toggle rate than static logic but the capacitative loads being toggled are smaller so the overall power consumption of dynamic logic may be higher or lower depending on various tradeoffs. When referring to a particular logic family, the dynamic usually suffices to distinguish the design methodology e.g. dynamic CMOS or dynamic SOI design.

3. GRAPHICAL AND TABULAR DATA ON CHIP

The observation of this data shows the manufacturing trends for future purpose 2020. This trends totally based upon the technology node , integration capacity and energy level .This trends continue in to year 2020 and that observation made by "GOORDEN MOORE" , co-founder of INTEL ,that the no of transistor per square inch incorporated on chip will be double approximately every 2 year . the mainstream of that observation is making high volume design will continue to use transistor as switching device and integration capacity is expected to be in 100s of billions of transistor . For the year 2020 the operational energy is predicted to be lower than 10^{-18} joules. Which shown in table and graph.

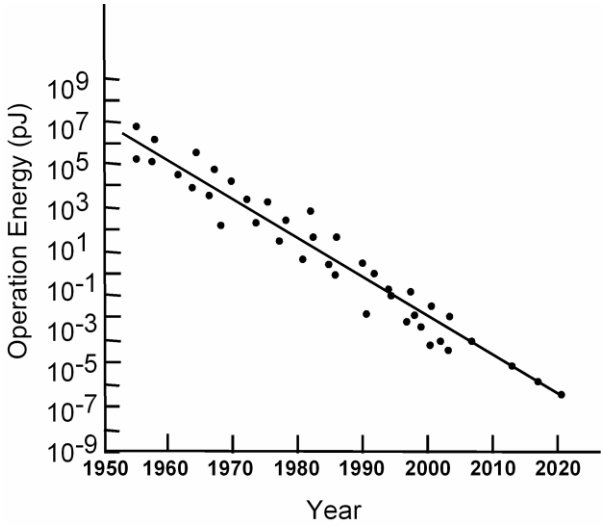

Fig.1 the operation of energy low to increase the year

High Volume Manufacturing	2004	2006	2008	2010	2012	2014	2016	2018
Technology Node(nm)	90	65	45	32	22	16	11	8
Integration Capacity (BT)	2	4	8	16	32	64	128	256

Table 1: Increase the capacity to increase the Year

4. EDUCATION & RESEARCH

Nanoelectronics chips has great potential for further, sustainable growth and this growth is needed worldwide, because new chips provide for the technology foundation for all those product and services that shapes our lives . we aspect that it provided the various research in different type of field among them some are listed below.

4.1 Silicon Brain

The more radical mapping of brain like structure and processes in to VLSI substrate pioneered by carver mead ago 30 year. The basic idea was to exploit the massive parallelism of such circuit and to create low power and fault-tolerant information system. neuromorphic engineering has recently seen a revel with the availability of deep CMOS technology , which allows for the construction of very large scale mixed – signals system combining local analog processing in neuronal cells with binary signaling via action potential . modern implementation are able to reach the complexity scale of large functional units of human brains , and they features the ability to learn by plasticity mechanism found in neuroscience. Combined with high performance programmable logic and elaborate software tools, such system are currently evolving in to user configurable NON-VON-NEUMANN computing system. The basic properties of biological brains with up to 200 billion neurons and their 10^{14} synapses , where action on a synapses takes approx. 10 ms and involves a energy of approx. 10 FJ .In Europe and the USA , which are intended to integrate 10^{8} neurons and 10^{12} synapses which is equivalent to level of cats brains ,in a volume of 1L and with a power dissipation < 1kw.

SOME FEATURE OF THE HUMAN BRAIN

The human brain consists of about 200 billion neurons , each connected via thousands of synapses to other neurons, forming an incredibly powerful sensing, information and action system that has-

1). Unparallel intelligence i.e, learning, comprehension knowledge, reasoning, planning

2). The unique capability of cognition, i.e the power of reflect upon itself , to have compassion for other and to developed a universal ethic code.

After developing of silicon brain we aspects that they work on this type of operation .

1). All kind of feature and pattern recognition.

2). Understanding many body scenes, objects people , traffic.

3). Language understanding and translation.

We aspects that all these task work properly in the age of femto –electronics.

On the basis of complex MOSFETS (CMOS) technology active pixel sensor (APS) began to appear in 1990. These pixel allows random access, global shutters and they are compatible with focal plane imaging system combining sensing and first level image. after sometimes it having smaller feature and towards ultra-low leakage currents has provided reduced dark current and micro size pixel resolution ,and many have very high sensitive equivalent to ASA 12.800 after this result HDTV video camera will become a commodity .Because charge integration sensor suffer from limited dynamic range , significant processing efforts is spent on multiple exposure and piece-wise analog –digital conversion to reach range >10,000:1 this offers a range of almost a million to 1 ,constant contrast sensitivity and constant colors , 3D retinal morphic stacking of sensing and processing on top of each other is being revisited with sub-100nm CMOS circuit and with TSV technology with sensor output directly on top of neurons ,neural focal –plane processing will regain momentum and new level of intelligent vision will be achieved .This pushes towards thinned wafers and TSV enables backside-illuminated and other pixel with a 100% fill-factor .3D vision ,which relies on stereo or on time of flight , high – speed circuit , will also benefit from scaled –down CMOS technology both because of their size as well as their higher speed .

In future, in the age of FEMTOELECTRONICS, vision sensor helps you finds defects earlier in the any manufacturing process. it offers standard and high resolution grayscale colors , single and multi-purpose vision sensor.

4.2 Vision and imaging fundamentals

According DR.THEUWISSEN, the scaling rules associated with pixel size or pixel edge (P) set up for standard visual information in future.

1) Pixel area -p^2

2). Chip area - p^2

3). Chip cost –p^2

4). Read out energy /Pixel - p^2

5). Lens volume - p^3

6). Camera volume - p^3

7). Camera weight – p^3

8). Sensitivity - p^{-2}

9). Dynamic range (bright dark) - p^{-2}

4.3 Supercomputer and Super processor

In recent decades, the world has seen compute penetrate almost every aspects of everyday life and this trend is likely to continue. This rise of internet and more recently smart phones resulted in an exponential increase of data. At the same time, companies and other organization are striving to use the available data more intelligently in order to reduce operational risk and increases revenue and profit.

But, this time the design challenge of processor and computer faced by technology and design scaling slow down , problem with the new design and potential solution as well as longer term trends and requirements for future processor and system with technology and design scaling slowing down ,the processor industry rapidly moved from high frequency design to multi core chips in order to keep delivering the traditionally expected performance improvement .however ,this rapid paradigm change create a hole new set of problems for the efficient usage of these multi core design in large scale system. we aspect that in future the new programming model developed, server system are more and more enriched with special purpose processor because these specially engines are able to deliver more performance within the same power envelope than general purpose microprocessor for certain application. We also aspect that in future processor and system need to be designed with tight collaboration between hardware and software.

4.4 Rational Implants for Blind Patient

Blindness is the one of the most serve handicaps we can imagine. However we have first to distinguish between people who are blind from birth, on the one hand and those who become blind by disease or accident. [1] People who blind from birth completely lack any training of their visual system and that means that probably there will never be any artificial vision for this group. However [2]people who have never seen in their life typically do not miss their ability too much. Today's approaches for prostheses for the blind work exclusively with patiently whose blindness is a result of disease. Among them are age related macular degeneration (AMD) and retinitis pigmentosa (RP) which are both related to photoreceptor degeneration [1, 2]. Now come on topic Retinal Implementation. [3]The first application of an Implantable stimulator for vision restoration was developed by DRS. BINDLY and LEWIN in 1968 by using of electrical stimulation and if motivated the development of several other implantable device for stimulation of the visual pathway including Implants.

Now a days, There are three types of retinal implants currently in clinical trials: epiretinal implants (on the retina),Sub retinal Implants (behind the retina) and suprachoroidal Implants (above the vascular choroid).Last year, the German company Retinal Implants, AG began a second round of clinical trials for their retinal implants after success of their first round the implant is wirelessly controlled chip about 9sq. meter that is implant directly beneath the retina. The chip contains 1500 pixel replacing the light receiving external light and then transmitting those signal directly to the brain.

In these trials of the nine patient included in the trial, 8 out of nine were able to perceive light, and seven out of nine able to definitely find the source of that light, six out of nine had a significant of portion of their vision restored, with some patients able to read letters out books and also distinguish facial features .

In the future the age of Femtoelectronics the researcher fully focused on long term stability and safety as well as the development of visual recognition abilities via learning effect, over a longer observation period will be addressed in future patients who receive the implant.

5. CONCLUSION

This paper conclude that in the year 2020 our world is equipped with advanced integrated circuit chips and these integrated chips play an important role in many day to day work. They can plays a great role in the area of the science and technology .These integrated chips made with better quality of components , reduce the complexity of integrated circuit ,smaller sizes , required low energy level for operation in the age of 2020. So it helpful in modern world with its tremendous advantages.

6. REFERENCES

[1] R .Jacob Baker "CMOS circuit design, layout and simulation" 3rd edition (IEEE press series on microelectronic system) on Amazon.com.

[2] Express computer magazine vol.24/no.13/September-2013

[3] Chips 2020,A Guide to future of nanoelectronics bernd hoefflinger in the frontiers collection(2012).ISBNL 978-3-642-22399-0 DOI I0.1007/978-3-642-28096-7 in springerlink journal

[4] Electronic Devices and Circuit Theory Tenth Edition. by Robert L. Boylestad.

[5] Hoefflinger , B. selzer ,M. warkowski, "digital logarithmic CMOS multiplier for very high speed

signal processing" IEEE custom integrated circuit conference, digest PP.16.7, 1991.

[6] P. Shivakumar " Modeling the effect of technology trends on the soft error rate of combinational logic" IEEE proc. Int. conf. on dependable and syst. And net. June 2002.

[7] International technology roadmap for semiconductors, http://www.sematech.org.,2005

[8] Emerging research devices, ITRS, http://www.sematech.org.2005

[9] Sharma, R.K Ehinger , management of hereditary retinal degeneration : present status and future direction. scen. opthalmol 43 (1991).