Performance Comparison of an Algorithmic Current-Mode ADC Implemented using Different Current Comparators

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ABSTRACT
In this paper a 4-bit algorithmic current mode Analog-to-Digital Converter (ADC) has been implemented. A vital component of this ADC is a current comparator. We have simulated three popular structures of current comparators that can be used to implement this ADC and compared their performance. The circuit has been implemented using 0.18 μm CMOS technology with a supply voltage of 1.8V.

General Terms
Signal Processing

Keywords
Algorithmic, ADC, current-mode, current comparator, current subtractor, current mirror.

1. INTRODUCTION
In the field of signal processing, use of digital circuits is quiet prevelant. However, the real world data is analog in nature and needs to be converted into digital form to be made compatible to digital signal processing systems. This necessitates the use of high speeds analog to digital converters (ADC) that are to be interfaced to these digital signal processing systems. An ADC accepts an analog electrical signal such as voltage or current as its input and outputs a corresponding digital number in the desired format.

There are many topologies of ADCs, each having its own advantages over the others. One such topology is that of Algorithmic ADCs. Algorithmic ADCs have a simple architecture and occupy smaller area. An algorithmic ADC is a combination of flash ADC and a successive approximation ADC. The main advantage of the topology is the availability of parallel outputs and the use of number of comparator equal to the number of ADC bits. Additionally, it has a very small size and provides high sampling rates.

Although the fist proposed Algorithmic ADC was realized using conventional voltage mode technology [1], several advancements have been made on that structure and a new class of algorithmic ADCs, current-mode algorithmic ADCs has been developed [2]-[3]. [4] had presented a current mode algorithmic ADC using the bipolar technology and [5] with CMOS technology. The current-mode approach facilitates reduced size and faster speed as compared to the voltage-mode algorithmic ADC.

In this paper, a 4-bit current-mode algorithmic ADC has been implemented. The 4-bit structure is exemplary and can easily be extended up to a higher number using the underlying algorithm elaborated upon in section 2. In Section 3 the basic modules used in this ADC design have been discussed. The simulations and results have been presented in the section 4. Finally, section 5 summarizes the conclusions.

2. THE CURRENT-MODE ALGORITHMIC ADC
Being a current-mode ADC, this structure accepts a current signal as input (Iin) which is to be converted into its corresponding digital value. The input current Iin is compared to a reference current (Iref). Fig. 1 illustrates the basic schema of the implemented algorithmic ADC. It comprises of 4 stages wherein the first stage produces the most significant bit (B0) and its complement (B0'). This output is passed on to the next stage to produce the next lower order bit and so on. At each stage, Iin is compared to a progressively increasing value of Iref as per the underlying algorithm. The algorithm is as below-

In Stage 1,

- Input current Iin is first subtracted from a current value equal to Iref/2.
- The difference thus calculated is then sent to a current comparator which generates the digital output which is the most significant bit (MSB), B0. B0 is 1 if Iin is greater than Iref/2, else 0.
- The value of B0 is used to calculate the next lower order bit B1.
- A current Iref/4 is added to the current Iin if B0=0 else to Iref/2 if B0=1. B1 is generated by subtracting these two currents using a current subtractor and then passing the result through the current comparator in stage 2.

In stage 2, current comparator generates an output level corresponding to the difference input being sent to it. The process of adding weighted currents to the previous current values and comparing their values upon subtraction is carried out till the required number of bits have been obtained.

The basic algorithm for calculating the bits for this topology is given as

For B0,

Iin is compared to Iref/2.

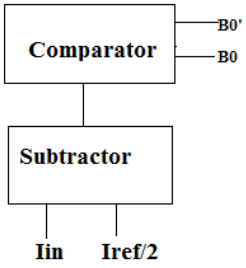
For B1,

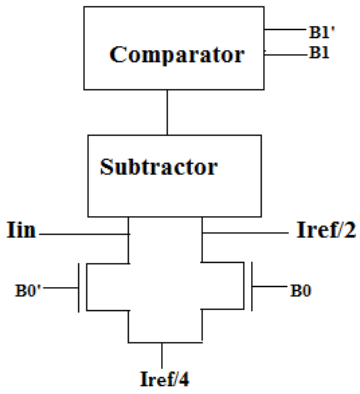
$$\text{Iin}+B0'.\frac{\text{Iref}}{4} \; compared \text{ to } \frac{\text{Iref}}{2}+B0.\frac{\text{Iref}}{4}$$

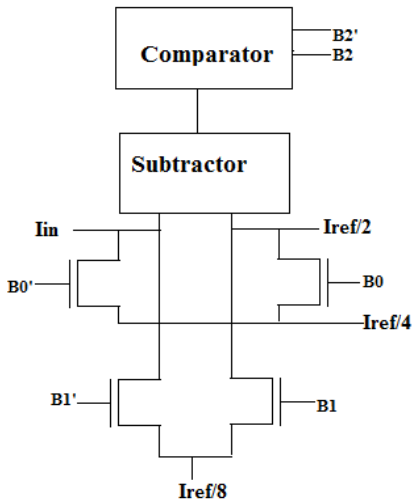
In general, for an n-bit current mode algorithmic ADC, nth bit is computed as-

$$\text{Iin}+B0'.\frac{\text{Iref}}{4}+B1'.\frac{Iref}{8}+....+Bn-1'.\frac{Iref}{2^{n+1}} \; compared \text{ to}$$

$$\frac{\text{Iref}}{2}+B0.\frac{\text{Iref}}{4}+B1.\frac{Iref}{8}+....+Bn-1.\frac{Iref}{2^{n+1}}$$







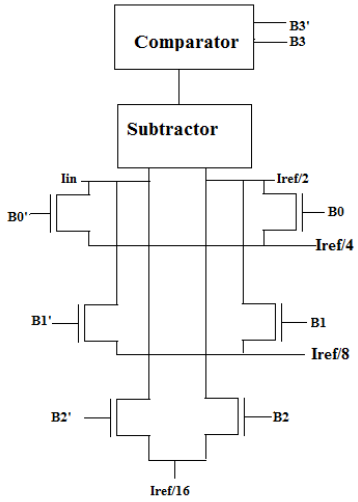


Fig. 1: The Algorithmic ADC

3. THE BASIC MODULES OF ADC

The different blocks for implementing this topology are as follows:

3.1 Current Subtractor

Every stage of this ADC requires a current subtractor to compute the difference between the input current and a reference current. Many popular architectures for these subtractor circuits have been reported in [5]-[6]. Most of them employ current mirror circuits for obtaining difference of the input and the reference current.

The implementation used in this paper has been designed using current mirror based current subtractor as shown in Fig. 2. This circuit requires careful calibration of W/L parameters, with reference to the input applied, to obtain correct output. Fig. 2 also gives the simulation result for our subtractor which gives a worst case delay is of 1.5 ns.

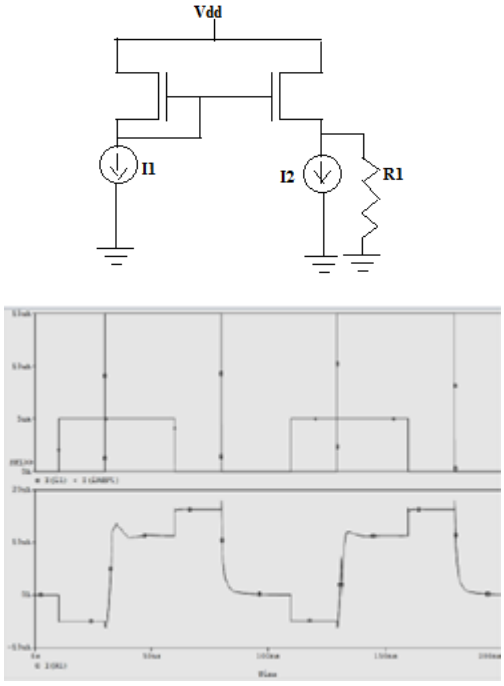


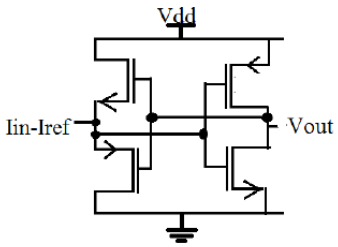
Fig. 2: Current Subtractor used in the design and its simulation results

3.2 Current Comparator

The current comparison process involves comparing one or two currents and distinguishing if the current (or the difference of two currents) is positive or negative. The basic requirement for the current comparator design to be used in current-mode ADC are low input impedance and a quick time response. Additionally, accuracy is also crucial which depends on the offset caused by the mismatch of transistors.

Many efficient structures of current comparators have been reported in literature [6]-[15], each of them emphasizing on one or several aspects as a trade off against the other characteristics. The first CMOS current comparator was proposed by D. Freitas and K. Current in [7]. Since then, many high performance current comparators have been proposed. H. Traff presented a simple and high-speed current comparator in [8], but the output swing of Traff's comparator could not reach the power supply rails results respectively. However, it still remains the pioneering structure in the field of current comparator design. Significant improvements to this structure were reported by Chen [10] and Tang [14]. These circuits offer various advantages in terms of speed and accuracy compared to other such structures. Hence, this paper employs the current comparators proposed by Traff [8], Chen [10] and Tang in [14] for the algorithmic ADC implementation.

Fig 3, 4 and 5 show Traff's, Chen's and Tang's current comparator and their simulation results respectively. The simulation results show that the worst case delay offered by Traff's is 0.5ns, Chen's is 0.42ns and that of Tang's is 0.252ns.



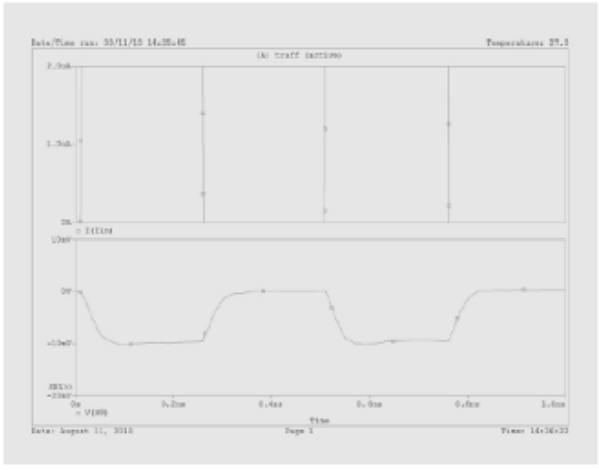
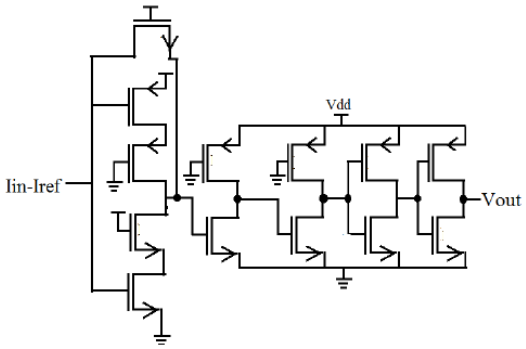


Fig. 3: Traff's Current Comparator and simulation results



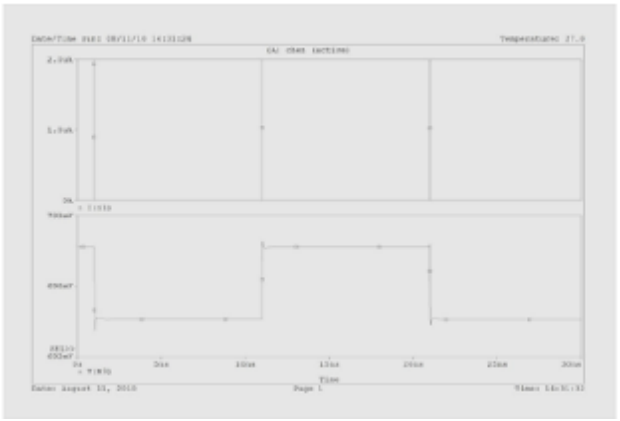
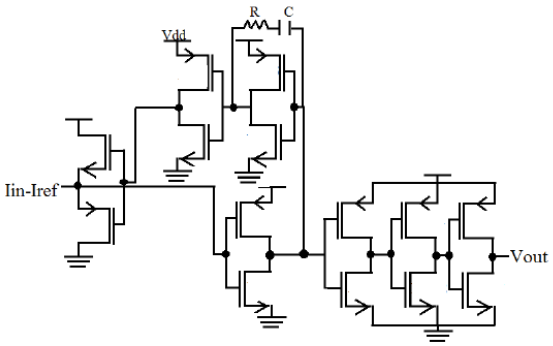


Fig. :4 Chen's Current Comparator and Simulation results



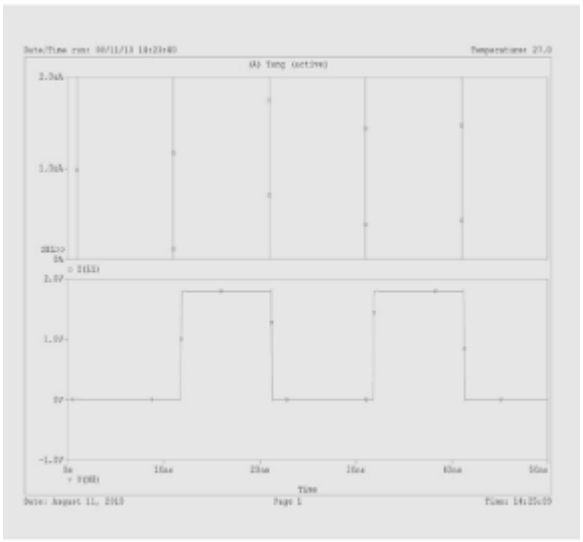


Fig. 5: Tang's Current Comparator and Simulation results

4. SIMULATION RESULTS

A 4-bit current mode algorithmic ADC based on the algorithm described in Section 2 was simulated using PSPICE program in 1.8 □m CMOS technology. Supply voltage was taken as 1.8V. All the blocks were simulated and their delays were calculated. The subtractor exhibited a delay of 1.5ns. For current comparators, simulation results show that Tang offered the minimum delay followed by Chen and Traff.

Fig. 6 shows the outputs of all the four stages corresponding to 4-bit outputs i.e. B0, B1, B2, and B3. The total number of transistors used to implement this 4-bit ADC is maximum when using Tang [14]'s comparator, followed by Chen [10] and Traff [8]. Thus, in choosing the current comparators for a particular implementation of this algorithmic ADC, the trade-off between the speed of operation or the total propagation delay and the total transistor count, which eventually translates in the chip area, needs to be given the due consideration.

The performance comparison for this 4-bit ADC in terms of the transistor count of the total structure and total propagation delay for different current comparators is summarized below in Table 1.

Table I. Performance Comparison of Different Current Comparators

Current Comparator	Total Propagation delay (comparator + subtractor)	Transistor count of the total structure
Traff [8]	2ns	36
Chen [10]	1.92ns	72
Tang [14]	1.752ns	76

5. CONCLUSIONS

In this work a current-mode algorithmic ADC compatible with digital CMOS process has been implemented. The structure has been designed for 4-bit but can be easily expanded for higher number of bits. The structure has been implemented using a high speed low delay CMOS based current comparators and a current mirror based current subtractor. A comparison of the performance with different current comparators used has also been drawn. It is observed that that while the ADC implemented using the Tang's structure offers a high speed but it occupies a very large area. On the other hand, Traff offers a slower speed but has significantly reduced transistor count which is less than half that of Tang. Further, Chen offers slower speed comparable to that of Traff, its transistor count is comparable to Tang.

Based on the observations made in this paper, it can be inferred that Algorithmic ADC applications requiring smaller area should prefer Traff's implementation while high speed applications which are not area sensitive can choose to opt for Chen's or Tang's implementation. These implementations can further be tested for power dissipation and can accordingly be utilized in power sensitive applications.

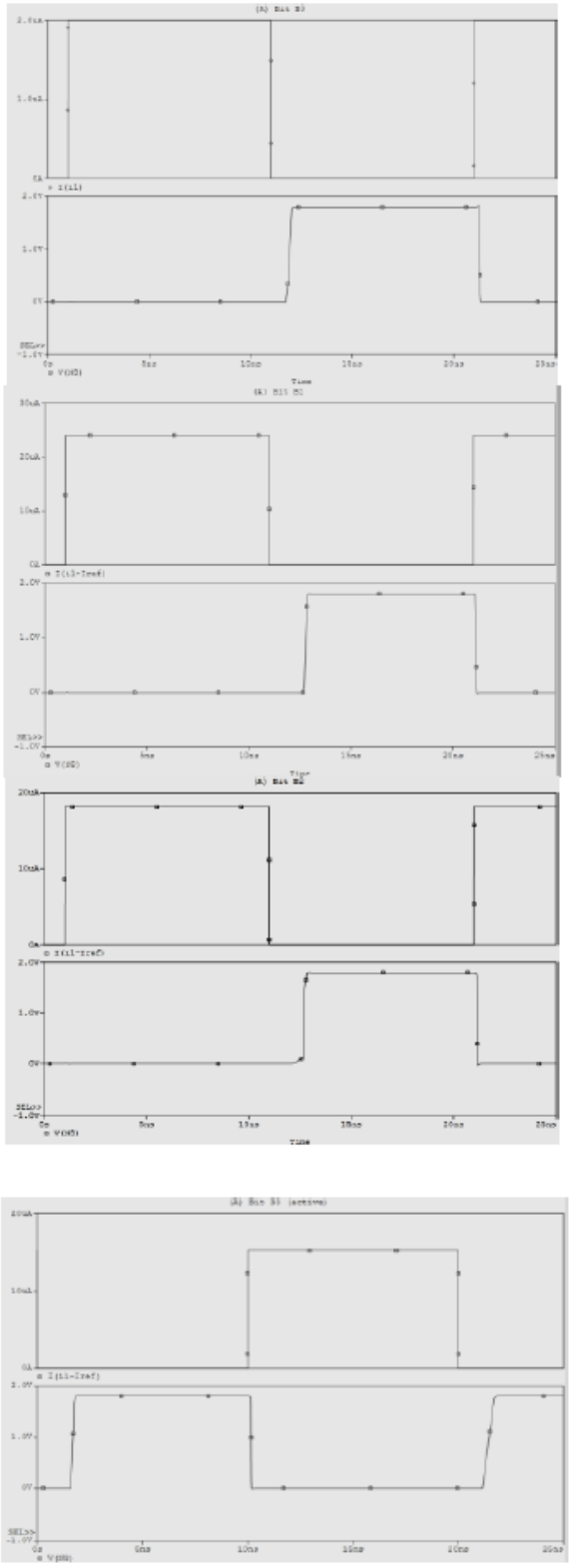


Fig. 6: Simulation results for 4-bit output

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