Design of VCO for Microwave Frequency Band

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ABSTRACT
Voltage Controlled Oscillator (VCO) is an important building block in wireless communication system. In this paper a five stage current starved Voltage Controlled Oscillator (CMOS VCO) is designed which is used in Phase Lock Loop (PLL). The design is implemented on CADENCE VIRTUOSO Platform with high oscillation frequency and low power dissipation. The oscillation frequency of the designed VCO ranges from (665.7MHz-1.128GHz). The circuit is simulated using 180nm CMOS Technology. Simulation result shows that the power dissipation is -12dBm at power supply of 1.8 volt and the phase noise is (-105dBc/Hz @ 10MHz offset). The designing of such VCO shows the efficient performance of the oscillator circuit under given conditions. Such design is useful for frequency synthesizer application in PLL with less design cost.

Keywords
Cadence Virtuoso, Current Starved VCO, PLL, Frequency Synthesizer, Phase Noise

1. INTRODUCTION
VCO is an essential block of the PLL in communication system. The design of such kind of VCO involves a trade-offs among power consumption, oscillation frequency, area occupied and speed of PLL. So it is important to estimate the oscillation frequency for the VCO. The main motivation behind the design of such type of several stages VCO is that how the power consumption and area occupied by the PLL circuit can be reduced up to the certain manner and also how can we evaluate the performance on the basis of high oscillation frequency and low phase noise as well as jitter [2],[4]. As the phase relationship between input reference data and feedback clock from VCO is not fixed and for reliable gain of high speed data, phase matching is essential for PLL [6].VCO is an essential block for several RF transceivers to select the frequency as well as to generate the signal. Recently RF transceivers acquire programmable carrier frequencies which depend upon PLL to accomplish that one. A less accurate oscillator circuit is required in the feedback path for a PLL which behaves as a control voltage function at the input. Mostly the oscillators in recent scenario require oscillators which are tunable. PLL is generally used for clock recovery, timing generation, FM & AM demodulation and as a frequency synthesizer in wireless communication system. Designing of CMOS-VCO can be done through many ways: by using LC-tank Circuit, Ring VCO, Relaxation Oscillator and Differential VCO circuits. In past years LC oscillator has depicted better phase noise performance because phase noise performance of such tuned VCO depends upon the Q- factor for LC-tank oscillator. Spiral inductor coils in LC-tank VCO requires some extra processing steps and designing cost, also there is a complications to control the eddy current. Tuning range is relatively low (10%-20%) for such VCO [1]-[5]. Also for high oscillation frequency the power consumption of ring VCO may not be less for the equipments which are operates through battery [1], [17]. To overcome these problems, we are going to work on five stage current starved VCO and evaluate the performance parameters. This paper is divided into three sections: Section II: describes the schematic of VCO, Section III: shows the simulation results, finally the conclusion are taking place in Section IV.

1.1 System Overview
A PLL is a closed-loop feedback system which produces a fixed phase relationship between its output clock phase and reference clock signal at input side shown in figure 1. A PLL generally detects the phase change within the bandwidth of PLL. A PLL also generates multiple frequencies of higher range for a single reference input frequency. This phenomenon is called as frequency synthesis. Basically a PLL is a negative feedback control circuit. The main purpose of PLL is to match the phase of input reference signal with the feedback signal. If there is any mismatching occur in the phase after comparison then it perform several iterations until same phase is not found. This situation is called as lock mode. Still the iteration will be continued but as the PLL is in lock mode so PLL output will be constant [13], [14].

A PLL basically consists of five main blocks:

1. Phase Frequency Detector (PFD)

2. Charge Pump (CP)

3. Low Pass Filter (LPF)

4. Voltage Controlled Oscillator (VCO)

5. Divide by N Counter

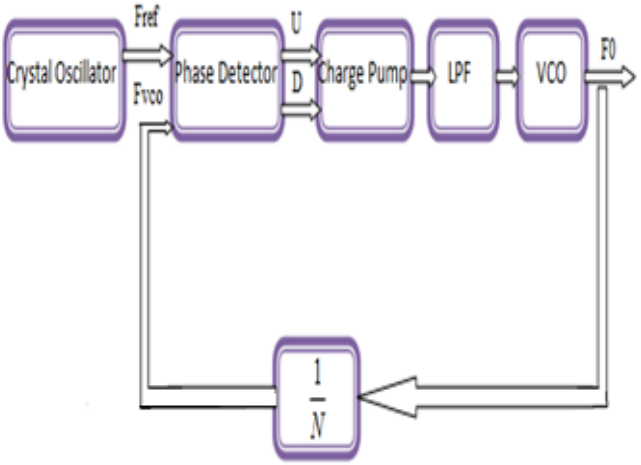

Fig 1: Basic Block Diagram of PLL

2. CIRCUIT DESCRIPTION

2.1 Current Starved VCO

Figure 2 shows the schematic of five stage current starved VCO. The schematic shows that there are five inverter stages cascaded in the middle which produces anti high gain at the output of the VCO. There is two current starved circuits placed in the upper part (PMOS) and lower part (NMOS). The drain current is same between two MOSFETs placed in the leftmost which behaves as current sources. It means the inverter is current starved.

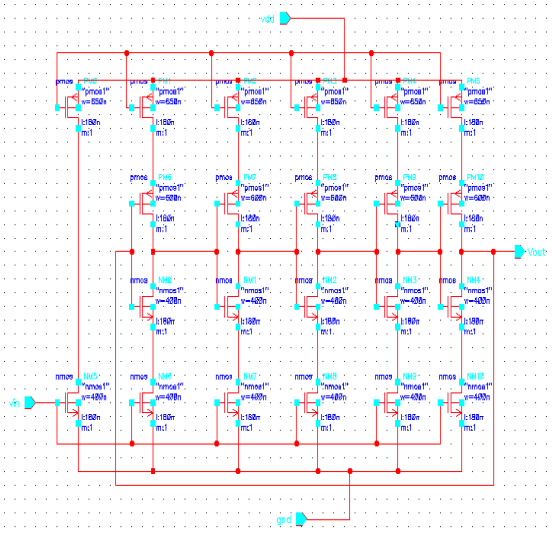

Fig 2: Designed Five Stage Current-Starved VCO

In such designed VCO basically five inverter stages are cascaded. Now the sizing of PMOS & NMOS transistors is done by the following equations given below.

2.2 Test Circuit

In order to check the functionality of designed current-starved VCO, a test circuit is made using the symbol of VCO schematic cell. A ramp input is applied at input terminal of VCO and output is taken from V_{out} terminal. Figure 3 shows the test circuit of the VCO.

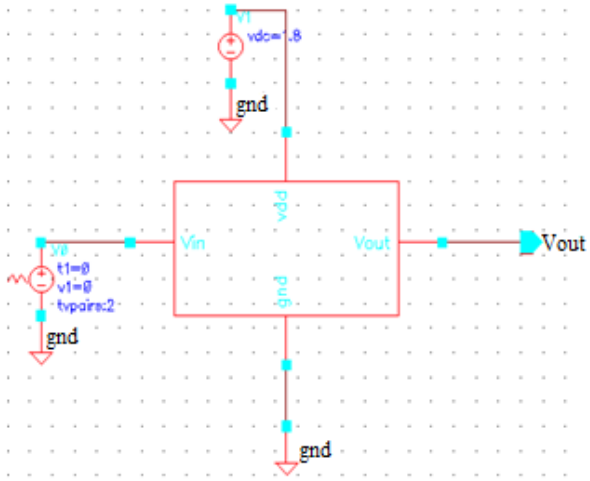

Fig 3: Test Circuit of VCO

2.3 Design Equations for VCO

The sizing of each MOSFETs in the CMOS circuit can be done using the design equations, consider the simplified single stage inverter circuit of VCO shown in figure 4.

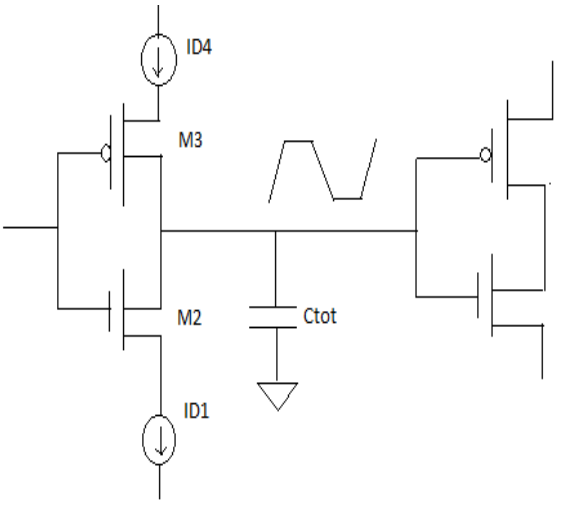

Fig 4: Single-Stage Inverter Circuit of VCO

Total Capacitance can be calculated as [5]:

$$C_{tot} = C_{out} + C_{in} = \frac{5}{2} C_{ox}(W_P L_P + W_n L_n) \quad (1)$$

Where gate-oxide capacitance is represented as C_{ox},

$$C_{OX} = \frac{\in_r * \in_0}{t_{ox}} \quad (2)$$

Charging time to charge C_{tot} for a constant current I_{D4} can be given as:

$$t_1 = C_{tot} * \frac{V_{SP}}{I_{D4}} \quad (3)$$

And discharging time to discharge C_{tot} for a constant current I_{D1} can be given as:

$$t_2 = C_{tot} * \frac{(V_{DD} - V_{SP})}{I_{D1}} \quad (4)$$

Total time when ($I_{D4} = I_{D1} = I_D$) can be given as:

$$(t_1 + t_2) = C_{tot} * \frac{V_{DD}}{I_D} = \frac{1}{T_d} \quad (5)$$

Frequency of oscillation can be given as [8]:

$$f_{osc} = \frac{1 * T_d}{N} = \frac{I_D}{N * C_{tot} * V_{DD}} = \frac{V_{DD}}{2} \quad (6)$$

Where T_d represent delay in time. f_{osc} will be equal to f_{center} if

$$V_{inVCO} = \frac{V_{DD}}{2}, I_D = I_{D\,center}$$

N can be selected according to design. Drain current can be formed as:

$$I_{Dcenter} = N * C_{tot} * V_{DD} * f_{center} \quad (7)$$

The size of Current Starved Circuit can be calculated as [7]:

$$I_{Dcenter} = \frac{\beta(V_{gs} - V_{thn})^2}{2} \quad (8)$$

Where

$$\beta = \frac{K_p * W}{L} = \frac{\mu * C_{ox} * W}{L}$$

3. SIMULATION RESULTS

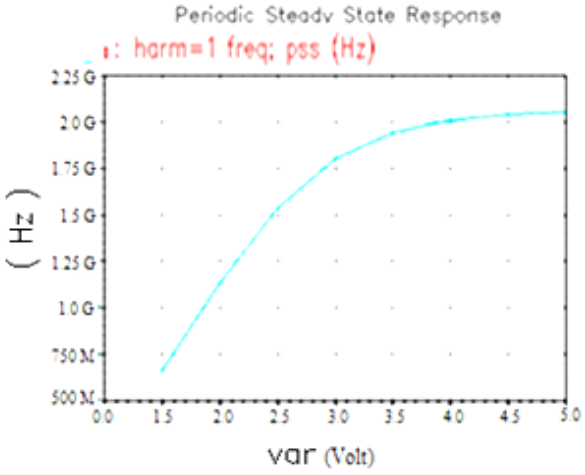

Fig 5: Oscillation Frequency Vs Control Voltage Plot

The plot in figure 5 shows the variation of oscillation frequency according to the control voltage at input. This shows the range of frequency upto which the plot is linear. The plot is linear in the range of (665.7MHz-1.128GHz).

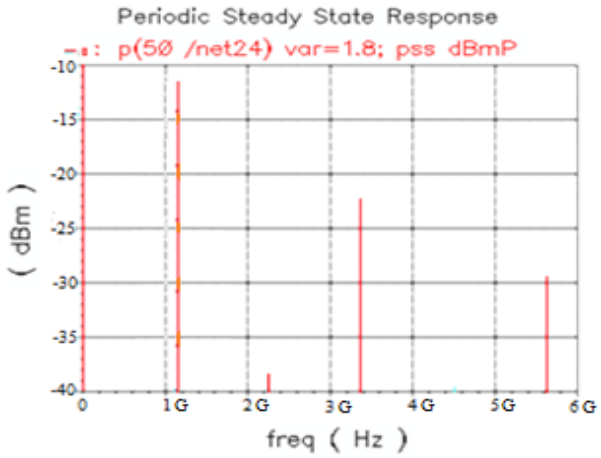

Fig 6: Output Power Vs Oscillation Frequency

The plot in figure 6 shows that the output power is -12dBm for Supply voltage of 1.8V.

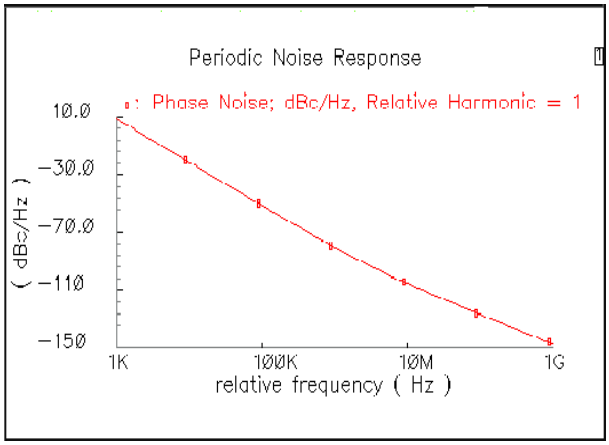

Fig 7: Phase noise Vs frequency

The plot in figure 7 shows that the phase noise is -105dBc/Hz @10 MHz offset.

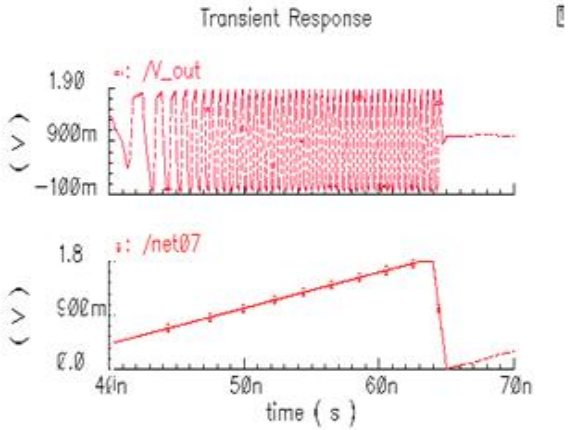

Fig 8: Output voltage Vs Time

The plot in figure 8 shows the transient response of the VCO which is in the form of oscillations.

Table 1. Comparison Table for Performance of Different VCOs at 0.18um Technology

Topology	Supply Voltage (Volt)	Centre Frequency/ Oscillation Frequency Range (GHz)	Phase Noise (dbc/Hz)	Power Dissipation
Ring VCO [6]	2.0	4.3-6.1	-88@ 1MHz	80mW
Ring VCO [9]	1.8	5.0	-82@ 1MHz	135mW
Current Reused LC-VCO [11]	1.8	3.1	-102@ 1MHz offset	4.32mW
Ring VCO [15]	1.8	2.3-2.8	-94.6@ 1MHz	10.1mW
Ring VCO [16]	1.8	3.125	-91@ 1MHz	12.6mW
This Work	1.8	665.7-1.128	-105@ 10MHz	-12dbm

4. CONCLUSION

Designed VCO is operating in the frequency range of 665.7MHz-1.128GHz.The phase noise is (-105dBc/Hz at 10MHz) and power dissipation is (-12dBm) which is very low as compared to other VCOs. The designed VCO can be used for GSM application and suitable for designing synthesizer circuit using PLL. Such technique can also be applied to other low voltage analog circuits and RF circuits to improve their performance.

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