Comparative analysis of Clock gated Data Look Ahead and Conditional Capture Flip-Flops and their area of Applications

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ABSTRACT
Flip-Flops are off many types. Choosing the correct type FF for any application is very important to achieve high performance. the data look ahead d Flip-Flop (DLDFF) from the family of master-slave type is compared with pulse triggered conditional capture Flip-Flop(CCFF).The effect of clock gating on the performance of these Flip-Flops are analyzed. The two Flip-Flops are compared, with clock gating for power and delay and their field of application is determined. Our simulation results in 0.18µm CMOS technology in HSPICE indicates that DLDFF, for various load values 75% power and 60% delay reduction than DFF due to gating.but Clock Gated CCFF consumes more power on increasing load. Hence for applications that include large load, DLDFF will be the best choice. CGCCFF works well on high frequencies applications with 75% power reduction and 60% higher performance than CCFF. A 8-bit synchronous counter is implemented DLDFF and CGCCFF saves 38% and 15% power consumption on clock gating than DFF and CCFF counterparts. The P_{avg} obtained for CGCCFF is proved as very much high when compared to DLDFF due to the increased load in couter. Hence it is determined that DLDFF is works well on large circuits and CGCCFF for high frequency applications.

General Terms
Master-slave, Pulse generated, Flip-flops

Keywords
Clock gating, Data look ahead, conditional capture, Young's architecture, Low power.

1. INTRODUCTION
Flip-flops are the basic elements used in digital VLSI for storing information and they are the fundamental building blocks for all sequential circuits[9]. Flip-flops, have their content change only either at the rising or falling edge of the enable signal. But, after the rising or falling edge of the enable signal, the flip-flop's content remains constant even if the input changes or not. Typically they consume a large amount of power because they are clocked at the system's operating frequency. Careful design of the flip-flop is important to a low power VLSI system. The energy dissipation of the flip-flop can be divided into two components: 1. Clock energy 2. Data energy.The 1st component is the energy dissipated when the flip-flop is clocked while the data of the flip-flop is unchanged. The second component is the additional energy required to write a data to the flip-flop[12]. When the data value is constant, signal gating techniques are employed to suppress unwanted switching activities from propagating forward to avoid unnecessary power dissipation.

In a synchronous digital chip, the clock signal is generally one with the highest frequency[10]. The clock signal typically drives a large load because it has to reach many sequential elements distributed throughout the chip. Therefore the clock signals have been a notorious source of power dissipation. In high performance microprocessors, the clock dissipation may take upto 40% of total power dissipation[1]. Also the clock signal carries no information content since it is predictable. It serves the purpose of synchronization. the most popular method for power reduction of clock signals is called clock gating. When the clock signal of a functional module is not required for some extended period, a gating function is used to turn off the clock feeding the module. But the gating signal should be enabled and disabled at a much slower rate compared to the clock frequency. Clock gating saves power by reducing unnecessary clock activities inside the gated module.

Major configurations of designing a Flip-flop are Master slave and pulse triggered flip-flops. The different gating techniques that can be applied to the above two configurations will be analyzed.

2. GATING IN MASTER-SLAVE AND PULSE TRIGGERED FLIP-FLOPS

2.1 Data Transition Look Ahead D Flip-Flop
Flip-flops, have their content change only either at the rising or falling edge of the enable signal. But, after the rising or falling edge of the enable signal, the flip-flop's content remains constant even if the input changes[1]. In a conventional D Flip Flop, the clock signal always flows into the D flip-flop irrespective of whether the input changes or not. Part of the clock energy is consumed by the internal clock buffer to control the transmission gates unnecessarily. Hence, if the input of the flip-flop is identical to its output, the switching of the clock can be suppressed to conserve power.

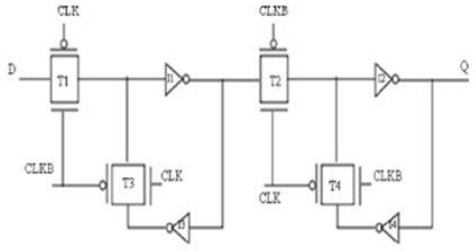


Fig 1: Conventional D Flip-flop

The sub-nano pulse generator used in the existing DLDFF circuit in [2] consumes around 22% of the total power . This

block can be overcome in our proposed DLDFF in figure 2 and the result shows a better improvement in power and also in performance.

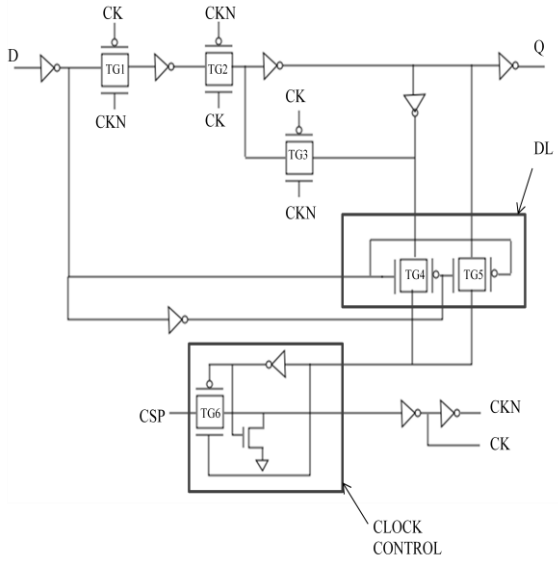


Fig 2: Proposed Data transition look ahead D flip-flop

2.1.1 Logic Gating

Figure.2, shows the proposed data transition look ahead D flip flop. The transmission gates TG4 and TG5 in data look ahead block do the data transition look ahead. It compares the hold data at the output with the respective input data and enables the flip flop to write the data, accordingly. The DL block act as an XNOR gate. For example, when D = Q = 1, the clock is inactive and transmission of data is not required. But, when D = 1, Q = 0, the clock is enabled and data gets transmitted.

2.1.2 Clock Gating

In Figure.2, the Clock control block consists of the transmission gate TG6 followed by an NMOS transistor. The clock control signal [3] depends on the DL's output. The input to the clock control is given by the external clock CSP and divides into CK and CKN.

2.1.3 Operation:

A DLDFF is triggered by the positive edge of the clock (CSP). When an input data D is the same as the holded outpu data Q, the DL circuit makes P1 to low. This turns the TG in the clock gating circuit to off. Because of that, CK and CKN do not transmit. CK and CKN transmit only when D and Q are different. When D changes to a value different from Q, P1 1st changes to 1. Next, when CSP rises, CK also rises and changes. Then, P1 again changes back to 0 since D and Q are the same again. This immediately makes CK low. Therefore, a DLDFF consumes less power than a conventional one, because CK is inactive when there are no data transitions.

2.2.Pulse Triggered Conditional Capture Flip-Flop (CCFF)

Pulse-triggered FF has been considered a popular alternative to the conventional master–slave-based FF in the applications of high-speed operations. More than the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A Pulse triggered flip-flop consists of a pulse generator for generating pulse signals and a latch for storing data. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF.

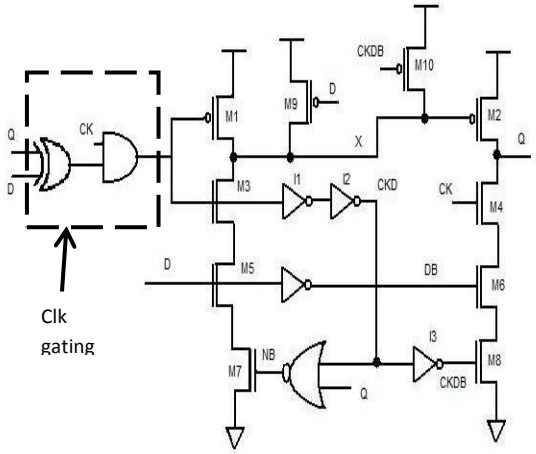


Fig 3: Clock gated conditional capture D Flip-flop

The schematic diagram of Clock Gated Conditional Capture Flip-Flop is shown in the Figure 3 [4] & [5]. The flip-flop uses a NOR gate and inverters I1, I2 and I3, which decide the width of the transparency period. The NOR gate is controlled by the output of the FF, which in turn makes node x to discharge or precharge. The flip-flop captures each transition and remains the data until next discharge path happens for precharge nodes.

2.2.1 Logic Gating

In the CCFF the internal precharge nodes have transitions only when the outputs need to be changed, as described later in operation principle. If both input and output are having identical logical values, the internal precharge node is held high, allowing no transitions to occur and power dissipation except for the clock path. This makes to a significant power reduction during latching operations.

2.2.2 Clock Gating

The clock gating circuit consists of XOR and AND gate is also shown in the schematic. Here the D and Q are given to XOR gate and output of XOR gate is given to one of the input of AND gate. The clock is given to another input of AND gate. This circuit allows clock to flow to the CCFF circuit only if the D and Q are different, else if both are same then the clock gating circuit blocks the clock not to flow to the Flip-fl op circuit. The cross coupled inverters at Q are removed in CGCCFF which is present in CCFF because the opaque phase is eliminated by using this concept. The remaining operation of CGCCFF is as same as CCFF

2.2.3 Operation

The operation of CGCCFF is as follows. Now the input D changes from 0 to 1 and the output Q has 0 value, at this moment the clk is low, making the precharge node X to charge upto VDD via M1 transistor, and the input D makes M5 to get on, while the DB makes M6 to remain off. The inverters I1, I2 and I3 produce 1 unit delay at each of its stage.

The CKD holds the high logic for previous CK for 2 unit delay, while CKDB is the inverted 3 unit delay of clock CK. The CKD and Q makes NB to 0v and M7 becomes off. Now the clock clk changes from 0 to 1 and CKD had changed for low logic after 2 unit delay, which makes NB to high logic and turns on M7 and makes the node X to discharge via M3,M5 and M7, and this X makes M2 to turn on and makes Q to VDD. Now this CKD changes from low to high logic after the 2 unit delay, this makes NB to low logic and makes M7 to turns off. Now the clock changes from high to low which pre-charge the node X, and does not make any unnecessary internal transitions.

For the next case, when the input D changes from 1 to 0 and the output Q has logic value 1, at this moment consider clk is at logic value 0, this makes the pre-charge node X to charge to VDD through M1 transistor, and the D makes M5 to get off, while the DB makes M6 to get on. After a 3unit delay the CKDB becomes logic high which makes M8 to be on and also at the same time the CK changes to logic high makes M4 on, now the Q discharges via the path M4, M6 and M8 and Q becomes logic low, then the CK changes to low and disconnects the discharge path.

3. SYNCHRONOUS COUNTER USING YOUNG'S ARCHITECTURE

The conventional synchronous counter shown in Figure 4, in which the output of the combinational logic is given as input to the flip flop, and triggering operation of the FF is monitored by a global clock [6]. The inputs to the FF from the combinational logic block are unconditionally captured at every triggering edge of CLK, regardless of the previous value of the FF to advance system states.

The switching activity of the nth bit in the binary counter is 1/2n, which means that the least significant bit has the maximum switching activity of 1, and the switching activity of the other counter bits reduces by half as their significance increases. There can be a lot of redundant transitions in these storage elements that capture the data whose values are the same as the previous values, particularly for counter bits having higher significance.

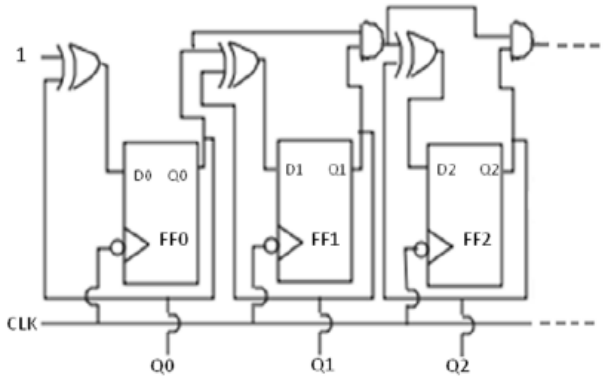


Fig 4: Conventional synchronous counter architecture

We propose a counter using our modified DLDFF and CGCCFF circuits in a power efficient counter architecture [7]. The 8 bit synchronous counter architecture shown in Figure 5 is based on the conditional pulse synchronous timing principle [7]. The counter consists of 8 Local Clock Generator (LCGs)

and 8 flip-flops. Flip-Flops storing counter bits (Q0-Q7) are triggered at the falling edge of a set of local pulsed clocks (IP0-IP7). The output of each flip-flop is sent to the corresponding LCG block, and an inverted version of the output is fed into the input terminal of the flip-flop to implement toggling operation. Two LCGs receive the bits to generate IP0-IP7 to indicate the triggering edges for the associated flip-flops. There are two types of LCGs, they are LCG_L and LCG_H. LCG_L is used for the four lower bits. Nodes IP0-IP3 is selectively pulled down according to the values of Q0-Q2 during the high period of CLK. They are simultaneously pulled up to VDD at the falling edge of clk. The LCG_H is used for higher bits.

4. SIMULATION RESULTS

4.1 Simulation of DLDFF

We use 180nm technology in HSPICE for the implementation of these counters. The supply voltage (Vdd) of 2.5V and a clock frequency (*f*clk) of 500MHz is used. Figure. 6 show the output waveform for the proposed DLDFF. It is observe that the power consumption of the DLDFF is 58% less than the conventional D Flip. And also, the performance of the DLDFF increases by 50% than the DFF.

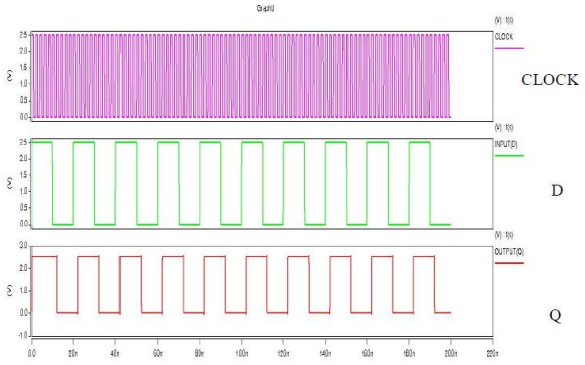
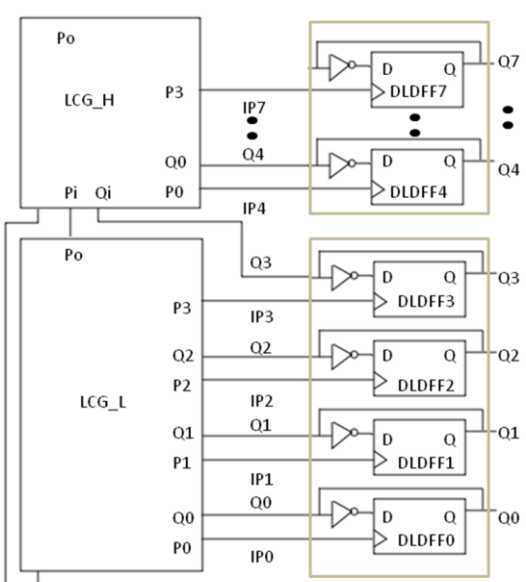


Fig 5: Synchronous counter using young's architecture

4.2 Simulation of CCFF and CGCCFF

The simulation waveforms for CCFF and CGCCFF are shown in Figure 7 and Figure 8 respectively, which is obtained with 2.5V in 180nm CMOS technology at room temperature using HSPICE. **Fig 6: Output Waveform for the DLDFF**



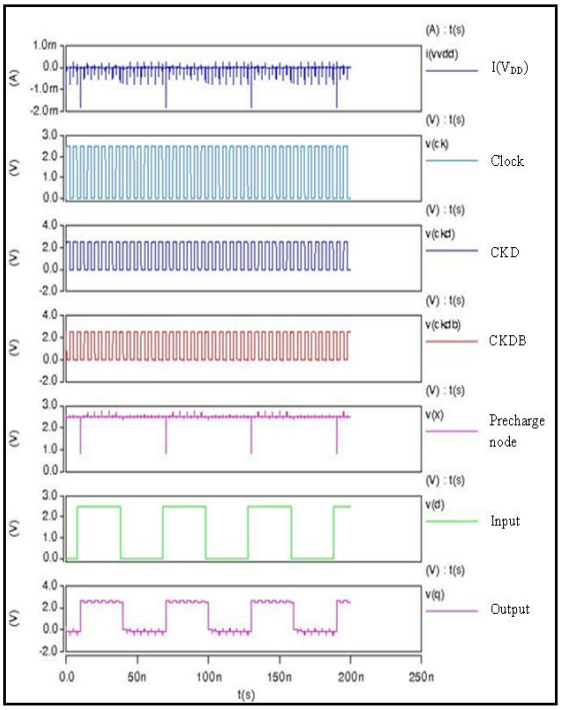


Fig 7: Simulated waveforms for Conditional capture flip-flop (V_{DD}: 2.5v, C_L: 10fF)

Figure 7 shows the simulated waveforms for the CCFF. Here we can observe unnecessary switching occurred due to clock signal even the input and output are at same logic, which gives glitches at the output[11]. Due to these unnecessary switching's the circuit consumes high power.

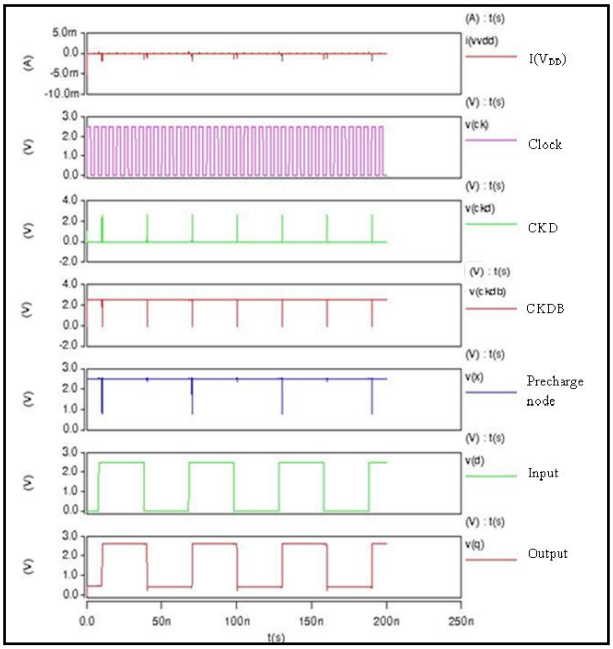


Fig 8: Simulated waveforms for Clock gated Conditional capture flip-flop (V_{DD}: 2.5v, C_L: 10fF).

Figure 8. shows the simulated waveforms for the CGCCFF circuit. Here it is observed that only if there is a change in input and output, then only the clock gets propagated to the FF and there is a discharge path in internal pre-charge node. Thus Q captures the D so the clock power consumption is reduced through clock gating circuit.

5. COMPARITIVE ANALYSIS

5.1 Delay Analysis

Figure 9. shows the relation between capacitive load and propagation delay for DFF and DLDFF. The results obtained indicates that the gated flip-flop provides around 75% less delay when compared to DFF. Figure 10. signifies the C_{load} vs t_{pd} relationship between CCFF and CCFF with CG. It is proved that the delay increases slightly (7%) with the application of clock gating technique. This is due to the additional circuitry added for clock gating.

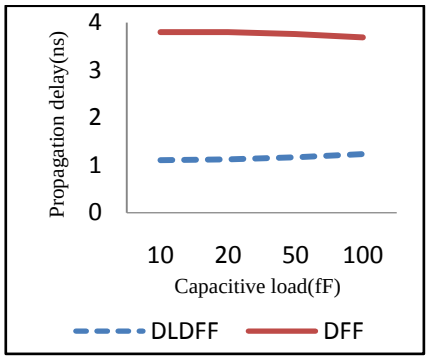


Fig 9: C_{load} vs Average propagation delay for DLDFF & DFF (with supply voltage: 2.5V, Freq= 200MHz)

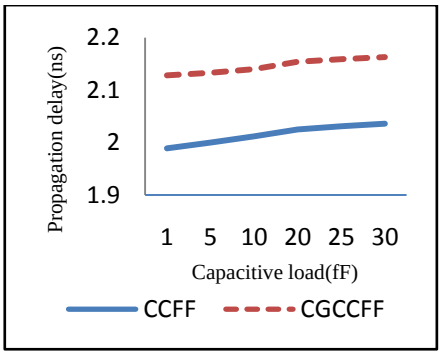


Fig 10: C_{load} vs Average propagation delay for CCFF & CGCCFF (with supply voltage: 2.5V, Freq = 200MHz)

5.2 Power analysis

Average power dissipated is measured for various values of load. Figure 11 shows the relation between capacitive load and $P_{avg.}$ it is shown that DLDFF provides a significant reduction in power consumption when compared to DFF. It consumes nearly 60% less power when compared to DFF. The P_{avg} vs C_{load} relationship is not linear. As C_{load} increases there is a much difference in consumption of power between both of it. i.e. CCFF consumes more power than CGCCFF till 20Ff and for 25Ff consumption of power for both becomes almost equal, further increase in C_{load} makes CGCCFF to consume more power than CCFF. Hence it is clear that clock gating will be effective in CCFF only when the capacitive load is small.

Figure 13. shows the relation between input clock frequency vs. average power consumption for both CCFF and CGCCFF [8]. At 50MHz the power consumption for both FF consumes almost equally till 90MHz, further increase in frequency results drastic increase in power consumption for CCFF but less consumption for CGCCFF. Figure 14 shows the relation

between input clock frequency vs. Average propagation delay for both CCFF and CGCCFF. At 50MHz the CCFF has more delay than CGCCFF, further increase in frequency results almost same value up to 200MHz and after increase in frequency results the reduced delay for CGCCFF than the CCFF.

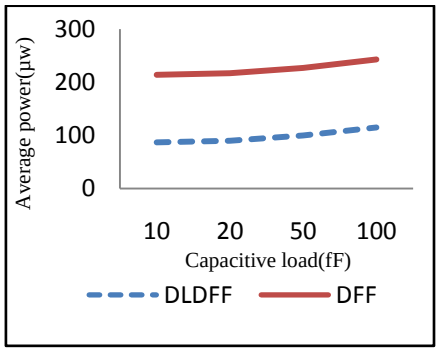


Fig 11: C_{load} vs Average power for DLDFF & DFF (with supply voltage: 2.5V, Freq = 200MHz)

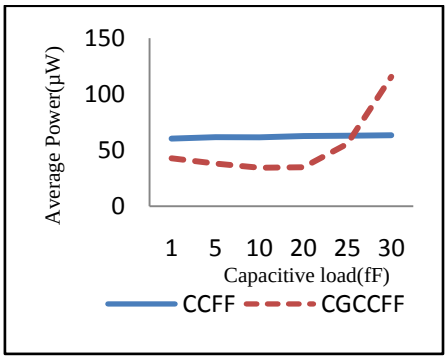


Fig 12: C_{load} vs Average power for CCFF & CGCCFF (with supply voltage: 2.5V, Freq = 200MHz)

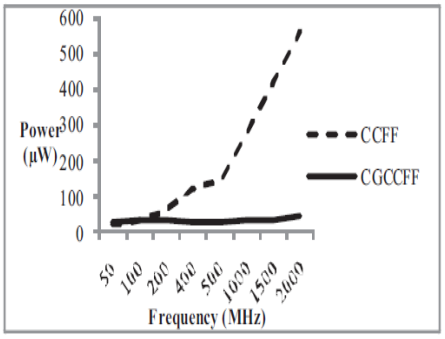


Fig 13: Frequency vs Average power for CCFF & CGCCFF (with supply voltage: 2.5V, C_{load} = 10fF)

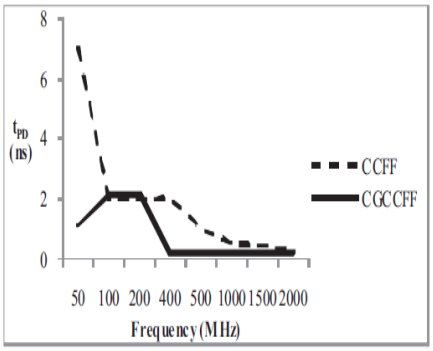


Fig 14: Frequency vs t_{pd} for CCFF & CGCCFF (with supply voltage: 2.5V, C_{load} = 10fF)

Figure 13. shows the relation between input clock frequency vs. average power consumption for both CCFF and CGCCFF [8]. At 50MHz the power consumption for both FF consumes almost equally till 90MHz, with further increase in frequency cause drastic increase in power consumption for CCFF but less consumption for CGCCFF. Figure 14 shows the relation between input clock frequency vs. Average propagation delay for both CCFF and CGCCFF. At 50MHz the CCFF has more delay than CGCCFF, further increase in frequency results almost same value up to 200MHz and after increase in frequency results the reduced delay for CGCCFF than the CCFF.

Figure 15 shows the output waveform for 8bit synchronous counter implemented using young's architecture using CCFF and CGCCFF as flip-flops where output bits varying from Q0-Q7. Figure 16 summarizes the comparison results for the overall power consumption of 8 bit counters implemented using DFF, DLDFF, CCFF and CGCCFF flip-flops .DLDFF provides around 38% power reduction than DFF where CGCCFF provides 15% reduction in power than CCFF. The average power consumed by both CCFF and CGCCFF flip-flops are greater when compared to DFF and DLDFF. This is because the counter circuit implies large amount of load and CGCCFF consumes more power with the increase in load.

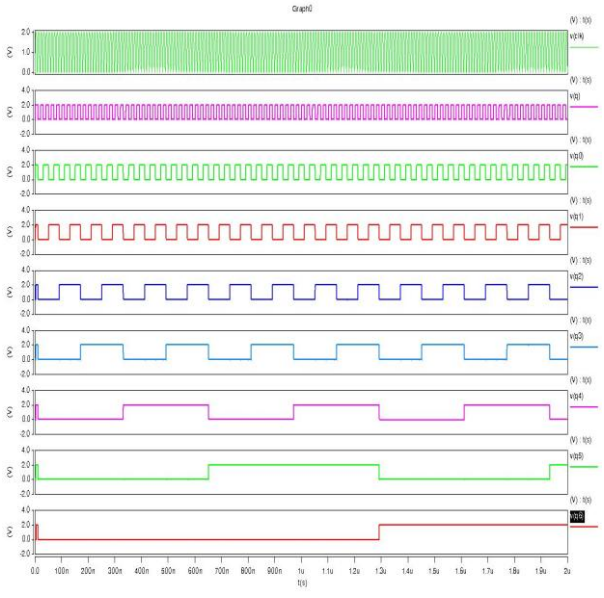


Fig 15: 8 Bit Counter output (VDD – 2.5V, C_L – 10Ff, F_{CLK}–400MHz, t_r/t_f – 10ps/10ps)

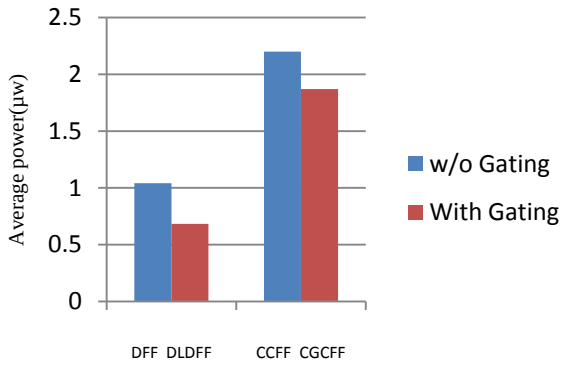


Fig 16: Power consumption of 4-bit synchronous counters using Young's architecture implemented in DFF, DLDFF, CCFF and CGCCFF

6. CONCLUSION

The comparative analysis explains the field of application for the flip-flops under study. The Data look ahead D Flip-Flop will be best suited for large circuits since it can drive very large loads efficiently. It consumes only 40% of total power with around 75% reduction in delay. The clock gated conditional capture flip-flop will work efficiently under high frequency applications provides around 75% power reduction. It is also proved that it has very less delay for high frequencies provided that only minimum amount of load connected to it.

7. REFERENCES

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