Design of Digital Filter using Low Power and Area Efficient SQRT CSLA

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ABSTRACT
The demand of delivering faster, portable and highly reliable products is the major goal of low power VLSI subsystems and it cannot be maintained in all the situations. But it can be optimized to a certain extent by controlling some of the factors. Design of area and power efficient high speed data path logic systems are one of the substantial researches and the most crucial parameter that requires ultimate attention is power consumption. With high power dissipation the reliability of the product is very much degraded. The second concern depends on area. Area should also be taken into concern for low power applications. Adders are designed in such a way which can effectively reduce the propagation delays, which is the major cause of power consumption. Carry Select Adder (CSLA) is one of the fastest adders used in many data processing processors to perform fast arithmetic functions. The structure of conventional CSLA is modified to achieve low power and area. This work proposes the development of improved SQRT CSLA from conventional SQRT CSLA and realization of digital filter using this improved SQRT CSLA. This improved SQRT CSLA is simulated for 16,32,48,64 and 128–b using Xilinx/Mentor Graphics tool. Its performance is measured and compared with conventional SQRT CSLA in terms of area and power.

Keywords
CSLA, SQRT CSLA, BEC.

1. INTRODUCTION
In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or 1's complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor. Other signed number representations require a more complex adder

.In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1] and [2]. However, the CSLA is not area efficient because it uses multiple pairs of (RCA) Ripple Carry Adders to generate partial sum and carry by considering carry input cin=0 and cin=1,which is also duplication of adders which makes the size to increase, then the final sum and carry are selected by the multiplexers (mux).

2. CONVENTIONAL SQRT CSLA
In figure 1, the conventional SQRT CSLA is shown. It has five groups of different size RCA. The area evaluation of each bit starting from 16, 32, 48, 64,128-b in which specify the area values. It has four stages of carry select adder in which the addition takes place in the stages by keeping cin=0 and cin=1which is the normal working of carry select adder. Due to this the duplication of adders takes place which is a great disadvantage in this adder. Even though the time spending to propagate the carry is used to calculate the time used to construct an extra bit at each stage which is the main characteristic change that involves in SQRT CSLA when compared to normal CSLA. The area makes the circuit to be big and when it comes till 128-b the number of duplicate adders which is used to calculate the value with cin=1 is large and occupies large number of logic gates used in this adders. This is the extension of normal Ripple Carry Adder [7] and [8]. Instead of having the same no of bits at the each stage the no of bits at the preceding stages increase.

The time spent for propagating the carry at each stage is used to calculate the increase in no of bits in the each stage. This is the main difference between normal CSLA and the SQRT CSLA. Due to the structure even though there may be reduction in time the area and power will be increased which is the main factor to be controlled in the low power design [9]. So changes are made to avoid the bottle neck and area efficient design can be obtained [10].

The groups that are subdivided as a,b,c,d these groups are consider as having full adders while their correct sum and the carry are obtained using mux selection. The mux selection is a major process involved in this adder by giving the correct sum and carry.

3. IMPROVED SQRT CSLA
From fig.1 it is shown that the structure of the conventional SQRT CSLA can be altered to obtain a structure which is area efficient and power efficient. The alternate way is to change one of the ripple carry adder into BEC which reduces the number of logic gates and the number of transistors used are reduced which can make the circuit more efficient. The BEC is replaced with n+1 bit BEC which is used to store the value if the carry is one. If the sum value is totally balancing and doesn't have a carry then the n+1 th bit is not needed and the value is stored as zero. When the sum

value is obtained with the carry one this extra bit is needed is store the value. The groups a,b,c,d of fig 4, the first full adder with the conventional SQRT CSLA is changed with the half adder followed by the full adders in each full adder and the one of the RCA is replaced with n+1 bit (BEC). The number of the logic gates is reduced when compared to the number of logic gates in the conventional SQRT CSLA. Each groups carry is given to the next group and the final sum and carry is generated with the help of mux.

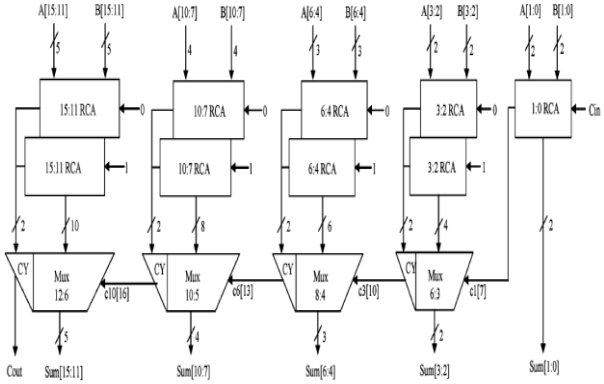

Fig 1: Conventional 16-b SQRT CSLA [4]

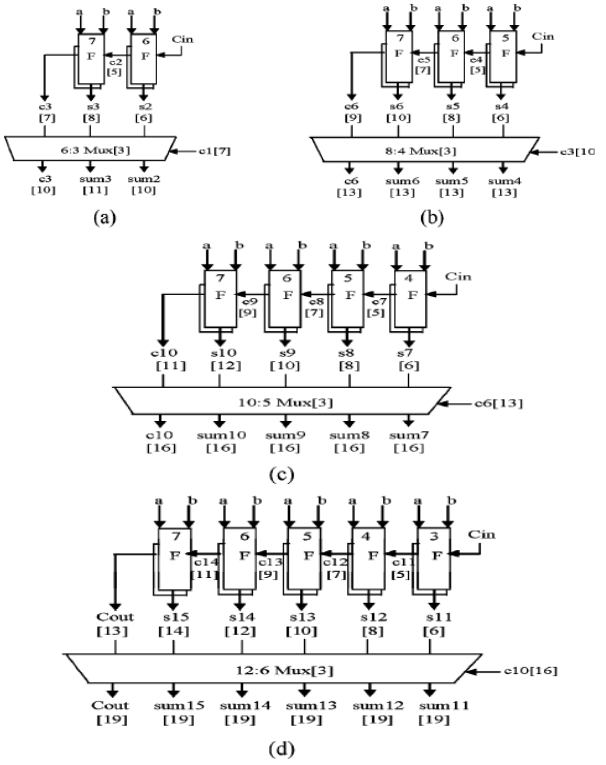

Fig 2: Groups of Conventional SQRT CSLA

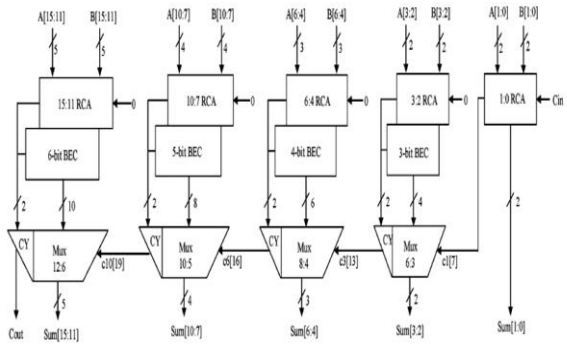

Fig 3: Improved 16-b SQRT CSLA [1]

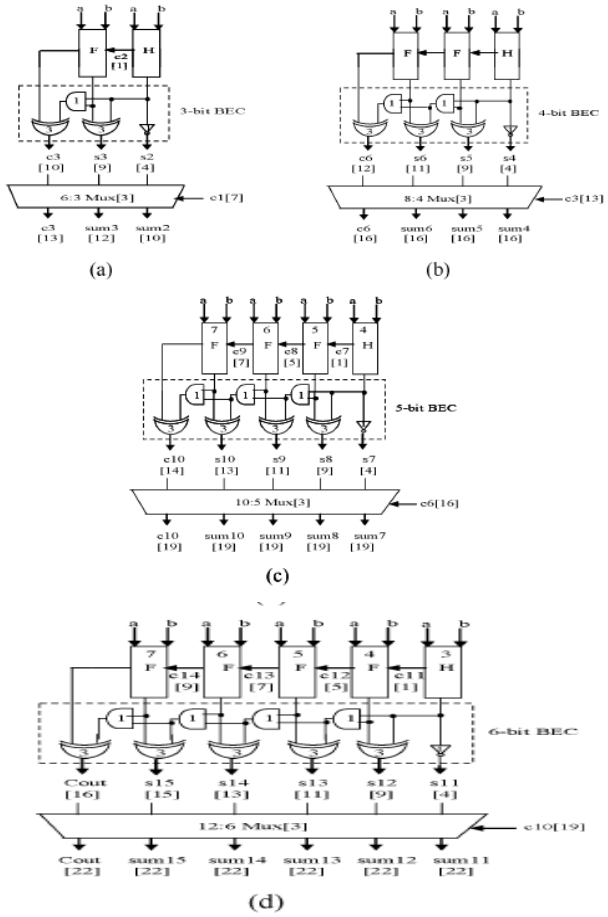

Fig 4: Groups of Improved SQRT CSLA

4. BINARY TO EXCESS 1 CONVERTER

The main idea of this work is to use BEC instead of the

Ripple Carry Adder with cin =1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit (RCA) Ripple Carry Adder, an n+1 bit BEC is required. A structure and the function table of a 4-b BEC are shown in fig.5 and table 1 respectively. Fig. 6 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux is B3, B2, B1, and B0 and another input of the mux is the BEC output. This produces the two possible partial results in parallel and

the mux is used to select either the BEC output or the direct inputs according to the control signal cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols ~ NOT, & AND ^XOR).

X0=~B0,X1=B0^B1,X2=B2^(B0&B1,X3=B3^(B0&B1&B2)

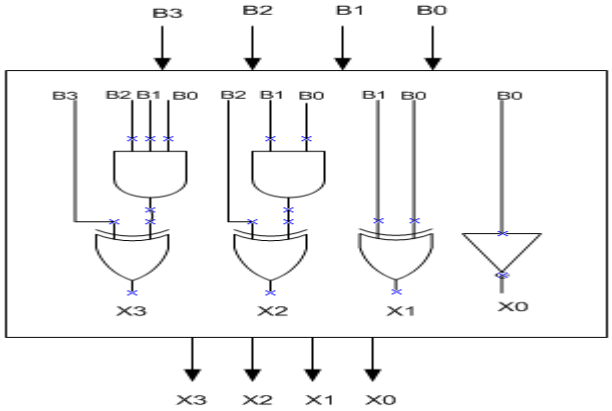

Fig 5: Structure of 4-bit BEC [1]

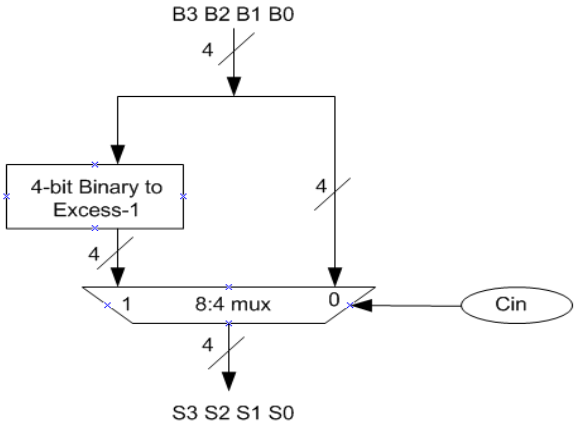

Fig 6: 4-bit BEC with 8:4 mux

Table 1. Functional Table of Four bit BEC

B[3:0]	X[3:0]
0000	0000
0001	0010
.	.
.	.
.	.
1110	1111
1111	0000

5. SIMULATION RESULTS

The simulation results are verified using Xilinx. The simulation results are given for both conventional and improved SQRT CSLA. The simulation result in the fig 7 consist of both the sum and carry but uses the normal set of Ripple Carry Adder in which the adders are placed parallel and their outputs are obtained by having the cin=0 and cin=1 for the other set of the adder. While the simulation in the fig 8 shows the result of 16-b improved SQRT CSLA which gets the same carry and the sum with one of the parallel adders replaced with BEC logic. The number of logic gates is reduced in improved SQRT CSLA than conventional SQRT CSLA.

The simulation results for 128-b conventional and improved SQRT CSLA are given in the fig 9 and 10 respectively. The same sum and carry are obtained in both the cases but one with the duplication of adders and the other with the BEC logic so as to reduce area and power as mentioned earlier. Area is the major concern in low power design. When area is reduced the other factors such as power will also have a major decrease. Even for 16-bit the area utilization is too large which can increase the area and power also by not satisfying the goal of the low power design .Hence another method is used to reduce this area consumption by using BEC circuitry which further decrease the utilization of area and also power of the circuit. The area utilization summary is obtained in Mentor Graphics using precision RTL in which the availability of the IOS is compared between the avail and used. The number of LUT_S, CLB slices, flip flops or latches is also obtained. From the synthesized report the area usage of improved SQRT CSLA is more efficient than the conventional SQRT CSLA.

Power is also a major concern which relays low power design after area. The power is estimated using Xilinx simulator in which the total on chip power with its junction temperature is obtained. Power is estimated for both the conventional and improved SQRT CSLA. Their comparison is given in table 2.

Table 2. Comparison Table for Area and Power

Word size	Area (LUT'_S)		Power (W)	
	Conventional	Modified	Conventional	Modified
16-b	78	68	2.667	1.309
32-b	169	144	2.668	1.310
48-b	254	198	2.675	1.311
64-b	339	221	2.678	1.312

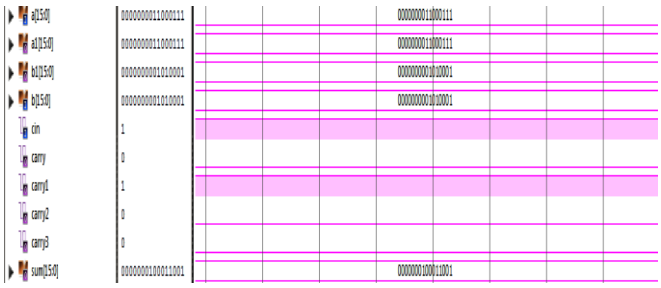

Fig 7: Simulation Result of 16-b Conventional SQRT CSLA

Fig 8: Simulation Result of 16-b Improved SQRT CSLA

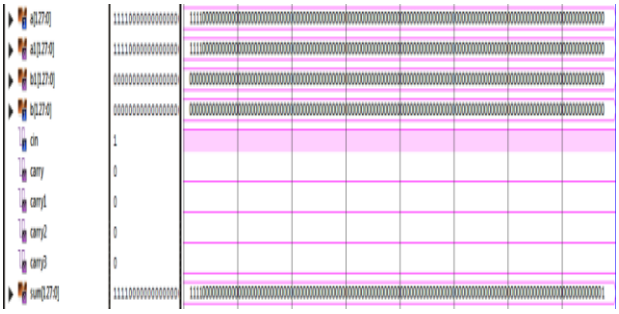

Fig 9: Simulation Result of 128-b Conventional SQRT CSLA

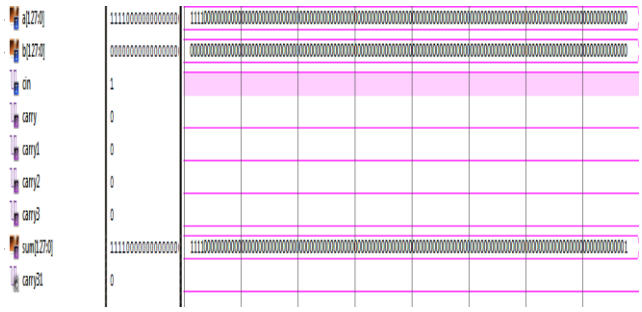

Fig 10: Simulation Result of 128-b Improved SQRT CSLA

6. DIGITAL FILTER DESIGN

A filter is used to modify an input signal in order to facilitate further processing. The most common digital filter is the Linear Time-Invariant (LTI) filter. Designing an LTI involves arriving at the filter coefficients which, in turn, represents the impulse response of the proposed filter design.

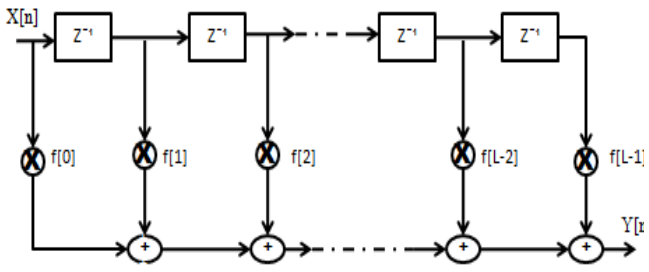

Fig 11: Finite Impulse Response [6]

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These coefficients, in linear convolution with the input sequence will result in the desired output. This adder part is replaced by the improved SQRT CSLA to achieve better performance in terms of area and power [6, 11, 12].

6. CONCLUSION

In this paper, the conventional and improved SQRT CSLA is compared in terms of area and power. The comparison results show nearly 34% decrease in area and 52% approximately in the reduction of power. The obtained results prove that the area and power are reduced in improved SQRT CSLA. This improved SQRT CSLA is useful to design low power and area efficient digital filter. Simulation is done using Xilinx / Mentor Graphics tool.

7.REFERENCES

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