4 Bit Reconfigurable ALU with Minimum Power and Delay

B. Lokesh
VLSI Design, M. Tech
Dept. of ECE
SRM University

K. Dushyanth
VLSI Design, M. Tech
Dept. of ECE
SRM University

M. Malathi
Professor
Dept. of ECE
SRM University

ABSTRACT
Arithmetic Logic Unit (ALU) can be implemented in various ways using different logics. We are proposing an ALU design in which logic gates are implemented using Differential Cascode voltage switching logic (DCVSL). Manchester Carry Chain (MCC) is used to reduce the delay when addition or subtraction is performed in ALU. Using DCVSL logic gates we can obtain complemented outputs without any extra circuitry with zero static power dissipation and rail to rail swing. MCC generates carries parallel to the addition of the inputs, so when adders are cascaded one stage need not to wait for the carry input from its previous stage. Hence the carry propagation delay is reduced. Proposed ALU can perform all logical operations XOR, XNOR, AND, NAND, OR, NOR and some arithmetic operations like addition and subtraction etc...

General Terms
Full adder, arithmetic operations, logical operations

Keywords
ALU, DCVSL, MCC, AND, OR, XOR, NAND, NOR, XNOR

1. INTRODUCTION
ALU is the most essential part in any processor design. It plays a very key role in the performance of the processor. Modern ALUs should be fast and consume less power. This paper presents a high speed low power ALU design which is based on two major techniques DCVSL and MCC. DVSCL is a differential logic in which complemented outputs are obtained by applying complemented inputs. Since complemented outputs can be obtained from it, the number of transistors required will be low. Manchester Carry Chain uses carry generate, carry propagate and carry annihilate functions to generate carries with very less delay.

Rest of the paper organized as follows section 2 presents the implementation of addition and subtraction using two input XOR, XNOR, AND, OR and few CMOS switches; section 3 presents design of reconfigurable ALU and incorporation of MCC in to it; section 4 and 5 presents the results and conclusions.

2. IMPLEMENTATION OF ADDITION AND SUBTRACTION IN ALU
Addition and subtraction are the most commonly used arithmetic operation and speed limiting elements in as ALU. Adders and subtractors are used for performing multiplication and division respectively. The truth table for addition and subtraction with carry input and borrow input respectively is shown in Table 1. Sum and difference are shown in the same column as they are same for the applied inputs.

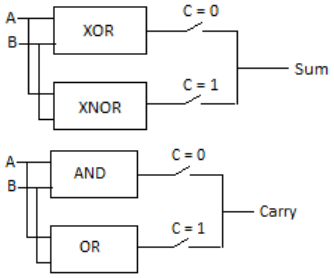
Table 1. Truth table for addition and subtraction

C	A	B	Sum / Difference	Carry	Borrow
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1

By observing the full adder truth table shown in table 1, we can interpret that:

- In the sum column, first four combinations of input and output are XOR operation on A and B when C is at logic ‘0’. Second four combinations of input and output are XNOR operation on A and B with when C is at logic ‘1’.
- In carry column, first four combinations of input and output are AND operation on A and B when C is at logic ‘0’. Second four combinations of input and output are OR operation on A and B when C is at logic ‘1’.
- We can generate borrow in a circuit (which can generate carry) by just complementing the carry input C.

From the above observations, reconfigurable full adder or subtractor is designed as shown in figure 1. Sum can be obtained by performing XOR and XNOR operation on inputs A and B when carry input C is at logic ‘0’ and at logic ‘1’ respectively. Carry can be obtained by performing AND and OR operation on inputs A and B when carry input C is at logic ‘0’ and at logic ‘1’ respectively. Similarly, borrow can be obtained by performing OR and AND operation on inputs A and B when carry input C is at logic ‘0’ and logic ‘1’ respectively.



Sum generation

Carry generation

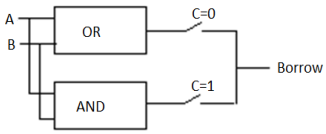


Fig 1: Reconfigurable full adder/full subtractor

3. RECONFIGURABLE ALU DESIGN USING DCVSL LOGIC

Differential cascode voltage switch logic combines two concepts differential logic and positive feedback [1]. This logic requires that each input is provided in complementary format and provides outputs in complementary outputs in turn. Feedback mechanism turns off the load device when not needed. This logic eliminates static power dissipation in steady state and provides rail to rail swing. Basic logic functions can be implemented using DCVSL logic as shown in the figure 2.

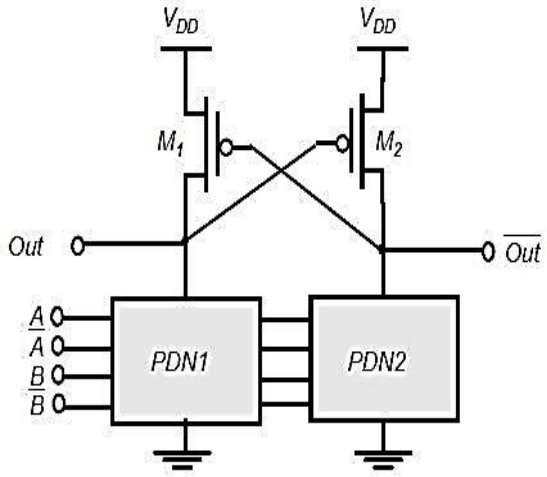


Fig 2: DCVSL XOR and XNOR logic

1-bit ALU implementation using DCVSL is shown in figure 3. In this design ALU is implemented by using two input DCVSL logic gates (XOR, AND, OR) and CMOS switches. This ALU can perform all logic operations on A and B inputs and can perform addition and subtraction on A and B with C as carry and borrow input.

4 bit ALU

3.1.1 Manchester Carry and Borrow Chain

For performing addition in ALU, Manchester Carry Chain is used (MCC). MCC reduces the delay in performing addition, by generating carry at each stage in parallel to the addition. Carries are generated concurrently by using carry generate, propagate and annihilate functions.

Carry generate, $G_i = A_i \cdot B_i$

Carry propagate, $P_i = A_i \oplus B_i$

Carry annihilate, $AN_i = \overline{A_i + B_i}$

From above functions it is clear that at any time only one of the following signals G_i, P_i, AN_i will be at logic '1' C_{i+1} (carry for next stage) is connected to '0' if AN_i is high or to '1' if G_i is high and to the incoming carry C_i if P_i is high. As the addition and carry generation is carried concurrently delay is reduced. From logic module (shown in Figure 3), we can obtain G_i, P_i and, AN_i. So, no extra circuitry is required for generating G_i, P_i and AN_i functions [4].

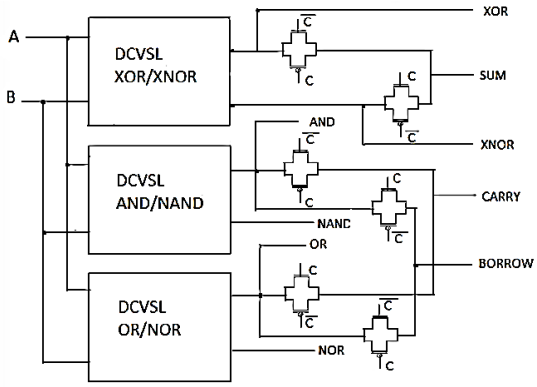
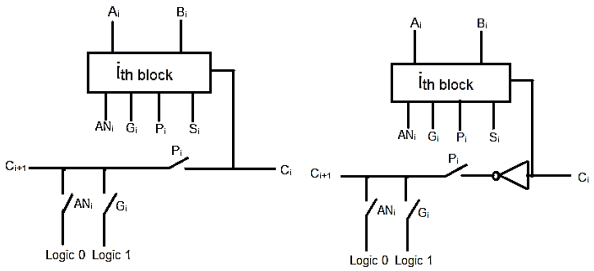


Fig 3: Multi-function /Multi logic module

Similarly, we can implement Manchester Borrow Chain (MBC) by using carry generate, propagate and annihilate functions but carry gets inverted when P_i is high. MCC carry and borrow generation is shown in figure 4.



A) carry for next stage B) Borrow generation

Fig 4: Carry generation using MCC

In figure 6 shows the carry chain implementation using transistors. G_i is complemented as it is given as input to a PMOS transistor (turns on when gate voltage is at logic '0').

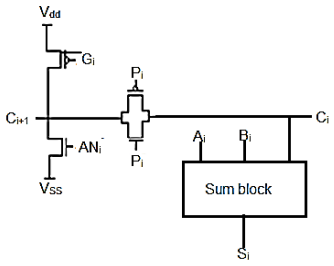


Fig 6: Transistor level implementation of single stage MCC

3.1.2 ALU implementation

For implementing ALU, four modules are cascaded as shown in the figure 7. Manchester carry chain and borrow chain are incorporated in the proposed design. So that delay can be reduced considerably. Carry chain and borrow chain are selected by using the control signal M. when M is at logic '0' carry chain gets activated and addition operation is performed. When M is at logic '1' borrow chain gets activated and subtraction operation is performed. From each module addition as well as logical operation on the inputs can be obtained at the same time. By using multiplexer we can select the required operation [7].

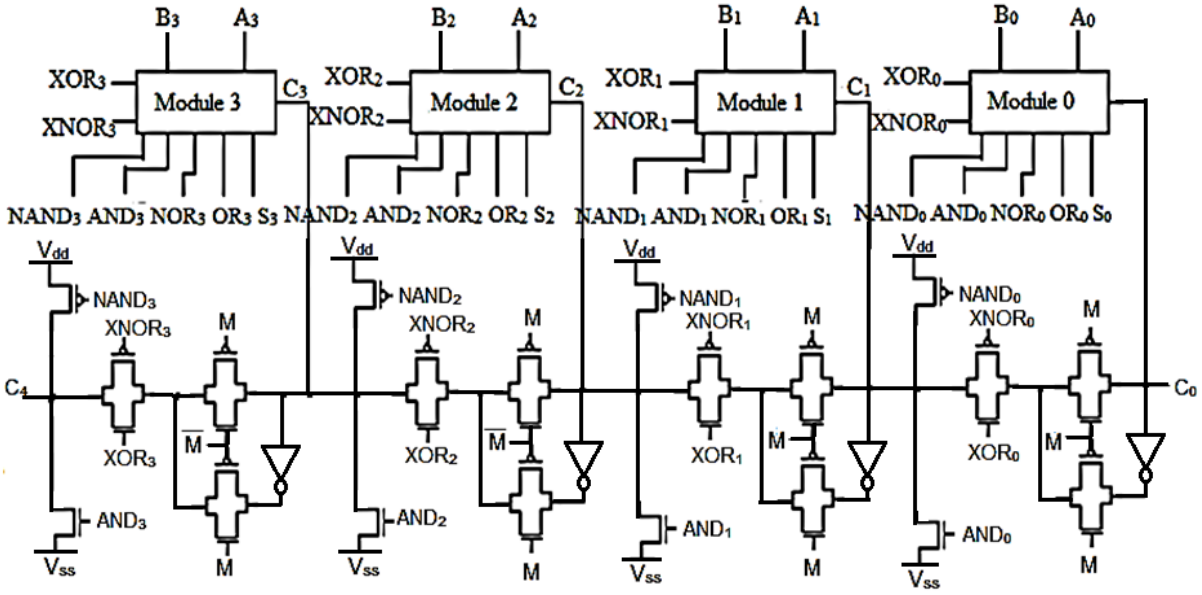


Fig 7: 4 bit ALU using DCVSL logic modules and MCC carry chain

5. RESULTS

4-bit ALU shown in Figure 7 is simulated using SPICE 180nm technology. Waveforms are shown in the Figure 8 and Figure 9. Figure 8 shows output waveforms of logical operation on A_0 and B_0. All logic operations are performed in ALU along with addition or subtraction (shown in Figure 9).

Addition is done when the control signal M is at logic '0' and subtraction is done when M is at logic '1'. The average power consumed and delay in 4 bit ALU is shown in Table 2.

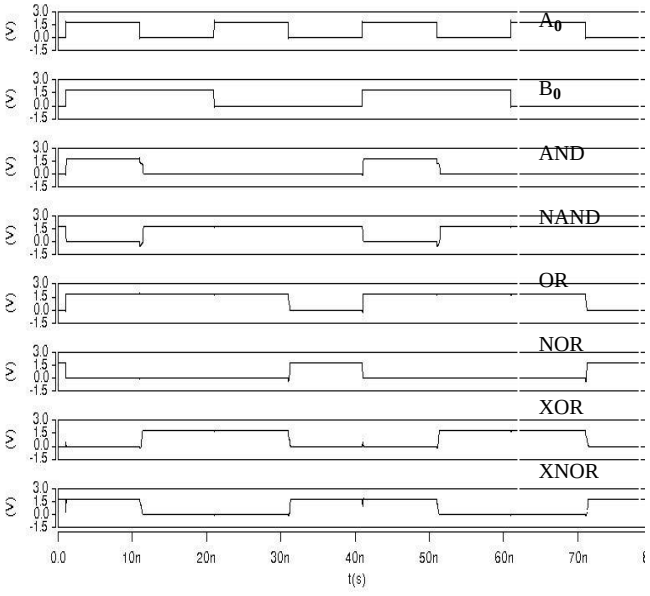


Fig 8: Logical operations on A_0 and B_0

Table 2. Comparisons of power and delay of proposed design with existing design

parameter	CMOS ALU	Proposed model
Power	91µw	65.27µw
Delay	0.5ns	0.3ns

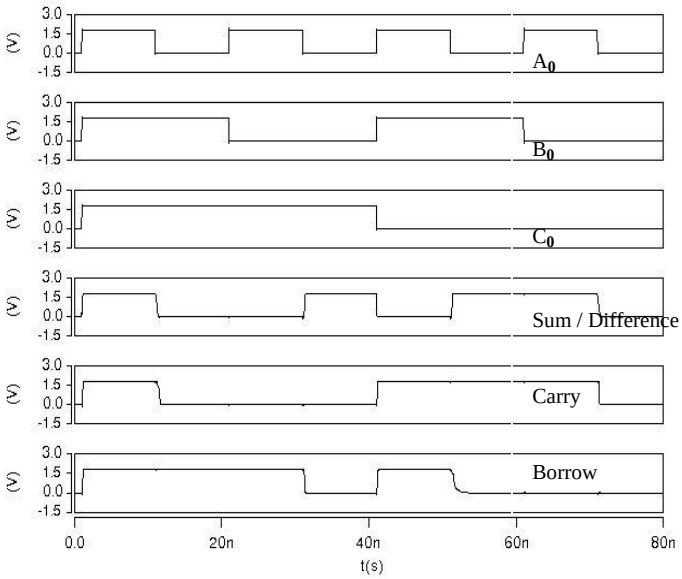


Fig 9: Addition operation on A and B inputs with C as carry input

6. CONCLUSION

From the above discussions and simulation we can conclude that the delay and power consumption reduces considerably when compared to the CMOS ALU.

As the arithmetic as well as all logical operations can be performed concurrently for given inputs, it can be used in

high performance applications where multiple operations need to be performed.

7. REFERENCES

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