Phase Noise Reduction Approach in PLL based Frequency Synthesizer for IEEE1394 PHY Applications

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ABSTRACT
Technology advances have made gigabit signal a viable and attractive. A method to design IEEE 1394 based 1GHz Phase Locked Loop (PLL) system as frequency synthesizer with Low Phase Noise is proposed. A complementary LC oscillator is used to generate the 1GHz oscillation frequency and is divided into lower frequency clock by the feedback frequency divider. The architecture is type II third order charge pump Phase Locked Loop. In order to suppress spurs and reduce ripples on control voltage a third order loop filter is used. Power consumption is significantly reduced by simplifying the circuit structure of digital frequency divider. Advance process of silicon-Germanium BiCMOS (SiGe) is used to integrate high-performance Hetero-junction Bipolar Transistors (HBTs) and MOSFETs actives and passives. This technology has the advantage that its flicker noise (1/f) is very low.

Keywords
Phase Locked Loop, mixed signal simulation, VCO, Frequency divider, passive filter, SiGe.

1. INTRODUCTION
Applications like camcorder, Audio and Video receivers, and Digital Televisions use IEEE1394 serial bus interface for high speed communication and real-time data transfer. The specification of IEEE 1394b-2002 allows a transfer rate of 100Mbit/s, 400Mbit/s and 800Mbit/s. When operating in 800Mbit/s mode, the internal PLL has to provide 1GHz clock for the clock data recovery (CDR) to extract data. The PHY provides the analog transceiver function and requires an external 25MHz crystal driving an internal PLL to generate reference clocks. There are different methods of clock and data recovery that can be applied. For moderate data rates, data can be recovered by oversampling the received signal to identify transitions in the data waveforms. At higher frequencies, techniques operating at or near the data rate are necessary. One method of recovering the bit clock is Surface Acoustic Wave (SAW) filters. Nonlinear processing is required since a Non-Return-to-Zero data waveform has a spectral null at the bit frequency. The disadvantage of this approach is that SAW filters are incompatible with low cost IC fabrication technologies. An alternative approach for generating the recovered clock is to use a PLL. PLLs are widely used for frequency synthesis in communication systems. The design of an analog or mixed signal system frequency synthesizer has lot of tradeoffs among system parameters. The task of the PLLs is also to maintain coherence between the input (reference) signal frequency (F_{ref}) and the respective output frequency (F_{out}) via phase comparison.

There are several important parameters for signals generated by a PLL circuit such as frequency range, frequency resolution, phase noise, spurs, loop bandwidth, switching speed. Other parameters deal with size, power, supply voltage, interface protocol, Temperature range and reliability.

The four basic components of the PLL circuit are voltage controlled oscillator (VCO), the phase-frequency detector and charge pump (PFD/CP), frequency divider (N) and the loop filter (LF). These components are noise sources as well, either the noise created by the blocks due to intrinsic noise sources (thermal, shot and flicker noise), or the noise coupled into the blocks from the external sources such as from the power supplies, the substrate and so on. Most of them are sources of phase noise because the circuit is only sensitive to phase at the point where the noise is injected. Phase noise and Jitter are two related quantities, Phase noise is a frequency-domain view of the noise spectrum around the signal, while jitter is a time-domain measure of the timing accuracy of the period. The noise in the PFD/CP comes from the jitter in the PFD and noise in the output current of the CP. The total noise produced by the CP will be proportional to how long it is ON, while the noise from the PFD will all be in the edges and so will be autonomous of how long the CP is ON. The noise from filter is noise due to resistors and capacitors in the circuit. VCO is responsible for most of the noise at the output of the well designed frequency synthesizers. This is because VCO essentially have a tendency to amplify noise found near their oscillation frequency and any of its harmonics. Even a small noise into a VCO leads to significant changes in its frequency spectrum and timing properties. The noise produced by the frequency dividers is more complicated because it is always followed by some form of edge-sensitive threshold circuit like PFD and the frequency divider noise power varies over time.

Contribution: In this Paper, PLL frequency synthesizer for IEEE 1394b PHY is proposed for a single frequency generation with third order passive loop filter design. In order to obtain better noise performance and lower power consumption to that of Jin-Yue et al., [2] a topology containing a LC oscillator, higher order loop filter and digital frequency divider is proposed. To develop the design, firstly a system model of whole PLL is created, in which the main circuit blocks are represented by the symbol. The operation of these blocks is done without going into the details of architecture choice or transistor sizing. After characterizing the entire system, each block must be defined in more detail and realized in the transistor level. Using SiGe Process Development Kit (PDK) from TowerJazz SBC35 (SiGe60) and National Instruments Advanced Wave Research (NI/AWR) Analog Office and Visual Simulation Suite (VSS) all the blocks and components circuits are realized and simulated. The challenges like gate leakage of MOS capacitor used in loop filter which may cause loop instability and mismatches in charge pump due to stringent voltage headroom requirements is solved in SiGe BiCMOS technology due to use of thick gate oxide MOS device.[1]

Organization: In this paper a comprehensive design of a PLL frequency synthesizer for IEEE 1394b PHY which generates 1GHz clocked is presented. In section 2, Literature survey is performed. In Section 3, loop characteristics and mathematical relationship of loop filter parameters are described. In Section 4 PLL architecture and circuit designs of PLL blocks are described. Section 5 explains simulation results and system performance of the proposed work with the behavior model.

2. LITERATURE SURVEY

Zhu Kehan et al., [1] presented the design of high frequency charge pump PLL for high speed data transfer using SiGe BiCMOS process. The paper expresses the advantages of the SiGe BiCMOS devices over silicon CMOS devices to obtain the loop stability and low phase noises of third order charge pump PLL. Jin-Yue et al., [2] described 1GHz charge pump PLL based frequency synthesizer using Verilog-A modeling. A Four stage Ring oscillator and second order loop filter based design is used the drawback of this tolopology is spurs and other undesirable signals besides phase noise which can severely

affect the performance of the synthesizer. F M Gardner [3] shown switching granularity effects can be ignored if switching frequency go beyond 10 times the loop bandwidth. Also shown salient features of passive filter with current switching and is fundamental paper for designs based on charge pump PLL frequency synthesizer. Xiang et al., [8] presented in his work a low noise sub-sample PLL in which he has eliminated the divider noise without multiplying PD/CP noise by N^2. But in this scheme a large filter capacitor is required for high detection gain i.e. there is a difficulty of integration also there is limited frequency acquisition range. Tamaddon et al.,[11] presented design of PLL based Frequency Synthesizer, to reduce the charge pump current a small filter capacitances are used maintaining a good phase margin and small settling time. Other techniques like use of True Single-Phase Clock (TSPC) logic counter and reduce the VCO gain. However overall performance is improved with better settling time and low power consumption yet there prevail the high frequency phase noises.

3. LOOP CHARACTERISTICS AND MATHEMATICAL RELATIONSHIP OF PARAMETERS

The frequency domain model shown in Figure 1 [2] can be used to drive the mathematical relationship between loop filter parameters.

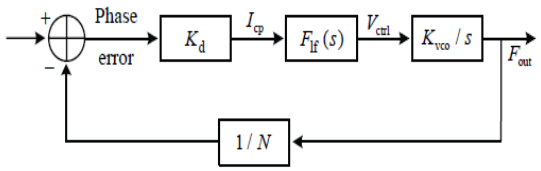

Figure 1: Frequency domain model of Phase Locked Loop

The Transfer function of the PFD/CP, also known as phase detector gain K_d, is $I_{CP}/2\pi$. The loop filter is a low pass filter, it removes the high frequency part of the charge pump output and plays a vital role in the stabilization of the whole loop. F(s) is the transfer function of loop filter. The transfer function of the VCO functioning as an integrator is Kvco/s and that of feedback divider is 1/N. Here, N is the frequency dividing ratio. The open loop transfer function G(s) is given by

$$G(s)=\frac{I_{CP}}{2\pi}.F(s).\frac{K_{VCO}}{s}.\frac{1}{N} \quad (1)$$

Where,

$$F(s)=\frac{s.R_2C_2+1}{s\{s^2.C_1R_2C_2C_3R_3+s[R_3C_3(C_1+C_2)+R_2C_2(C_1+C_3)]+(C_1+C_2+C_3)\}} \quad (2)$$

Where R1, R2, R3 are filter resistors and C1, C2, C3 are filter capacitors

Design for 1 MHz Bandwidth (ω_c) and 60 degree Phase margin (ϕ_{PM})

K_{vco} is chosen as 1.25GHz/V

$K_d = I_{CP}/2\pi$, I_{CP} is the charge pump current = 100µA

N = VCO output Freq / Ref Freq

$$\tau_1=\frac{(\sec\emptyset_{PM}-\tan\emptyset_{PM})}{\omega_c} \quad (3)$$

and $$\tau_2=\frac{1}{\omega_c^2(\tau_1+\tau_3)} \quad (4)$$

Where τ_1, τ_2 and τ_3 are Time constants

$$C_1=\frac{\tau_1}{\tau_2}\frac{K_d}{\omega_c^2N}\sqrt{\frac{1+(\omega_c\tau_2)^2}{(1+(\omega_c\tau_1)^2)(1+(\omega_c\tau_3)^2)}} \quad (5)$$

$$C_2=C_1\left(\frac{\tau_2}{\tau_1}-1\right) \quad (6)$$

$$R_2=\frac{\tau_2}{C_2} \quad (7)$$

As rule of thumb choose $C_3 \le C_1/10$ and $R_3 = 2R_2$

4. PHASE LOCKED LOOP ARCHITECTURE

The general block diagram of the PLL is shown in Figure-2. A conservative topology of CP [3] is used for ease and stability, LF which is third order Low Pass Filter (LPF), VCO and a frequency divider (N) is proposed.

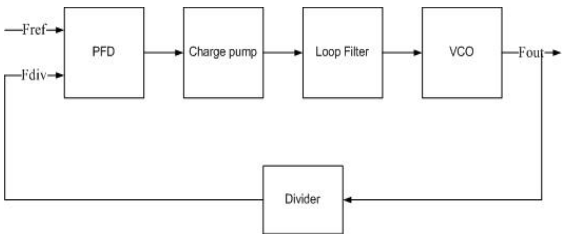

Figure 2: Block diagram of Phase Locked Loop

4.1 Phase/Frequency Detector and Charge Pump

Phase/Frequency detector (PFD) employs sequential logic to create three states and respond to the rising (or falling) edges of the two inputs. Figure 3 shows the behavioral model of the PFD.

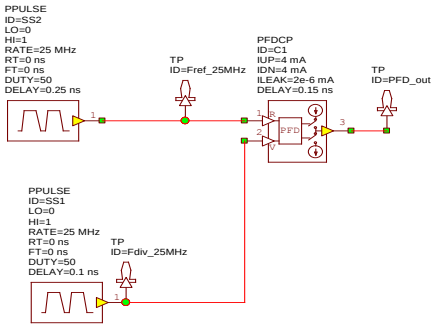

Figure 3: PFD system diagram

The sequential circuit used is edge triggered D-Flip Flop (DFF). The reference frequency (F_{ref}) is 25MHz and other input coming from the frequency divider (F_{div}) is also of same frequency. If F_{ref} leads the F_{div}, the rising edge of the F_{ref} triggers DFF connected to the UP signal and switches it ON and DFF connected to the DOWN signal switches OFF. The UP signal remains ON until the occurrence of rising edge of the F_{div} which triggers the DFF connected to DOWN (DN) signal ON and DFF connected to the UP signal switches OFF. Since PFD compares edges of the inputs, pulse width of the inputs does not matter. Note that a few delay inverters are added in the reset signal path to prevent dead zone problem [9]. Since the switch of the charge pump needs certain amount of time to turn ON and OFF, very small phase difference of F_{ref} and F_{div} cannot be captured (dead zone). In order to solve this problem, a delay time of ΔT is introduced in the reset path. Figure 4 shows the simulation result.

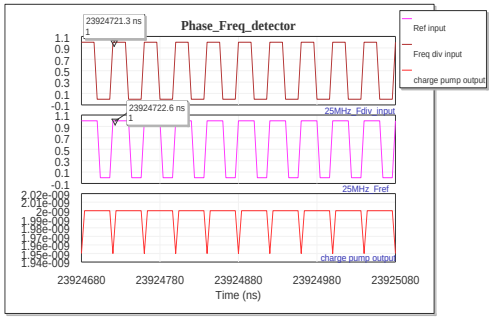

Figure 4: PFD Simulation result

The charge pump is a three position electronic switch [3][10] that is controlled by the logic states of the PFD. The concept diagram of charge pump is shown in Figure 5. When the switch is set in the Up or Down position, it delivers a pump voltage ±Vp or pump current ± Ip to the loop filter which controls the VCO. When the Up signal is high the capacitor C_1 is charged and the control voltage at input VCO changes to pull up VCO frequency. When Down signal is high the capacitor C_1 is discharged and the control voltage at input of VCO changes to pull down the VCO frequency. The significant parameters involved in the design of charge pump are the dynamic range, charge pump current, spurs. The mismatch of the Up or Down current and leakage current at the charge pump output which modulates the control voltage of the VCO is responsible for spurs in the PLL output spectrum. The technique used to reduce the mismatch current is gain boosting structure at the output. This technique allows the Up and Down currents to be constant and reduces current flowing in to the passive filter.

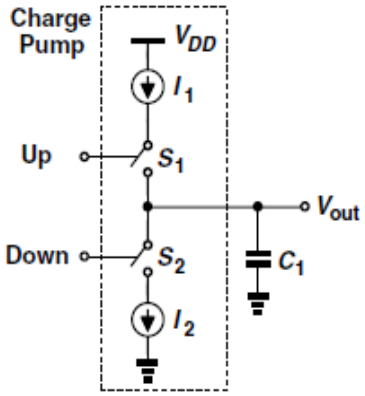

Figure 5: Charge Pump

4.2 Loop Filter

As mentioned in section 3 the values of R_2, R_3, C_1, C_2 and C_3 are determined. The Loop Filter removes the high frequency part of the charge pump's output and plays a very important role in the stabilization of the whole loop which is typically a low pass filter (LPF). A figure 6 show the circuit of loop filter which is passive third order low pass filter.

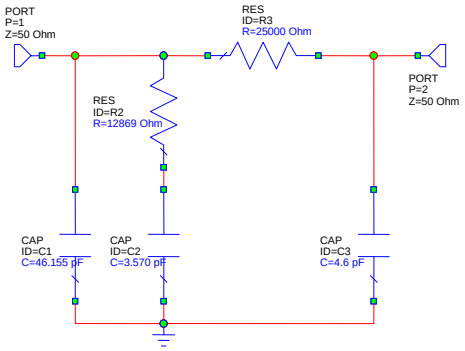

Figure 6: Third order passive Loop Filter

The loop filter is essential for stability and noise suppression. The loop Filter can be of passive or active type implementation. Passive filter is implemented by using R & C lumped components where as an active filter is implemented using active devices like operational amplifier (OP-AMP). Though active filter using OP-AMP is really necessary when voltage controlled oscillator (VCO) tuning voltage needs to be higher than the charge pump can supply and can provide a wide range of control voltage for the VCO. The OP-AMP adds cost, noise and size to a design and is therefore undesirable. Passive filter is easy to design and implement such as discrete or integrated implementation. Since in the current design there is no need for large variance of the control voltage & hence passive filter is used. The typical loop filter parameters are order, Insertion Loss, Loop Bandwidth and Phase Margin. In terms of filter order, the most basic is the second order filter, this filter is used where the first spur to be filtered is less than 10 times the loop bandwidth frequency and the lock time is minimum. Additional RC low pass filter stages can be added to reduce the reference spurs. Phase Margin and Loop Bandwidth are

crucial for loop filter design. Choosing the appropriate Phase Margin, Loop Bandwidth will better the PLL performance. Figure 7 shows the phase response and Figure 8 magnitude response simulation results respectively of loop filter. Comparison between first order, second order filter and third order filter was analyzed and third order filter was chosen for the design.

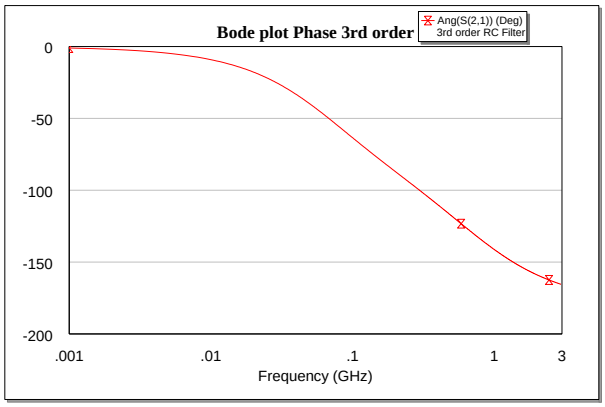

Figure 7: Third order Loop Filter phase response

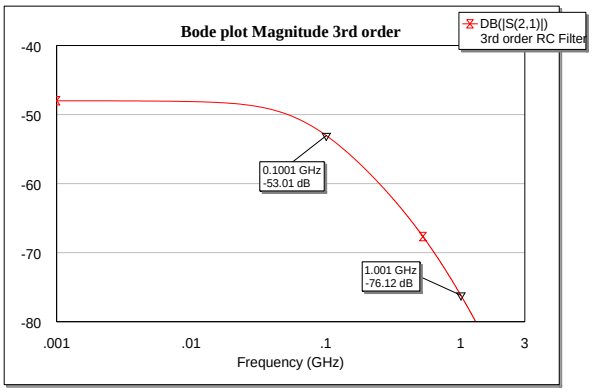

Figure 8: Third order Loop Filter Magnitude response

The Table 1 shows performance comparison of first, second and third order loop filter and observed that third order filter provides better attenuation for higher frequencies.

Table 1: First, Second and Third order Filter Comparison

Freq (GHz)	1st order RC Filter (dB)	2nd order RC Filter (dB)	3rd order RC Filter (dB)
0.1	-47.1525	-47.2064	-52.9997
0.5	-59.5138	-60.6933	-67.0843
1	-65.4727	-68.991	-76.11
1.5	-68.983	-74.7904	-82.2783
2	-71.4778	-79.2539	-86.9237
2.5	-73.4141	-82.8594	-90.6271
3	-74.9967	-85.8722	-93.6975
3.5	-76.335	-88.4542	-96.3159
4	-77.4945	-90.7105	-98.5966
4.5	-78.5172	-92.7127	-100.616
5	-79.4322	-94.5113	-102.427

Magnitude and phase bode plots comparison of first order, second order and third order filter is shown in Figure 9 and Figure 10.

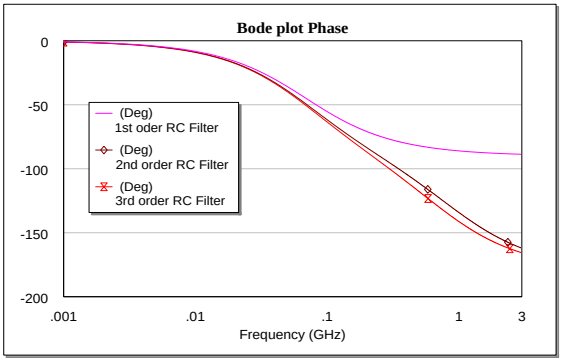

Figure 9: Comparison of Phase responses

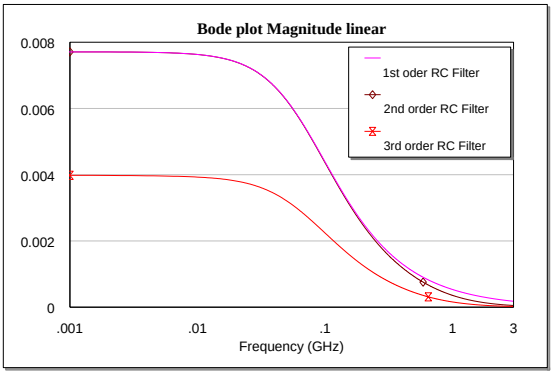

Figure 10: Comparison of Magnitude responses

4.3 Voltage Controlled Oscillator

The topology of the voltage controlled oscillator is very essential building block for its application. Oscillators are two types LC-oscillator and ring oscillator [6]. However, ring oscillators suffer from poor phase noise compared to LC oscillators and are less suitable for very high frequency applications.

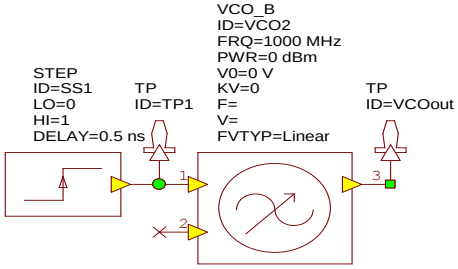

Figure 11: Voltage controlled Oscillator system diagram

LC oscillators are more attractive due to their better phase noise performance and lower power consumption. They occupy larger area compared to ring oscillators and frequency tuning is more complicated.

In order to provide 1GHz a behavioral model of VCO is used as shown in Figure 11. Different LC VCO topologies are NMOS, PMOS and complimentary VCO [7] shown in Figure 12. The idea is to use SiGe BiCMOS complementary LC which includes both PMOS and NMOS cross coupled structure. One of the most important design parameter of VCO is the phase noise performance. In order to achieve a low phase noise, this paper proposes to increase the tank inductance quality factor (Q) or filter the tail current noise. Increasing the Q of the tank inductance leads to a narrow tuning range. The inductors and varactors forming the LC tank circuit have to be symmetrical from both sides in order to ensure a true differential circuit. The advantages of complimentary topology are (i) the bias current of this structure results in better phase noise performance and also improves the switching of the cross-coupled pair.

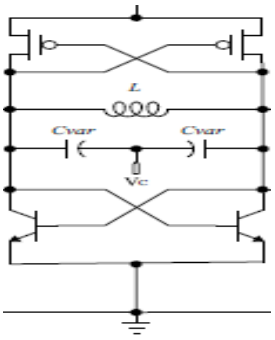

Figure 12: SiGe BiCMOS Complementary VCO

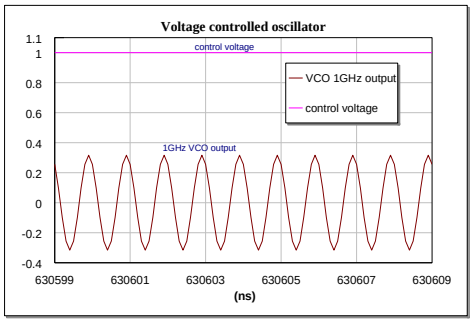

Figure 13: VCO output waveform

(ii) The cut-off frequency f_T of NMOS and PMOS transistors can be improved since the gate capacitors of both transistors are reduced to half. (iii) Due to symmetrical architecture the up conversion of 1/f noise improves. The output of VCO is shown in Figure 13.

4.4 Frequency Divider

The Frequency divider is one of the building blocks of a Phase Locked Loop (PLL) which converts the VCO high frequency output (F_{out}) to a lower frequency which can be compared to the reference input $F_{ref.}$ As the VCO is operated in the high frequency range, the PLL requires high frequency dividers [8]. The four key design issues related to the design of the frequency dividers are the high input frequency, division ratio, power consumption of the divider and input sensitivity (minimum amplitude of the input signal). In general, the power consumption of the divider is linearly proportional to the operating frequency. Its maximum operating frequency depends on the architecture, supply voltage and output load. Dividers are classified into two types mainly, analog and digital dividers. The analog dividers are based on the injection locking technique where as digital dividers are implemented using latches and flip-flops. For the present work, we are implementing digital frequency divider. Figure 14 and Figure 15 shows the circuit diagram of frequency divider. In the design VCO output is 1GHz and the Phase frequency detector requires reference input of 25MHz so the required frequency division ratio, N is 40.

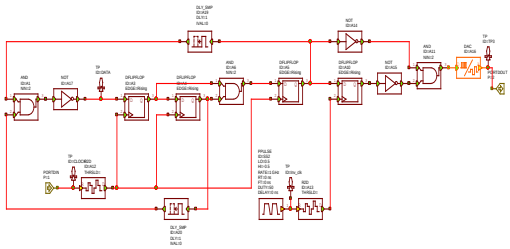

Figure 14: Frequency divider down to 200MHz

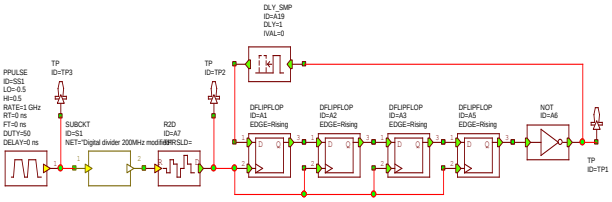

Figure 15: Frequency divider down to 25MHz

The Frequency divider is implemented using a divide- by-5 50% duty cycle divider followed by three D flip-flops (DFFs) that provide divide-by-8 logic. The divide-by-5 divider circuit consists of four DFFs, two and gates and

single nand gate. The divide-by-5 divider circuit not only divides the VCO 1GHz output to 200MHz, it make certain a duty cycle of 50% is achieved. The timing graph shown in Figure 16 explains how the 50% duty cycle is achieved. But their duty cycle is 60% or 40% the last flip flop is triggered by the falling edge of the clock which is half period after the flip flops triggered by the rising edge. This is how the 10% is eliminated and 50% duty cycle produced. The 200MHz is given to the three flip flops and the inverted output from the third flip-flop is fed back to the first flip flop to produce divide-by-8 and thus bring 200MHz down to required output of 25MHz frequency.

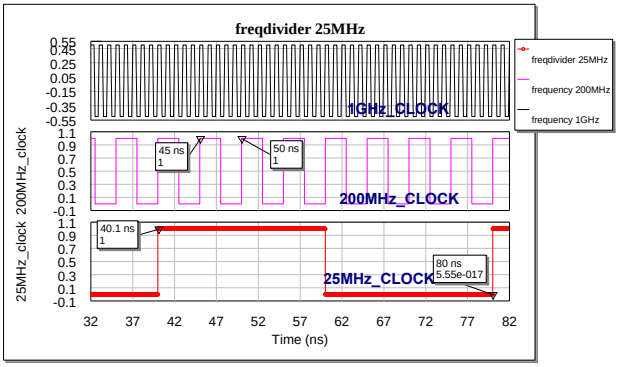

Figure 16:Frequency Divider waveform

5. PERFORMANCE ANALYSIS

The circuit of type II third order PLL is shown in Figure 17 and the output spectrum of VCO is shown in Figure 18. The power consumption is -4.835 dBm which corresponding to 0.32mW. Since the behavioral VCO model is used and phase noise is injected through a text data file "phmask" and the corresponding values are shown in table 3. The Figure 19 shows the phase noise simulation result at the VCO output. The measured value is -160dBc/Hz which is lower than the earlier carried out work.

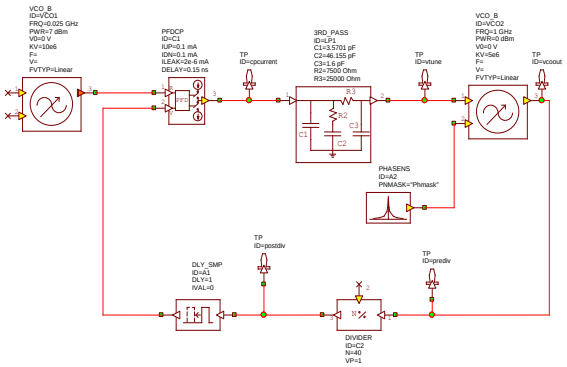

Figure 17: PLL Design

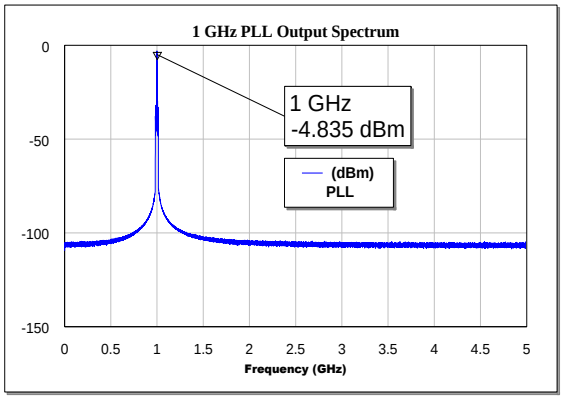

Figure 18: PLL output spectrum

Table 3: Phase noise data

(Hz)	(dBc)
10	-22.64
100	-45
1000	-75
10000	-105
1.00E+05	-125
1.00E+06	-145

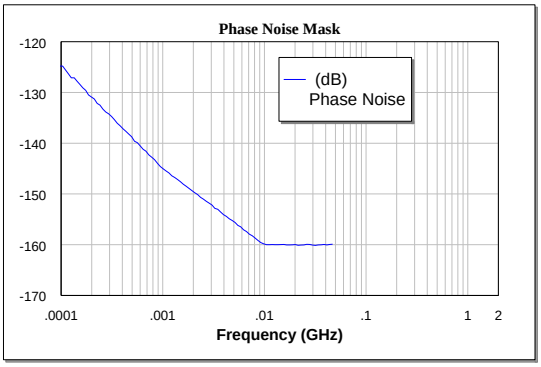

Figure 19: Phase noise spectral density

The performance analysis of current work and the earlier carried out work is shown in below table.

Table 2: Comparison of previous works with the proposed work

Reference	[11]	[2]	Proposed work
Process	CMOS	CMOS	SiGe
Channel spacing	20MHz	25MHz	25MHz
Freq range	2GHz	1GHz	1 GHz
Tuning Bandwidth	1MHz	1MHz	1MHz
Loop Filter	3rd order passive LPF	2nd order passive LPF	3rd order passive LPF
Phase Noise	-120dBc/Hz	-	-160dBc/Hz
Settling Time	~ 3µs	< 4µs	< 3µs
Current consumption	-	16.5mA	
Power consumption	1 mW	-	0.32 mW

6. CONCLUSION

In this Paper, complementary cross-coupled VCO design offer superior symmetry properties to the oscillating waveform decreasing the up-conversion of 1/f of the devices to the $1/f^3$ noise region. Charge pump mismatch and leakage currents increase the ripples on the control voltage and modulate it to appear as spurs at the PLL output degrading the PLL performance. Spurs are attenuated with the third order passive loop filter. VCO and frequency divider are main

sources of power consumption. Simple circuit structure and digital frequency divider helps in reducing the power consumption because of their lesser density logic. These along with SiGe BiCMOS process aid in generating a smooth signal spectrum at VCO output. Future work may include extensive design of resonant tank with a high Q to reduce phase noise significantly and enhancement of proposed frequency synthesizer to multiple frequencies.

7. ACKNOWLEDGEMENT

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