

Review on Deign of 16-Bit Quaternary Adder using Various Encoding Techniques

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ABSTRACT

I am designing a 16 bit quaternary adder. Outline of the parallel rationale circuits is restricted by the necessity of the interconnections. A conceivable arrangement could be touched base at by utilizing a bigger arrangement of signs over the same chip region. Quaternary outlines are picking up significance from that point of view. It shows numerous esteemed full viper circuits, actualized in quaternary rationale. This is planned by utilizing one hot encoding and barrel shifter to accomplished Optimization in zone, speed and power will be accomplished by CMOS quaternary rationale. Sum and convey are handled in two separate squares, controlled by code generator unit. The circuit level execution of the different esteemed rationale administrators: legitimate aggregate, consistent item, level-up, level-down and level transformations are exhibited. Plan check will be done by Tanner Tools.

Keywords

CMOS, Adder,

1. INTRODUCTION

Current computerized gadgets innovations are basically based upon paired frameworks. Multi-esteemed frameworks are generally proposed to give focal points by diminishing the quantity of information interconnect lines and preparing components. Such rationale circuits can speak to numbers with less bits than paired, e.g. the decimal number 255 is spoken to as 11111111 in paired and 3333 in quaternary [1]. As the circuits turn out to be less confused, the information handling might be quick and solid.[4]The thought of the various esteemed rationale, or fluffy rationale opened a limitless exploration range. To reduce the area, interconnection, power, transistor by using quaternary logic. There are four quaternary states 0, 1, 2 and 3 for which we can take parallel comparable as 00, 01, 10 and 11 [5]. They are called as total low, medium low, medium high and supreme high. In the event that the bits of paired representation trade their position and quaternary state stay unaffected then it is called as twofold symmetry if not called as halter kilter.[3]

1.1 Full Adder Using One Hot Encoding

The propose quaternary full adder is shown in fig 1 in which barrel shifter use for sum calculation. It is a novel circuit with one hot encoder. Barrel Shifter is controlled by two inputs A and B. one hot encoding means at one time only 1 bit is 1 and reset is zero.

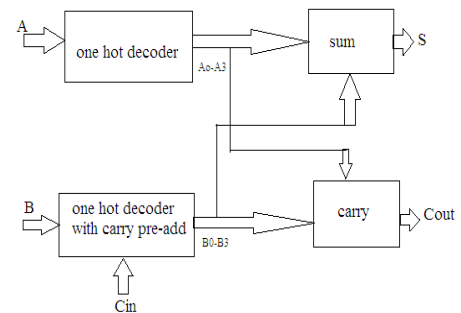


Fig 1: Block Diagram of Quaternary Full Adder

Table1. Truth table of quaternary full adder
SUM
CARRY

		B						B			
		0	1	2	3			0	1	2	3
A	0	0	1	2	3	A	0	0	0	0	0
	1	1	2	3	0		1	0	0	0	1
	2	2	3	0	1		2	0	0	1	1
	3	3	0	1	2		3	0	1	1	1

1.2 Operation Definition And Algebraic Property

Let the rationale estimations of a four-esteemed (quaternary) framework be in the set $Q = \{0, 1, 2, 3\}$. A quaternary variable is meant by a lower-case letter. Let a, b, c, d, x, y and z be quaternary variables.[4]

1.3 MAX & MIN Operation

The circuits executing the intelligent total (max) and sensible item (min) administrators are appeared in Fig. Every circuit incorporates three transistors: two exhaustion mode and one improvement mode. To fathom the operation of these circuits, the operation of the maximum administrator circuit is currently clarified in point of interest. The operation of the min circuit could then be effectively caught on. Give us a chance to accept that we supply the maximum circuit with two quaternary inputs: x and y .[4]

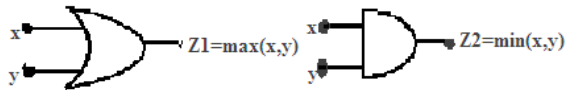


Table2. Truth table for MAX & MIN Operation

MAX					MIN				
X\Y	0	1	2	3	X\Y	0	1	2	3
0	0	1	2	3	0	0	0	0	0
1	1	1	2	3	1	0	1	1	1
2	2	2	2	3	2	0	1	2	2
3	3	3	3	3	3	0	1	2	3

1.4 SUM & DIFFERENCE

Operator

The truncated total by one and truncated distinction by one administrator circuits are appeared in Fig. Every circuit comprises of three stages: to be specific, two for voltage-shift and one for voltage-revision. The $x \oplus 1$ and $x \ominus 1$ operations are comparable to and, in this way, just the operation of truncated entirety by one administrator circuit is portrayed here.[4]

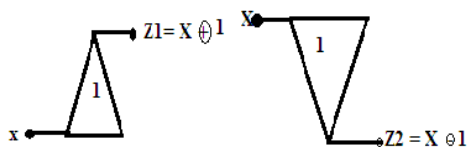


Table 3. Truth table for Increment & decrement operator

INCREMENT		DECREMENT	
X	Z	X	Z
0	1	0	1
1	2	1	0
2	3	2	1
3	3	3	2

2. RELATED WORK

The twofold rationale circuits are configuration confined by the interconnection prerequisites. On this issue arrangement is that by utilizing extensive arrangement of signs over the same chip territory. In this paper plan quaternary snake utilizing different encoding methods. The different encoding methods are One Hot Encoding and the barrel shifter plan. By

utilizing quaternary snake he can diminish the transistor furthermore decreased the force dissipation. [1]

In earlier year advancement strategies utilized for diminishing the time and chip zone of viper circuits in double rationale framework. In this paper, he give the important mathematical statements required to outline a full snake in quaternary rationale framework. Finally, he thinks about the entryway postponements of full snake and logarithmic stage parallel viper with the assistance of scientific expressions. By utilizing scientific mathematical statement he can diminished the region on same chip.[2]

In double circuit need of interconnection outline is restricted. It expands territory, deferral and vitality utilization of advanced circuit. In this paper he plans different combinational modules utilizing Quaternary rationale. Different quaternary snake utilizing one of a kind encoding, quaternary encoder. It decreases the transistor and force dispersal. Reenactment has been done in tanner. [3]

To design quaternary voltage mode CMOS circuit level execution of the numerous esteemed rationale administrators: logical sum, logical product, increment, decrement and level conversions are presented.[4]

3. PROPOSED WORK

In earlier research after studied these papers it is observed that the work on quaternary. In some papers quaternary adder is design to reduce the power dissipation. I am designing a 16-bit quaternary adder using various encoding techniques to reduce the transistor, area and power dissipation using tanner tool.

4. CONCLUSION

From latest research after studied various papers it is observed that work done on quaternary adder is very less. In most paper they design single bit quaternary adder. In this paper I am designing a 16-bit quaternary adder using various encoding techniques.

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