Analysis of Various Full-Adder Circuits in Cadence

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ABSTRACT
The Adder is the important part in any processor/controller design. Till date there are a plenty of 1-bit full-adder circuits which have been proposed and designed. In this paper we have a analytic and comparative description of various full adder circuits, considering various constraints like power consumption, speed of operation and area. The circuits are designed in the virtuoso platform, using cadence tool with the available GPDK – 45nm kit. The Full-adder circuits with the most 28 transistor to the one with only 6 transistors are successfully designed, simulated and compared for various parameters like power consumption, speed of operation(delay) and area (transistor count), and finally concluded the best designs, that suite for the particular specifications.

Keywords
Cadence, Virtuoso, GPDK, Delay, Power Consumption, Area (Transistor Count)

1. INTRODUCTION
Summation (Addition) is the basic arithmetic operations and is used in VLSI systems as a full adder circuit extensively. It adds the binary numbers and is the main part for other operations such as subtraction (complement addition), multiplication (successive addition), division (successive subtraction), etc. The overall performance of the system is mainly dependent on the adder performance. Hence the performance enhancement of a 1-bit full-adder cell is to be done at the initial stages only. The full adder circuit performance is dependent on the approach for designing the circuit. The speed of operation of a circuit is indirectly found with the help of delay time calculation which directly depends on the transistor count, the logic depth and other criteria. The power consumption depends on the switching activity and the number and the transistor size. The transistor size and routing complexity helps to know the area of a die.By varying the size of the transistors, the speed of the design can be varied. Till Today, many 1-bit Full Adder Circuits are Designed, in which the transistor counts varies from 28 to a minimum of 6 transistors. The proposed Full adder Circuits have their own advantages and disadvantages. Hence the main objective of this paper is to collect all the existing circuits in a single paper, design them and simulate the same and find out the various parameters like Power Consumption, Delay,

Transistor Count(Area), etc., and finally tabulate the same to conclude the best design that suites the designer's Specifications.This paper is organized as follows. Section 2 explains about the Existing Full Adder circuits collected from various reference papers. Section 3 gives the snapshots of Designed designs of these full adders in cadence and the results are presented in Section 4. A conclusion and future work is given in Section 5.

2. EXISTING FULL ADDERS
The Full Adder circuit is an important component in applications such as in various processor, and controller and data processing units. In recent years, several variants of different logic styles have been proposed to implement Full Adder cells. Many papers have been published regarding the optimization of low-power full adders, trying different options for the logic style. So in this paper the brief discussion of the various full adder circuits, starting with the most conventional 28 transistor full adder and then gradually studied full adders consisting of as less as 6 transistors has been discussed.Now the various Existing Full adder design circuits are been explained with detailed details of the paper from which it has been collected, and its other information.In the paper [7], the conventional CMOS adder cell using 28 transistors based on standard CMOS topology which is as shown in figure 4a had been discussed. And there it was described that, due to high number of transistors, its power consumption was high, and also the large PMOS transistor in pull up network resulted in high input capacitances, which caused high delay and dynamic power. And this adder was based on regular CMOS structure (pull-up and pull-down network). So the full adder with 28 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 3.

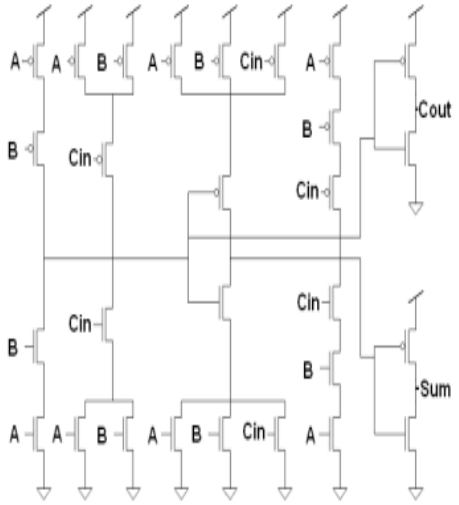

Fig 3: 28T Conventional Full Adder

In the paper [9], they have proposed two new full adder designs by combining common digital gates and majority functions. They have compared the performance of the better one with six other full adders. So the full adder with 26 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 4.

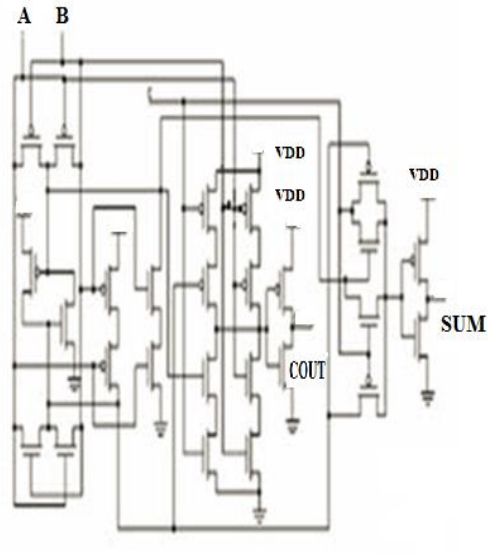

Fig 4: 26T Full Adder

In the paper [8], a new Full Adder cell based on Majority function and DCVS (Differential Cascade Voltage Switch) technology was presented. They produce sum and carry at the same time with two separate circuits. And their newly proposed new Full Adder has been compared with following Full Adders like 24T Full Adder cell, Conventional CMOS Full Adder cell, CPL Full Adder cell and TGA Full Adder cell. So the full adder with 24 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 5.

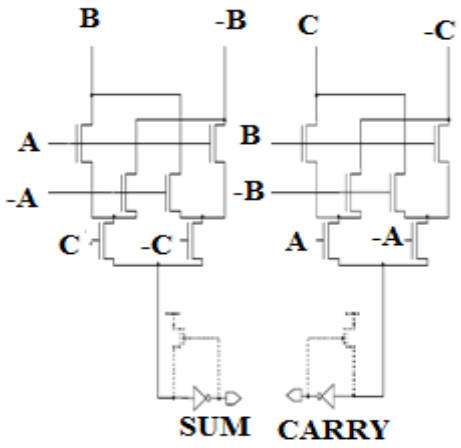

Fig 5: 24T Full Adder

In the paper [10], two new 1-bit full adder cells operating in sub threshold region with 65nm, 90nm and 0.18um technologies. Inverse Majority Gate (IMG) together with NAND/NOR were used as the main computational building blocks. A modification was done to optimize W/L ratios with different supply voltages. They used W/L ratios for all the PMOS transistors 1.5 times the ratio of W/L for all NMOS transistors. And the Results were compared with a previously reported minority-3 based full adder; the results involve better performance in terms of power, delay and PDP. So the full adder with 22 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 6.

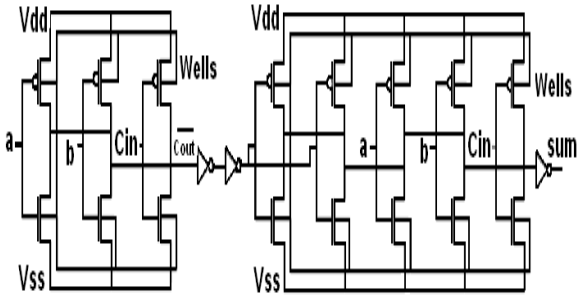

Fig 6: 22T Full Adder

In the paper [11], Transmission gate approach which is another widely used CMOS design style to implement digital function has been discussed. Transmission gate based implementation is similar to pass transistor with the difference that transmission gate logic uses NMOS and PMOS transistors where as pass transistor logic uses only one type of transistor i.e. either NMOS or PMOS. Full adder implementation based on TG logic is shown in the Figure above. So the full adder with 20 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 7.

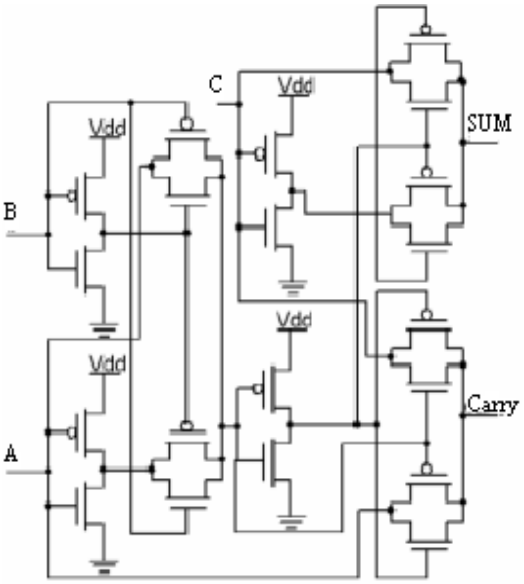

Fig 7: A 20T TG Based Full Adder

In the paper [3], NMNFA is a Nand-Majority-Nor based Full Adder cell and is comprised of three capacitors and 18 transistors. This circuit is designed based on the similarity of Cout and Sum signals. In this design, Nand and Nor functions are implemented by setting desired threshold for the inverters by choosing proper aspect ratio for their transistors. So the full adder with 18 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 8.

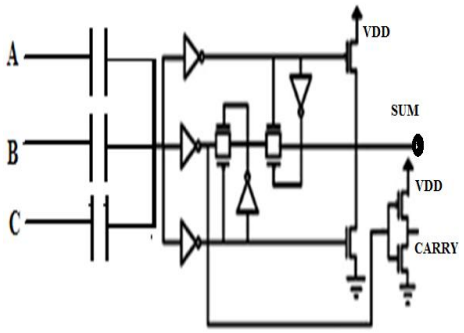

Fig 8: 18T NMNFA, a Nand-Majority-Nor based Full Adder

In the paper [3], the proposed Full Adder cell (MBFA) was designed using a 3-input Minority circuit, followed by a Bridge style structure. The MBFA adder module has advantages of the Bridge style Including low-power consumption and the simplicity of the design. Although the presented structure is designed based on capacitor network and Minority function, this design is totally different from the previous circuits and outperforms them considerably. For instance, in comparison with BCFA, the proposed design has some great advantages which improve the metrics of the design significantly. The Cout node is the Achilles‟ heel of BCFA because the Bridge circuit which has not high driving power should drive a 2C capacitor and an inverter. This increases the delay of the circuit specifically at low voltages and nanoscale. So the full adder with 16 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 9.

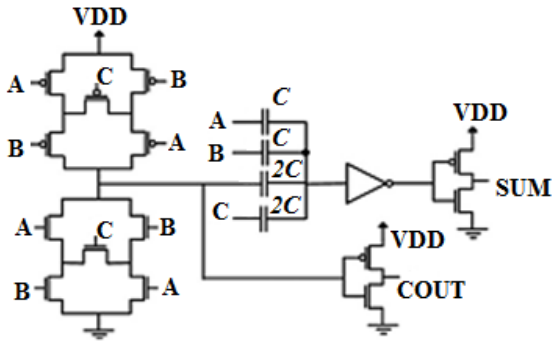

Fig 9: 16T Low-Power CMOS Bridge Style & Capacitors Full Adder

In the paper [2], the various existing full adder circuits are been compared, and in that it includes many circuits like CMOS Transmission Gate (TG), PassTransistor Logic (PTL), Complementary Pass-transistor Logic (CPL), Gate Diffusion Input (GDI), LPFA (Low Power Full Adder), GDI based full adder, etc. So the full adder with 14 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 10.

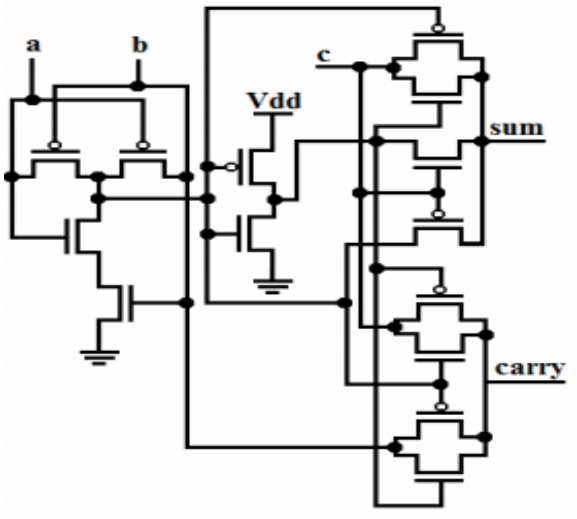

Fig 10: 14T Full Adder

In the paper [13], two new designs for single bit full adders have been presented using three transistors XOR gates. Simulations of the same were carried out at different supply voltage with increasing reverse biased applied to NMOS transistor and results showed improvements in power consumption of adder. So the full adder with 12 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 11.

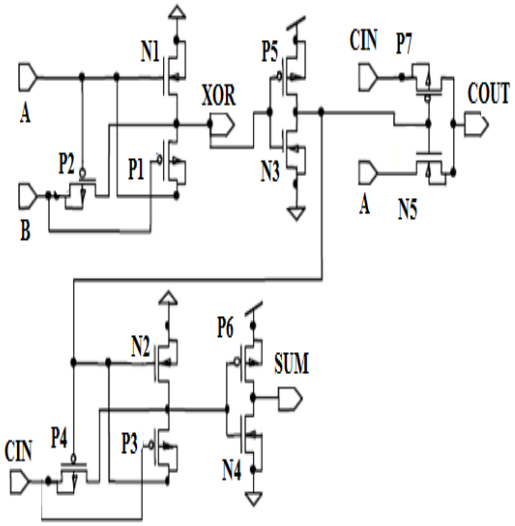

Fig 11: 12T Full Adder

In the paper [4], an overview of performance analysis and comparison between various parameters of a low power high speed 10T full adder had been presented. This paper showed comparative study of advancement over active power, leakage current and delay with power supply. So the full adder with 10 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 12.

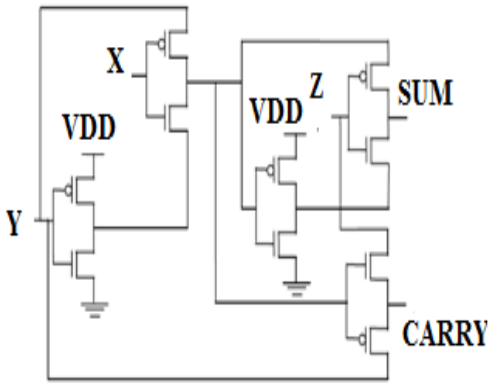

Fig 12: 10T Full Adder

In the paper [5], pre-layout and post-layout simulations of a new 9T full adder cell at low voltages. The main objective of design was low power consumption and full voltage swing which was achieved at low supply voltage. The proposed design showed its superiority against existing adder in terms of power consumption, power-delay product (PDP), temperature sustainability and noise immunity. So the full adder with 9 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 13.

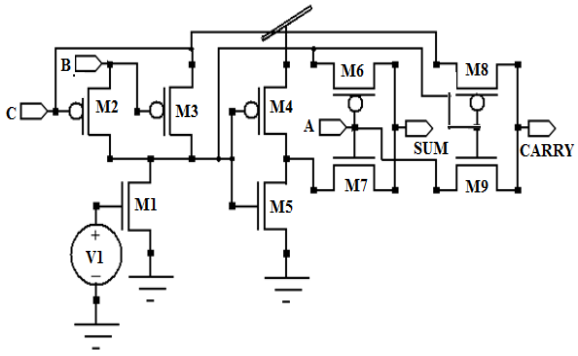

Fig 13: 9T Full Adder

In the paper [12], low power and high performance 1-bit full adder cell is proposed. The 8T Full Adder technique has been used for the generation of XOR function. So the full adder with 8 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 14.

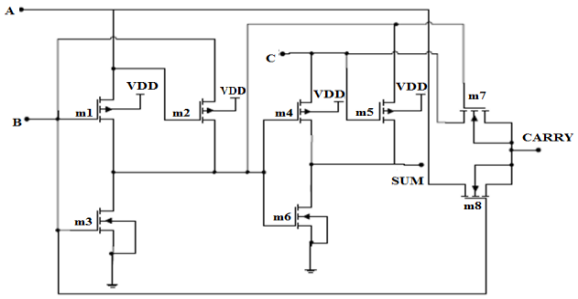

Fig 14: 8T Full Adder

In the paper [6], the design of an adder circuit based on majority function is proposed. The adder comprises of only six MOS transistors. To make the design to be used invariably in the system with least nano device dimensions, some modifications have been done in the existing adder design. So the full adder with 6 transistors was presented in that paper and we have chosen and have taken the same and has been compared it with other circuits and it is as shown in Figure 15.

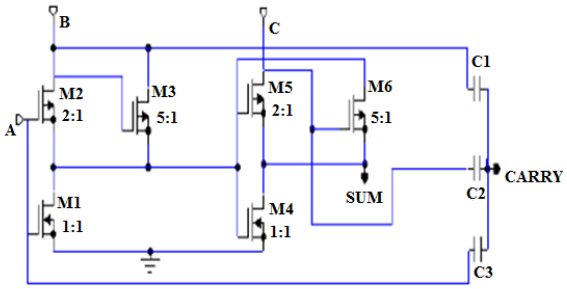

Fig 15: 6T Full Adder

3. DESIGNED DESIGNS IN CADENCE

In this Section, we show the snap shots of the designed Existing Full Adder circuits, which has a schematic, symbol and a test circuit and output waveforms, from which the Power Consumption, Area, and Delay are calculated. For the time being we have shown only 26T Full Adder Design's Schematic, symbol and Test Circuit, and output Waveforms in Figures 16, 17, 18 and 19 respectively.

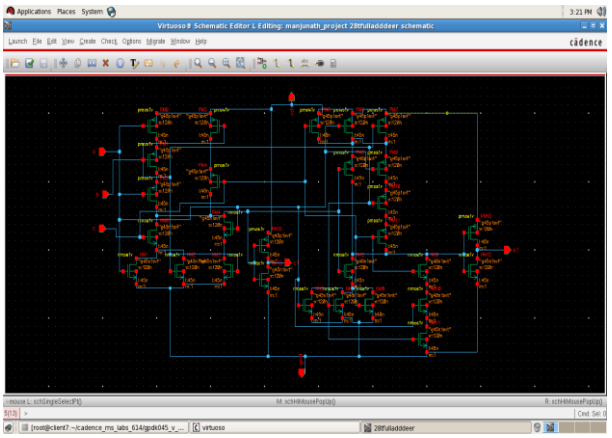

Fig 16: Schematic of a 28T Full Adder in Cadence.

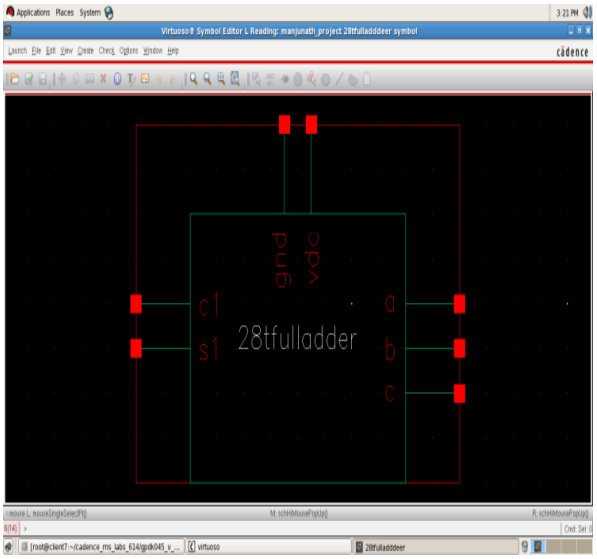

Fig 17: Symbol of a 28T Full Adder in Cadence.

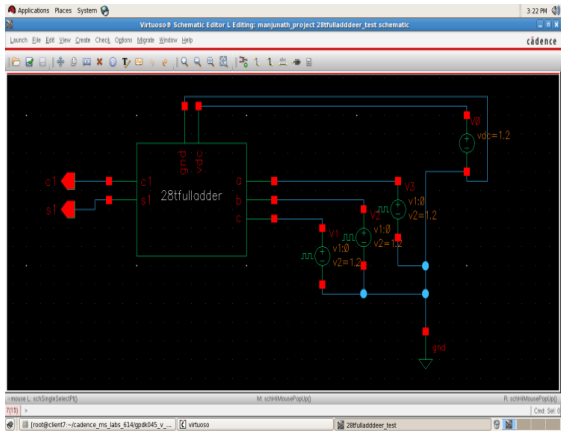

Fig 18: Test Circuit of a 28T Full Adder in Cadence.

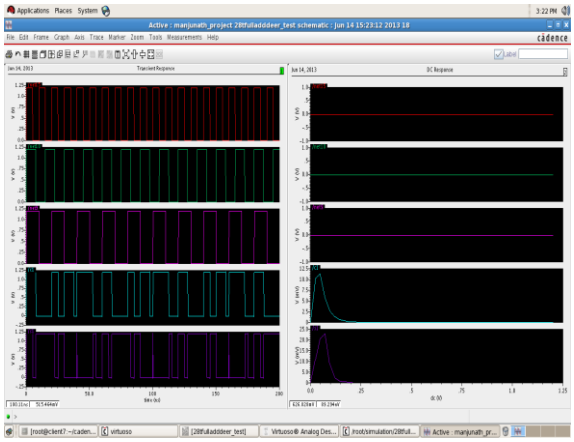

Fig 19: Waveforms of a 28T Full Adder in Cadence

4. RESULTS

The circuits are designed in a Cadence Virtuoso Environment using 45nm Technology GPDK Tool Kit, with a voltage supply of 1.2V, and Threshold Voltage of 0.9v and compared with each other and Tabulated as shown in this chapter. The Comparison is done in terms of Number of Transistors, Delay (Sum and Carry), as well as Power Consumption as shown in the following tabular columns.

4.1 Designed Full adders in terms of Number of Transistors

The table 2, and also Figure 20 shows the comparison of Full Adder types and its Transistor Count, which will indirectly, gives us information about the Area. More the number of Transistors, Higher is the area, and vice versa.

Table 2: Full Adder Type vs Number of Transistors

FULL ADDER TYPE	NUMBER OF TRANSISTORS
28T CMOS Full Adder	28
26T Full Adder	26
24T Full Adder	24
22T Full Adder	22
20T TG Full Adder	20
18T NMN Full Adder	18
16T Full Adder	16
14T Full Adder	14
12T Full Adder	12
10T Full Adder	10
9T Full Adder	9
8T Full Adder	8
6T Full Adder	6

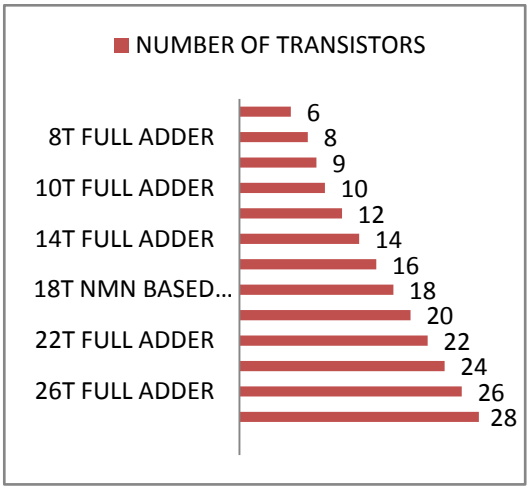

Fig 20: Graphical representation of the Table 2

So from the table 3 and also from figure 20, we can conclude that the '28T CMOS Conventional Full Adder' has highest area, since it requires 28 Transistors for its design and '6T Full Adder' has lesser area as it requires only 6 Transistors for its design.

4.2 Designed Full adders in terms of Sum and Carry Delays

The Tables 3 and 4 shows the comparison of Full Adder types and its Delays in terms of sum and carry of each of the inputs to the sum and carry output respectively. More the Delay, lesser is its speed of operation, and vice versa.

Table 3: Full Adder Type vs Sum Delays from A, B, C inputs

FULL ADDER TYPE	SUM DELAY		
	A to SUM	B to SUM	C to SUM
28T CMOS Full Adder	1.53E-11	2.23E-11	5.98E-11
26T Full Adder	7.17E-11	3.42E-11	3.33E-12

24T Full Adder	7.53E-09	7.61E-09	7.64E-09
22T Full Adder	2.13E-11	1.62E-11	5.37E-11
20T TG Full Adder	1.07E-10	6.97E-11	3.22E-11
18T NMN Full Adder	9.85E-09	9.89E-09	9.93E-09
16T Full Adder	6.48E-11	2.73E-11	1.02E-11
14T Full Adder	6.23E-11	2.48E-11	1.27E-11
12T Full Adder	2.00E-08	2.00E-08	2.00E-08
10T Full Adder	6.41E-11	2.66E-11	1.09E-11
9T Full Adder	4.85E-09	4.89E-09	4.93E-09
8T Full Adder	5.11E-11	1.36E-11	2.39E-11
6T Full Adder	3.00E-12	4.05E-11	7.80E-11

Table 4: Full Adder Type vs Carry Delays from A, B, C inputs

FULL ADDER TYPE	CARRY DELAY		
	A to CARRY	B to CARRY	C to CARRY
28T CMOS Full Adder	4.12E-11	3.64E-12	3.39E-11
26T Full Adder	7.36E-11	3.61E-11	7.36E-11
24T Full Adder	9.46E-12	9.68E-12	9.86E-12
22T Full Adder	3.02E-11	7.30E-12	4.48E-11
20T TG Full Adder	1.10E-11	4.85E-11	8.60E-11
18T NMN Full Adder	1.27E-11	2.48E-11	6.23E-11
16T Full Adder	3.59E-12	4.11E-11	7.86E-11
14T Full Adder	1.08E-11	4.83E-11	8.58E-11
12T Full Adder	8.72E-10	9.09E-10	9.47E-10
10T Full Adder	6.12E-11	2.37E-11	1.38E-11
9T Full Adder	4.38E-11	8.13E-11	1.19E-10
8T Full Adder	4.09E-12	4.16E-11	7.91E-11
6T Full Adder	4.29E-11	5.35E-12	3.21E-11

Finally the Table 5 shows the average sum delay, and the average carry delay with respect to each full adder type. The graphical view of the same is shown in figures 21 and 22 respectively.

Table 5: Full Adder Type vs Average Sum and Carry Delays

FULL ADDER TYPE	FINAL AVERAGE DELAYS	
	SUM	CARRY
28T CMOS Full Adder	9.73E-11	7.08E-11
26T Full Adder	1.09E-10	1.83E-10
24T Full Adder	2.28E-08	2.90E-11
22T Full Adder	9.12E-11	8.23E-11
20T TG Full Adder	2.09E-10	1.45E-10
18T NMN Full Adder	2.97E-08	9.98E-11
16T Full Adder	1.02E-10	1.23E-10
14T Full Adder	9.98E-11	1.45E-10
12T Full Adder	6.00E-08	2.73E-09
10T Full Adder	1.02E-10	9.87E-11
9T Full Adder	1.47E-08	2.44E-10
8T Full Adder	8.86E-11	1.25E-10
6T Full Adder	1.22E-10	8.04E-11

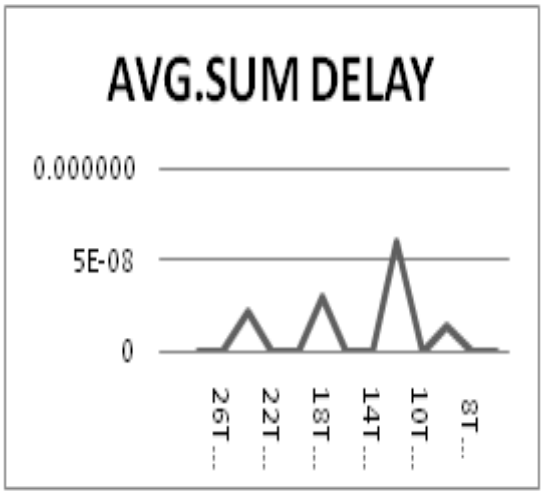

Fig 21: Graphical representation of Average Sum Delay

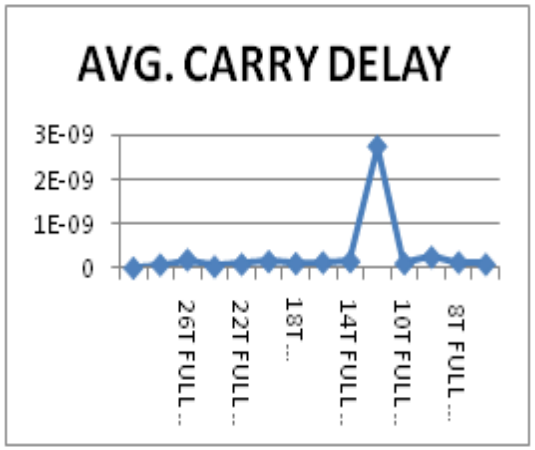

Fig 21: Graphical representation of Average Carry Delay

So, from the Table 5 and figures 20 and 21, we can conclude that the '8T Full Adder' has the Least Sum Delay of 8.86E-11, and '24T Full Adder' has Least Carry Delay of 2.28E-08. And if we consider the Total Delay, then the '22T Full Adder' with a total of 17.35E-11 (because 9.12E-11 + 8.23E-11), is the best one to give Least Total Delay.Also, we can conclude that the '12T Full Adder' has the Highest Sum Delay of 6.00E-8, and the Highest Carry Delay of 2.90E-9 and also the Highest Total Delay of 6.29E-8 (because 6.00E-8 + 2.90E-9).

4.3 Designed Full adders in terms of Power Consumption.

The full Adders are been compared in terms of power consumption, and the results are tabulated and is as shown in table 6.

Table 6: Full Adder Type vs Current, Voltage and Power

FULL ADDER TYPE	(POWER) in WATTS
28T CMOS Full Adder	1.61E-10
26T Full Adder	7.07E-05
24T Full Adder	4.81E-05
22T Full Adder	1.59E-06
20T TG Full Adder	4.64E-05
18T NMN Full Adder	6.80E-05
16T Full Adder	2.08E-05
14T Full Adder	5.93E-11
12T Full Adder	3.48E-05
10T Full Adder	6.10E-11
9T Full Adder	3.05E-06
8T Full Adder	4.40E-10

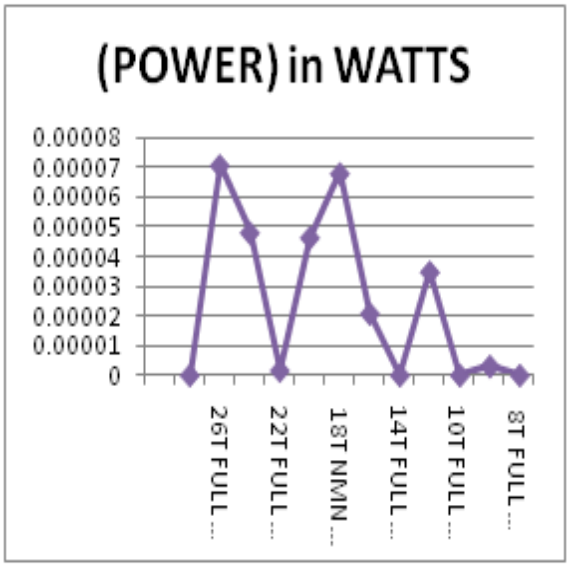

Fig 22: Graphical Representation of Power

So from the table 6 and figure 22, we can conclude that the '26T Full Adder' type consumes More Power of about 7.07E-5 Watts, and the '14T Full Adder' type consumes very Less Power of about 5.93E-14 Watts.

5. CONCLUSION AND FUTURE WORK

All the proposed Existing Full Adder circuits are been designed in a Cadence Virtuoso Environment using 45nm Technology GPDK Tool Kit, with a voltage supply of 1.2V, and Threshold Voltage of 0.9v and comparison results are tabulated, and finally the best designs for the particular parameters are been concluded. If we consider 'Area (Transistor Count)' as the main factor, then the designers can prefer '6T Full Adder Design', which has lesser Area. Similarly, if we consider 'Delay' as the main factor, then the designers can prefer '22T Full Adder Design', which has lesser Total Delay. And similarly, if we consider 'Power Consumption' as the main factor, then the designers can prefer '14T Full Adder Design', which has lesser Power Consumption.The many Future works that can be done are as follows. We can improve the performance of each of these designed 1-bit full adder blocks by varying their W/L ratios or by adding some of the passive elements like Resistors, Capacitors, etc. Using the designed 1-bit full adder blocks, we can design the 2-bit, 4-bit, 8-bit, 16-bit, 32-bit, 64-bit Adder/Subtractor circuits and so on. We can even design and compare these designs in all possible Nanometer technologies like 180nm, 90nm, 65nm, 32nm, 22nm, and so on. We can replace the full adder blocks of any previous application projects, with our designed full adder circuit blocks, that can do the same function as that is done by the old full adder circuits, to improve the performance factors like Area, Delay, or Power consumption, etc. The heading of a section should be in Times New Roman 12-point bold in all-capitals flush left with an additional 6-points of white space above the section head. Sections and subsequent sub- sections should be numbered and flush left. For a section head and a subsection head together (such as Section 3 and subsection 3.1), use no additional space above the subsection head.

6. REFERENCES

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