Design and Power Analysis of Memory System using Conventional 6T, Sleepy Stack 8T and Single Ended 6T SRAM Cell

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ABSTRACT
Low power design has become the major challenge of present chip designs as leakage power has been rising with scaling of technologies. As the demand for low power and low cost increases, it is very important to design low power, high performance, and fast responding SRAM (Static Random Access Memory) since they are critical component in high performance processors. The Conventional 6T SRAM cell is very much prone to noise during read operation[2]. To overcome the problems in 6T SRAM cell, researchers have proposed different SRAM topologies such as 8T, 9T, 10T etc. bit cell design. These designs can improve the cell stability but suffer from bit line leakage noise. Dynamic power was previously the single largest concern for low-power chip designers, but as the feature size shrinks, the leakage power reduction has become the great challenge for current and future technologies. In this paper, different SRAM cells are used for the power analysis and also single ended 6T SRAM is introduced which reduces the power and area considerably.

Keywords
SRAM cell, Pre-charge circuit, Sense amplifier, Single ended SRAM cell .

1. INTRODUCTION
Power dissipation is one of the major concerns of Very Large Scale Integration (VLSI) circuit designs, for which CMOS is the primary technology. Low power design has become the major challenge of present chip designs as leakage power has been rising with scaling of technologies. With increasing chip densities, leakage power has become dominant in memory design. This work compares the reduction of power dissipation in different SRAM system. An 8T SRAM cell that uses two NMOS sleep transistors, one each in the pull down path of the two inverters of 6T SRAM cell is chosen as the ultra low power SRAM cell to build this array. This SRAM cell uses self correcting feedback to achieve stable operation. This cell also reduces dynamic power consumed during active mode of operation compared to conventional 6T SRAM cell.
The functional blocks for the 1-bit memory array are SRAM cell, data write circuitry, bit line conditioning circuitry and sense amplifier. This work addresses design, simulation, and functionality verification of 1-bit memory cell using different SRAM cell.

2. IMPLEMENTATION
In this section design of 1 bit memory cell is shown using 6T,8T and single ended 6T SRAM.

2.1 Conventional 6T SRAM Cell
The 6T SRAM cell is composed of six transistors, one NMOS transistor and one PMOS transistor for each inverter, plus two NMOS transistors for access. This configuration is called a 6T Cell. This cell offers better electrical performances than a resistive load 4T structure. Each bit in an SRAM is stored on four transistors that form two cross coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional access transistors serve to control the access to a storage cell during read and write operations.
Access to the cell is enabled by the word line (WL in figure 1) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL bar. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, but both the signal and its inverse are typically provided in order to improve noise margins.
The disadvantages of 6T SRAM cell is ,as the transistor size shrinks, the leakage power increases which in turn increases the power dissipation of the memory cell . To overcome this problem different SRAM topologies are introduced.

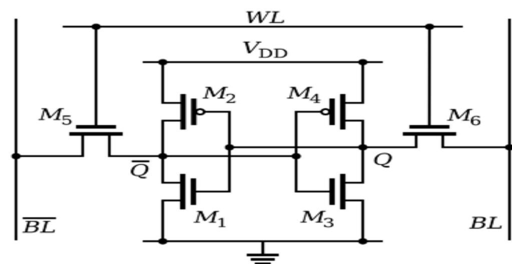


Figure 1: Conventional 6T SRAM cell

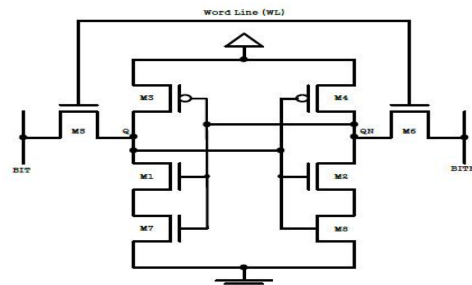


Figure 2: 8T SRAM cell

2.2 Low Power 8T SRAM Cell

The 8T SRAM cell (figure 2) consists of two cross-coupled inverters made up of transistors M1, M3 and M2, M4. The transistors M5, M6 are access transistors. The two additional NMOS transistors M7 and M8, one each in pull down path of cross coupled inverters are used to achieve leakage power reduction. The access transistors are connected to the word line at their respective gate terminals, and the bit-lines at their drain terminals. The word line is used to select the cell while the bit lines are used to perform write and read operations on the cell. Internally, the cell holds the stored value on one node and its complement on the other node. The node Q holds the stored value while other node QN holds its complement. The two complementary bit lines are used to improve speed of write and read operations. The 8T SRAM cell is shown in Figure 2. The SRAM cell is symmetric and hence M1=M2, M3=M4, M5=M6, and M7=M8.

2.3 SRAM Memory System for Writing and Reading Single Bit Data:

The whole memory system is shown in figure 3.To access the SRAM cell, extra circuitry is needed. They are,

- Pre-charge Circuit
- Data Write Circuit
- Sense Amplifier

The Pre-charge Circuit is used to pre-charge the bit-lines, BIT and BITN, to logic “1” value during inactive state of memory cell. When memory cell is being written/ read, pre-charging is deactivated.

The Data Write Circuit is used to write data and its complement onto the bit-lines. Writing a value into the SRAM cell is done by forcing one of the bit lines (BIT/BITN) high while keeping the other low. To write a “1” into the SRAM cell, the word line (WL) is Asserted, bit line BIT is made high and bit line BITN is made low. To write a “0” into the SRAM, bit line BIT is made low and BITN is made high. Before reading from the SRAM cell both bit lines (BIT, BITN) are pre-charged high and SRAM cell is selected. When WL selects the SRAM cell to be read, depending on the data in the

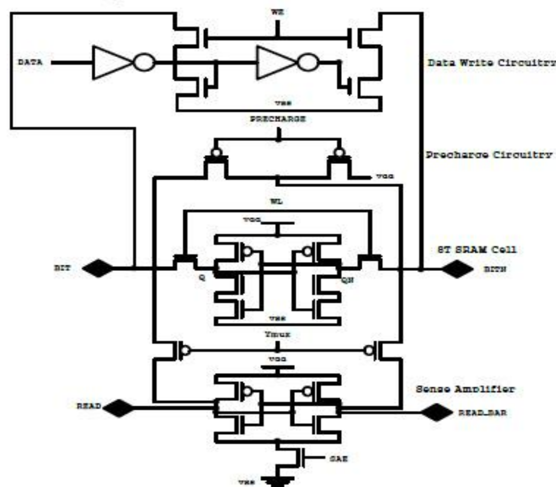


Figure 3: SRAM Memory System for Writing and Reading Single Bit Data

SRAM cell, one of the bit lines is pulled down. If BIT is pulled down the stored data is “0”. If BITN is pulled down the stored data is “1”.

The Sense amplifiers are used to sense which line is being pulled down and perform the read operation of the stored data. READ and READ_BAR indicate the data stored and its complement during the read operation. SRAM cell, word line (WL) that decides to/from which address data will be written or read from and the signal data is the one bit data either 1 or 0 that is to be stored into or read from the SRAM cell. The two output signals are READ corresponding to the data signal and READ_BAR is the inverse of data.

The major disadvantage of the memory system including write circuit, pre-charge and sense amplifier circuit is that it consumes large area and also power consumption is high. Hence a single ended 6T SRAM is introduced which reduces the area and power considerably and uses less number of transistors compared to the previous memory cells.

2.4 Single Ended 6t SRAM Cell

In this paper the existing 8T SRAM Cell is being compared with the single ended 8T SRAM design (figure 4). In this design, a transmission gate is used for Read purpose. The additional signal RWLB is an inversion signal of read wordline (RWL). It controls the additional transistor M7 of the transmission gate. While the RWL and RWLB are asserted and once the transmission gate is ON, a stored node is connected to RBL. Thus a stored value at Q is being transferred to or read through RBL.

One of the major advantages of this design is that it is not necessary to prepare a pre-charge circuit as required in prior 8T SRAM cell and a sense amplifier circuit as required in 6T

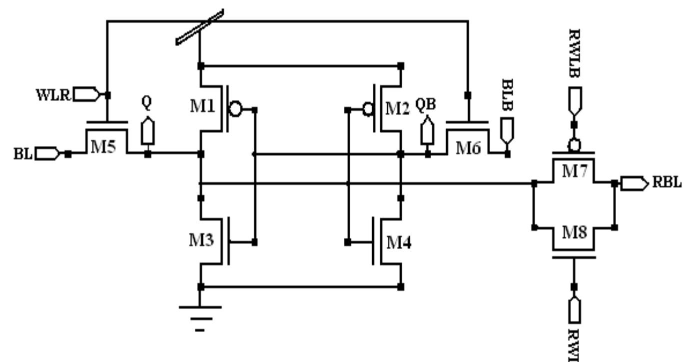


Figure 4: Single Ended 8T SRAM Cell

SRAM cell because the stored value is directly passed through transmission gate. A charge/discharge power on the RBL is consumed only when the RBL is changed. Consequently, no power is dissipated on the RBL if an upcoming data is the same as the previous state. The design reduces a bitline power in both cases that the consecutive “0”s and consecutive “1”s are read out.

3. POWER ANALYSIS

In 8T SRAM cell, a pair of NMOS transistors are added in each pull down path. Though the number of transistors are increased in the design compared to conventional 6t SRAM, power consumption is reduced considerably. When the word line is high, M5 turns on and the bit value on the bit line B, passes through M5 to the node Q. Because of charge sharing, the value at node Q discharges through M1, to ground. Hence value on node Q can’t be read properly. Therfore to retain the value at node Q, the discharging time should be increased. This is achieved by connecting M7 in series with M1 and M8 in series with M8. M7 and M8 must be sized properly, so that the total resistance of each pull down path should be increased. Thus the disharging time increases. Hence data read stability can be achieved.

As discussed above, the resistance of the pull down path increases. Hence the power consumption decreases according to the equation 1.

$$P = V^2/R \qquad (1)$$

In other context, the transistors connected in series reduces the capacitance which inturn reduces the power dissipation of the device.

In single-ended 6T, peripheral circuits such as precharge and sense amplifier, are eliminated and transmission gate is connected at node Q for reading the data. Thus the complexity of the SRAM memory cell is reduced and hence low power is achieved compared to 8T SRAM memory cell

4. SIMULATION AND RESULTS

Cadence Virtuoso Schematic Editor is used for circuit design and the circuit is analyzed and verified for functionality through simulations using Cadence Virtuoso Spectre tool. The total power measurement is done using Cadence Virtuoso ADE Visualization and Analysis XL Browser and XL Calculator.

3.1 Peripheral Circuits:

Peripheral circuits consists of pre-charge circuit, write circuit and sense amplifier which are shown below.

i).Precharge circuit

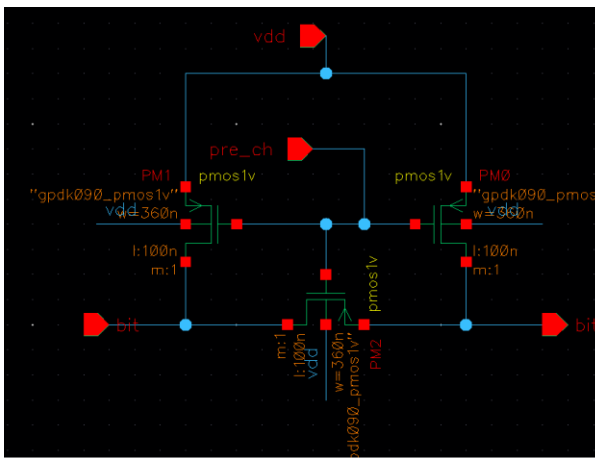


Figure 5: Schematic of pre-charge circuit

when pre_ch is logic 0,then both Bit and Bit' are charged to VDD whenever the SRAM cell is in inactive state. In active a state, pre_ch is disabled by making it high. The waveform of pre-charge circuit is shown in figure 6.

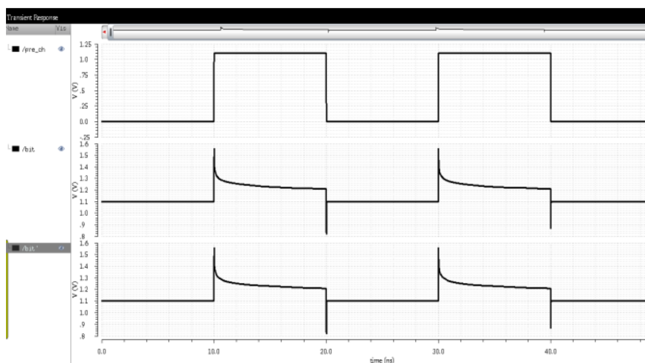


Figure 6: waveform of pre-charge circuit

ii).Write circuit

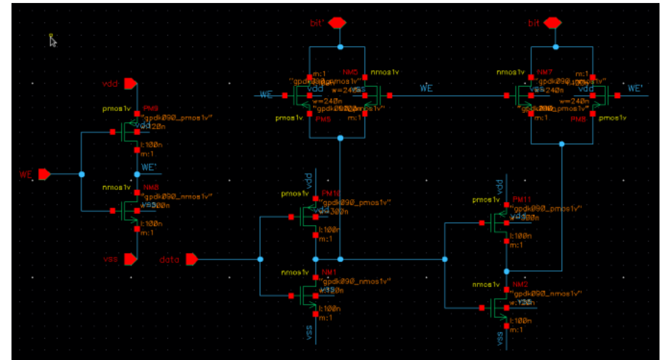


Figure 7: Schematic of write circuit

Whenever WE is enabled, data is written into the SRAM memory cell. If it is deactivated, then memory cell retains the previously stored data.

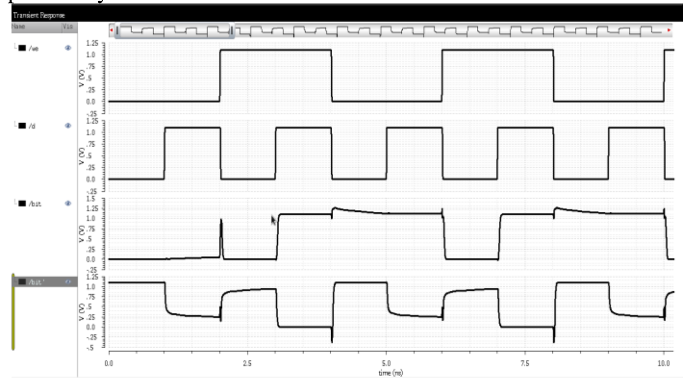


Figure 8: waveform of write circuit

iii). Sense Amplifier

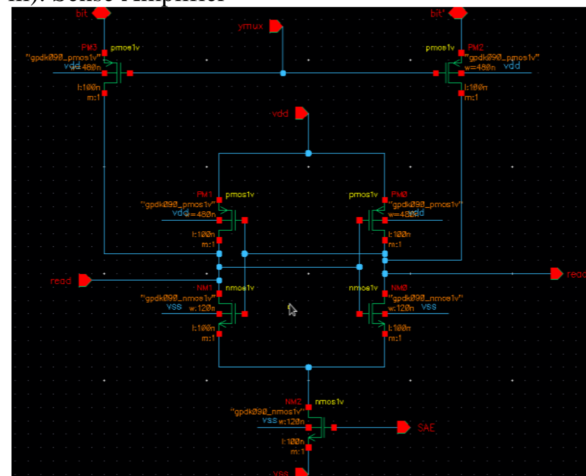


Figure 9: Schematic of sense amplifier

Sense amplifiers are used to sense which line is being pulled down and perform the read operation of the stored data. READ and READ_BAR indicate the data stored and its complement during the read operation

4.1 6T SRAM

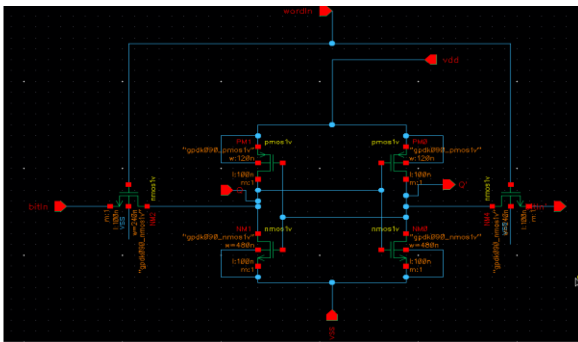


Figure 10:Schematic of 6T SRAM

Figure 11 shows the 6T SRAM connected to other peripherals such as pre-charge, write circuit and sense amplifier.

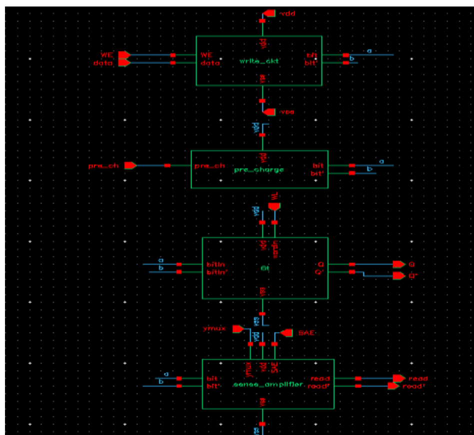


Figure 11 :6T SRAM with peripherals

When data to be written into the SRAM cell, pre-charge and Word line enble are made high.SE(sense amplifier Enable) is made low.Data to bo written is given at data line which is stored into SRAM cell and can be seen at output Q.The waveform is shown in figure 12. When ever the data to be need to read freom the SRAM cell, SE is enabled and output is read at read and read'.

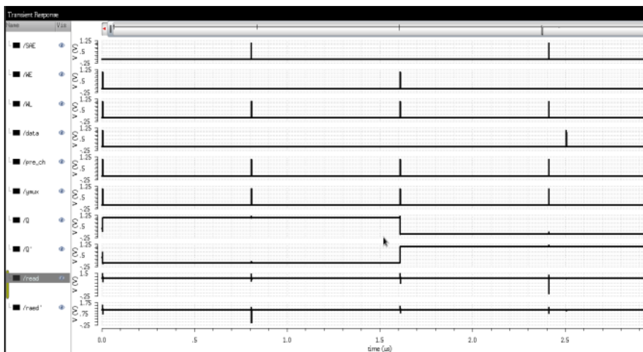


Figure 12 :Waveform of 1-bit memory cell using 6T SRAM

4.2. *8T SRAM*

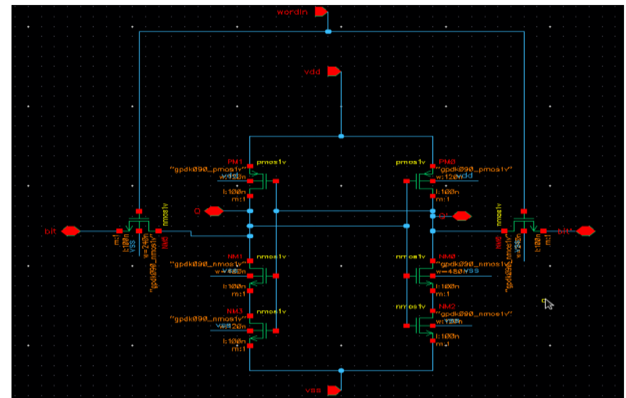


Figure 13: Schematic of 8T SRAM

Figure 14 shows the 8T SRAM connected to other peripherals such as pre-charge, write circuit and sense amplifier.

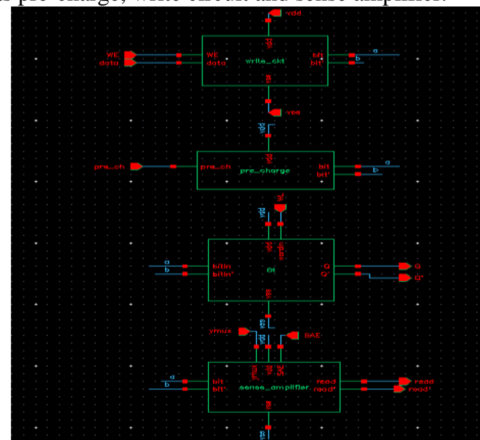
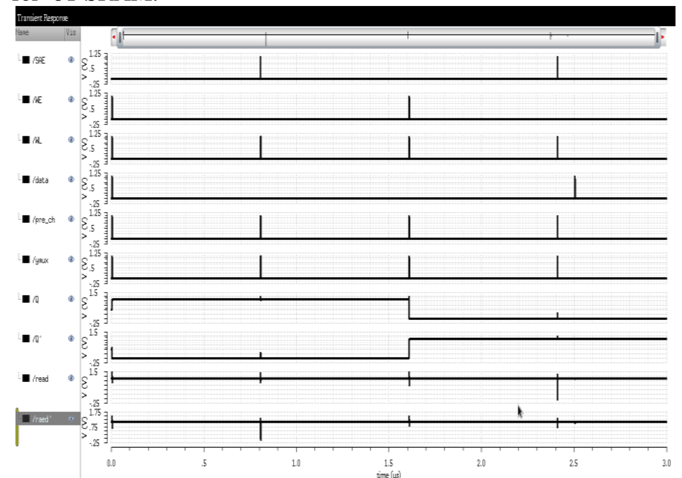


Figure 14 : 8T SRAM with peripherals

In this SRAM, same operation is done as previously explained for 6T SRAM.



. Figure 15: 8 T with peripherals-Waveform

4.3 Single Ended 6T SRAM Cell

In single ended design,there is no need of using sense amplifier and pre-charge circuit.only write circuit is used as peripheral circuit which considerably reduces the number of transistors which in turn reduces the area.

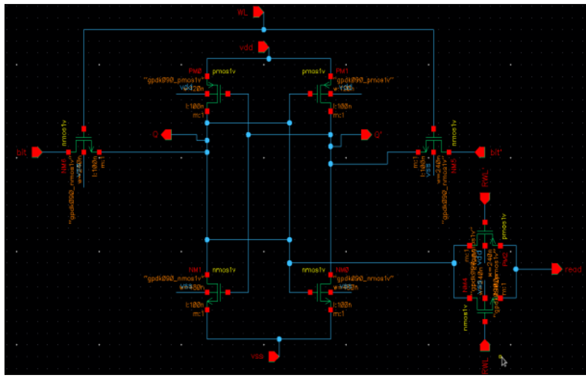


Figure 16 : Single ended 6T SRAM cell

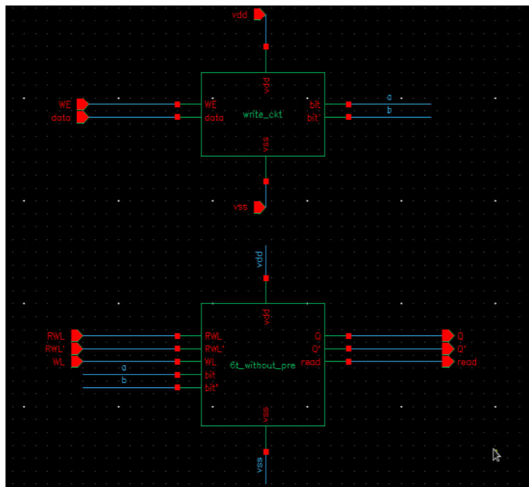


Figure 17 : Single ended 6T SRAM cell without pre-charge and sense amplifier

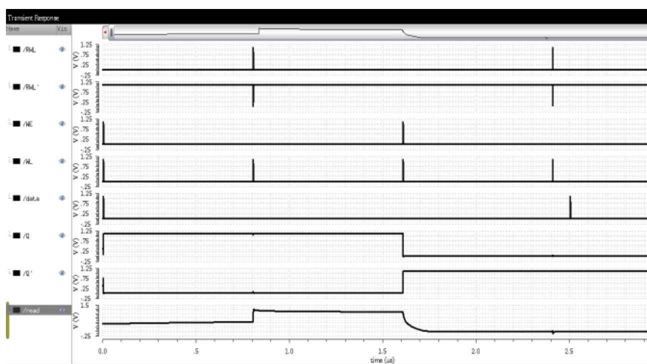


Figure 18 : Waveform of single ended 6T SRAM cell

All simulations were performed with Cadence Virtuoso tool in 90nm GPDK process. Simulations were carried out for the operating temperatures of -50^{0}C to 125^{0}C for 90nm with a power supply voltage of 1.1V

Table 1 shows the power consumption of different SRAM cell. The observation shows that single ended 6T SRAM cell consumes less power compared to convensional 6T and low power 8T SRAM.

Table 1: power analysis of 1-bit memory cell using different SRAM cells

Sl No.	1-bit SRAM Cell	Total Power(nW)
1	6T	446.7
2	8T	349.4
3	Single Ended 8T	276.6

5. CONCLUSION AND FUTURE SCOPE

The design and implementation of the SRAM memory cells to be a challenging and valuable learning experience. It gave us the opportunity to learn Cadence Virtuoso tools used in full custom IC design, and also gained deeper understanding of the challenges of deep submicron VLSI design. The static RAM is very widely used in CMOS systems. In single ended 6T, the power is reduced considerably compared to conventional 6T and 8T SRAM cell.

As the Single ended SRAM cell, consumes less power, reduces complexity, it can be used to design memory system of 16 bit,32bit , 64 bit and so on.

6. REFERENCES

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