International Journal of Computer Applications (0975 – 8887)
National Conference on Innovations and Recent Trends in Engineering and Technology (NCIRET-2014)

Controller Design for Buck Converter Step-by-Step Approach

Swapna Manurkar
Asst.Prof(Electrical)
Sknsits Lonavala

ABSTRACT
Almost all power supplies (Regulating / SMPS) require a closed –loop control the function of which is to keep the output matching with the reference value. For the above purpose either analog or digital methods can be used. In analog method an error is generated with the help of operation amplifier and can control the circuits of power supplies having capacity up to many megawatts. The present paper takes into simulation study of such a voltage mode PWM dc-dc buck converter in continuous conduction mode (CCM). Results for type1, 2, and 3 amplifiers is compared and presented.

Keywords
VM, CCM, error amplifier

1. INTRODUCTION
In the last ten years, switching regulators have received considerable attention because of the high performance requirements of power processing systems. Switch mode regulators have almost replaced the conventional dissipative series regulators because of their inherent superior characteristics, i.e., high efficiency, small size and weight, low volume, low weight, and equal reliability. These regulators are very useful in rectifier, inverter, chopper and ac voltage controller conversions and to buck or boost the voltage levels with isolation.[3]

For almost all the applications, SMPS delivers a parameter a Voltage or a current –whose values must remain constant, independent of various operating conditions, such as the input voltage, output loading, ambient temperature etc. To perform such a task a portion of circuit must remain insensitive to any of above variations. This portion is called a reference and is continuously compared to a fraction of converter output variable with feedback loop.

Loop analysis consists of studying the open loop/close loop gain i.e. phase response of transfer function mostly with the help of Bode plot and shaping it with the help of compensation network to stabilize against various input output conditions mentioned above.

The purpose or duty of compensating network is to settle the system as fast as possible after a variation in normal operating condition occurs. This compensating network is the controllers for converters. This controller takes a portion of the output variable and compares it with the stable reference. It then further amplifies the error between the signals, via the loop gain, to generate a corrective action. The control action consists of opposing the variations observed on the regulated output, hence the term negative feedback.

For a system to be stable, the loop gain must fall below unity by the time the total phase shift has reached 360 deg. The gain margin is defined as the amount of gain below unity when the total phase shift is 360 deg. The phase margin is defined as the difference between the actual phase shift when the loop gain is unity and 360 deg. Stability is sometimes described in terms of 180 deg of phase shift. This is because even at dc, the feedback is negative, i.e., there is a phase inversion of 180 deg.

Thus the main purpose of this paper is to present method for modeling and design of error amplifier for switching regulators.

2. ANALYSIS OF VARIOUS CONTROLLERS
In recent years, there are many SPICE-based models developed for simulating dc-de converters. In general, three types of model can be identified: the detailed model, the large-signal averaged model, and the small-signal model. All three models are valuable in analysis and design of dc to dc converter systems. The small-signal model is required to design the control system of a dc-dc converter Different types of controllers are possible for PWM converters [1]. The converter type and the transient response we need for our design will guide through selection of one particular controller type.

There are number of well documented techniques and guidelines for designing of controller for DC-dc converter [1-5]. Nevertheless, the design of a feedback compensator is still not a simple task, especially for a new designer. The task involves the tedious, mechanical and human error prone computation of the transfer functions, and repetitive fine tuning of compensation network component values. Moreover, the designer's judgment and experience are often required in the design process.

Various types of amplifiers are possible, with each one having its own specialty in order to compensate the given network. Following is the list and functions of the compensator network.

TYPE 1: it does not offer phase boost. It brings largest overshoot in sudden load change. This is widely used in PFC (power factor correction) circuits.

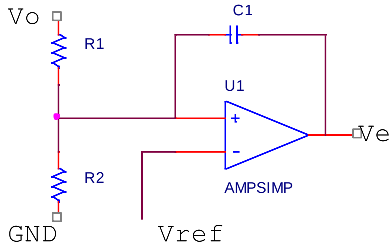


Fig1 : Type1 error amplifier

TYPE2: This compensation is most widely used in circuits where the effect of boost brought by the ESR capacitor is to be brought down.

TYPE2a: This is similar to TYPE 2 but where the effect of ESR can be neglected.

TYPE2b: This compensation technique offers superior transient response, but at the cost of reduced dc gain. This has an additional proportional term.

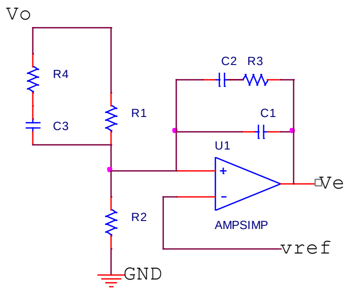


Fig2: Type3 error amplifier

Kfactor is another advanced tool available. The present paper does not take into consideration the methodology for this compensation technique. However through this paper we want to show the step by step procedure to design and decide the suitable compensator for DC- Dc converters.

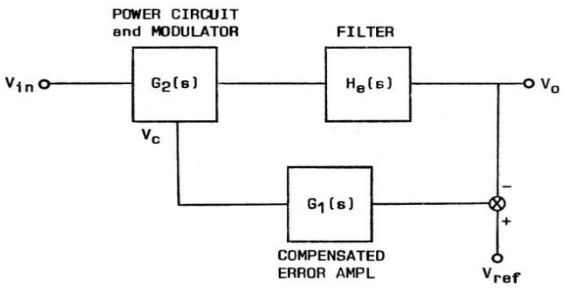


Fig3: Type3 error amplifier

The above fig shows the general block diagram for Dc- Dc converter with feedback or compensated error amplifier. Duty of design engineer is to select the correct block for required power stage. Through this paper we propose the design procedure of compensated error amplifier for VM CCM buck converter.

The actual circuit for buck converter in closed loop with negative feedback is as follows

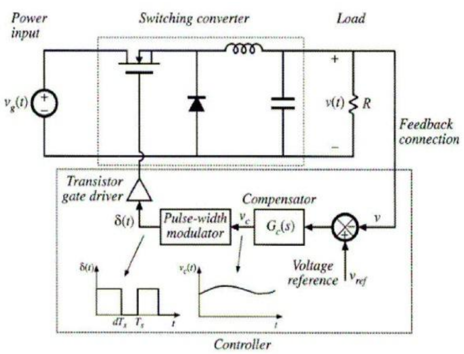


Fig4: closed loop diagram of buck converter with negative feedback

The output voltage is function of input voltage duty cycle and the load current as well as the converter circuit element values. However it is desired to obtain constant output voltage in spite of disturbances in input voltage, load current and element values.

So we cannot simply set duty cycle to single value and obtain a given constant output voltage under all conditions thus we have to go for a compensator network with negative feedback.

Following are the results of negative feedback on network transfer function

- It reduces the transfer function from disturbances to the output.
- It makes the transfer function to be insensitive to the changes in the in the gains in forward path of the loop.
- Feedback loop cause an otherwise stable system to become unstable.

3. DESIGN PROCEDURE

Regulator design consists of following steps:

1. Effect of load current variation on the output voltage regulation.
2. Effect of input voltage variation on the output voltage regulation.
3. Transient response time
4. overshoot and ringing

Each and every constraint impose limitation on the loop gain T(s) and hence a compensator is added.

The compensator network is designed to attain good phase margin and adequate rejection of expected disturbances.

Lead compensator or PD controllers are used to improve phase margin and extend the bandwidth of feedbackloop.lag compensator or PI controllers are used to increase low frequency loop gain. More complicated networks are used to have advantage of both approaches.

The process to select the compensator can be described as follows

Step1: for the given converter viz buck, boost or buck boost. Obtain the small signal model of the configuration

Step 2: find out the converter transfer function

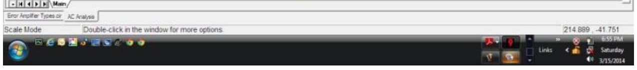
Step 3: obtain the gain plot or phase plot

Step4: find out the requirement of the circuit.

Step5: if no specific requirement is there then go for type1, type2 one by one to see the changes in the gain and phase plot.

Here type 2a results are shown.

Also comparison of different error amplifier is also presented.



4. RESULTS

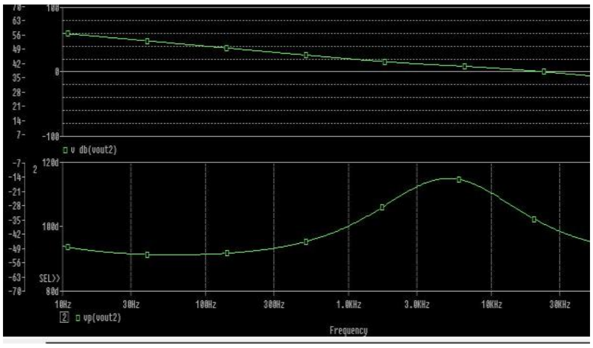


Fig 5 : Simulation Results of Type 2 a error amplifier gain and phase plot of output signal

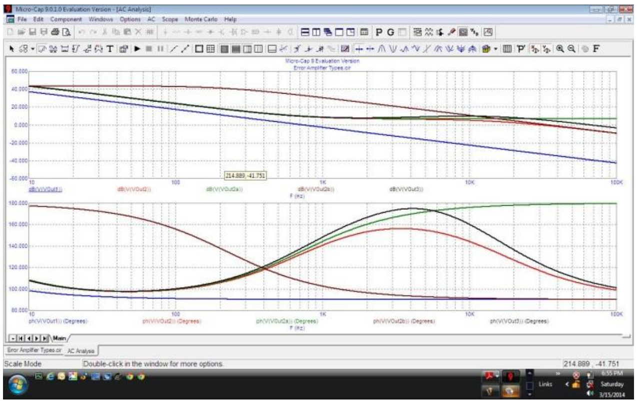


Fig 6 : Simulation Results of various error amplifier gain and phase plot of output signal

5. CONCLUSION

The above results show the gain and phase plot for small signal model of buck converter with type 2a error amplifier. After comparing the results with type1, type2 and type 3 it is observed that distinct difference in gain and phase is obtained. Also GM and PM with this type of amplifier is acceptable. The space and cost requirement also suggests that type2 is suitable for keeping output within range.

Also comparison of various error amplifiers shows their suitability over other.

6. REFERENCES

[1] Nik Din Muhamad and Abd laafar Sh!ifie, “An Approach to PSpice-aided Control Loop Design of DC-DC .Converter Systems,” National Power and Energy Conference (PECon) 2003 Proceedings, Bangi, Malaysia*)*

[2] Marian K. Kazimierczuk, Nehru Sathappan, and Dariusz Czarkowski “Voltage-Mode-Controlled PWM Buck DC-DC Converter with a Proportional Controller,” 1993 IEEE

[3] P.R.K. chetty, “Modeling and Design of Switching Regulators”, Sundstrand Advanced Technology Corporation, IEEE transactions on aerospace and electric systems vol. aes-18, no.3 may 1982.

[4] Error Amplifier Design and Applications, Technical Note #3.

[5] Fundamentals of power electronics second edition.R.W EricksonSIE.

[6] Switch mode power supplies –SPICE simulation and practical designs-Cristophe P Basso Mc Graw Hill