# Modelling Of Compact Models of Carbon Nanotube Field Effect Transistors with VHDL-AMS

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## ABSTRACT
This paper related to modelling and simulation of the carbon nanotube field effect transistor (CNTFET). There are two compact models for CNTFET's, the first which behaves like a MOSFET is known as the classical behaviour model and the other one is schottky barrier CNTFET is known as ambipolarbehaviourmodel . Like MOSFET devices these models implemented in VHDL-AMS. MOSFETs are modelled in VHDL which is a hardware description language and results are simulated on the simulators. CNTFET models are implemented on VHDL-AMS and have been compared with numerical simulation.

## Keywords
CNTFET, VHDL, MOSFET

## 1. INTRODUCTION
In last few years Siliconbased technology has experienced phenomenal growth. MOS transistors are most successful component in semiconductor industry because they have the property of scaling. From this property designers can scale down the dimensions, which results in higher performance. But there are certain limitations with MOSFET size that's why the silicon industry search out the new material to integrated the devices based on the current silicon based technology. The electrical properties of the CNTFETs are superior to the MOSFETs for this reason they can be the best option to replace the MOSFETs.

From the invention of the transistor till now the size of transistor and the electronic circuits size is continuously reduce and the power dissipation is also reduced. This feature of size reduction is represented by well-known "Moore's law". This law represents the evolution in transistor industry with growing years. However as the feature size becomes smaller, scaling the silicon MOSFET becomes increasingly harder. This increasing challenge is often attributed to: quantum mechanical tunnelling of carriers through the thin gate oxide, quantum mechanical tunnelling of carriers from source to drain and from drain to body and control of the density and location of dopant atoms in the channel and source/drain region to provide high on/off current ratio.

This limitation can be resolved with many other solutions. There can be two type solutions- first can modified the existing material properties orstructures.Other solution is using the new material, new structure which will replace the old one completely. From the second solution the silicon material replaced by the Carbon and the transistor or MOSFET structures replaced by the Carbon Nanotube based field effect transistors.

These new technologies and devices require the creation of accurate compact models, suited to the circuit design and easily translatable into a hardware description language (HDL) such as VHDL-AMS.

In this paper author proposed two compact models for CNTFETs, the first one with a conventional behaviour (i.e. a MOSFET behaviour), and the second one with an ambipolarbehaviour. The former is based on an existing model developed at Purdue University. Unfortunately, in its present form, this model is not appropriate for circuit simulation. In this paper, author proposed an efficient compact model for the designer, with a range of validity clearly defined. The second model is devoted to compact modelling of the CNTFET with an ambipolarbehaviour(n- or p-type depending of the gate voltage value). This characteristic is quite different from a classic behaviour, namely MOSFETbehaviour. To our best knowledge, this compact model is the first analytical ambipolar model for CNTFET introduced in the literature. It is a behavioural compact model that simulates in a realistic way the ambipolar characteristic observed with Schottky-Barrier.

The paper is organized as follows. Section II provides some background CNTFETs and MOSFET's like CNTFET's. In Section III author tells about the Quantum-Capacitance Derivation VHDL-AMS implementations simulations result. Section IV Conclusion and section V about the references.

## 2. CARBON NANOTUBE FIELD EFFECT TRANSISTOR
In Future nanoelectronic technology the Carbon nanotubes (CNTs) are considered as promising building blocks.In CNT hollow cylinders composed of one or more concentric layers structure the carbon atoms are bonded with each other in honeycomb lattice arrangements. Single-walled nanotubes (SWCNTs) typically have a diameter of 1–2 nm and a length up to several micrometers. The large aspect ratio makes the nanotubes nearly ideal one-dimensional (1-D) objects, and as such the SWCNTs are expected to have all the unique properties predicted for these low-dimensional structures [1]. SWCNTs can be metallic or semiconducting depending on the detailed arrangement of the carbon atoms.Two types of semiconducting CNTs are being extensively studied. One of these devices is a tunnelling device. These devices works on the principle of direct tunnelling through a Schottky barrier at the source-channel (and drain-channel) junction.By the application of gate voltage the barrier width is modulated and thus the transconductance of the device is dependent on the gate voltage. To overcome these problems associated with the SB CNTFETs, there have been attempts to develop CNTFETs which would behave like normal MOSFETs. In

this MOSFET-like device, the ungated portion (source and drain regions) is heavily doped and the CNTFET operates on the principle of barrier-height modulation by application of the gate potential. In this case, the on-current is limited by the amount of charge that can be induced in the channel by the gate. It is obvious that the MOSFET-like device will give a higher on-current and, hence, would define the upper limit of performance.

Transport through short nanotubes has been shown to be free of significant acoustic and optical phonon scattering and thus is essentially ballistic at both high and low voltage limits. In the following, we consider MOSFET-like mode of operation, and assume ballistic transport. The theory of CNT transistors is still primitive andthe technology is still nascent. However, evaluation of such high-performance transistors in digital circuits is absolutely essential to drive the device design andunderstand the bottlenecks in multi-gigahertz processor design. However, from the circuit designer's pointof view, circuit simulation and evaluation using CNTFETs is challenging because most ofthedeveloped models are numerical, involving self-consistent equations which circuit solvers like SPICE are not able to handle.

## 2.2 MOSFET-like CNTFET

First, author present a compact model for CNTFETs with a classical behaviour. This compact model is based on a CNTFET model developed at Purdue University [16]. To our best knowledge, this is the first compact model(i.e., fully dedicated to circuit simulation)of CNTFET available in the literature. It is a surface potential-based SPICE compatible model that enables to simulate CNTs with ballistic behaviour. It has been incorporated in HSPICE but is not well-suited for circuit simulation due to some convergence issues.

In this paper, author proposed a modified model with fundamental improvements solving the convergence problems of the original model. The new model is applicable to a wide range of CNTFETs with diameters between 1 to 3 nm and for all chiralities as long as they are semiconducting. The model uses suitable approximations necessary for developing any quasi-analytical, circuit-compatible compact model. Quasi-static characteristics (I-V) have been modelled and validated against numerical models, with an excellent agreement. The computational procedure to evaluate the drain current $I_D$ and the total channel charge $Q_{CN\ T}$ is illustrated. The main quantities used in the model are the surface potential $\psi_S$ (or control potential) and the specific voltage $\xi_{S(D)}$ that depends on the surface potential, the sub bands energy level $_p$ and the source (drain) Fermi level $\mu_{S(D)}$. The conduction band minima for the first sub band is set to half the nanotube bandgap

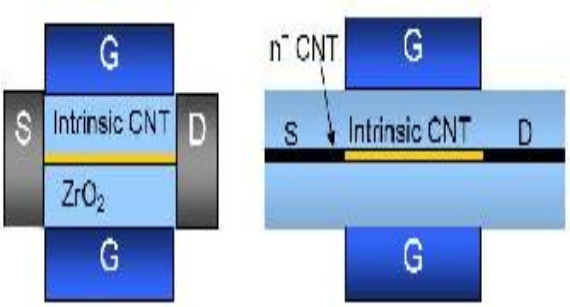


**Figure 1: Different types of CNTFETs: (a) Schottky-barrier (SB) CNTFET with ambipolarbehaviour, and (b) MOSFET-like CNTFET with classic behaviour.**

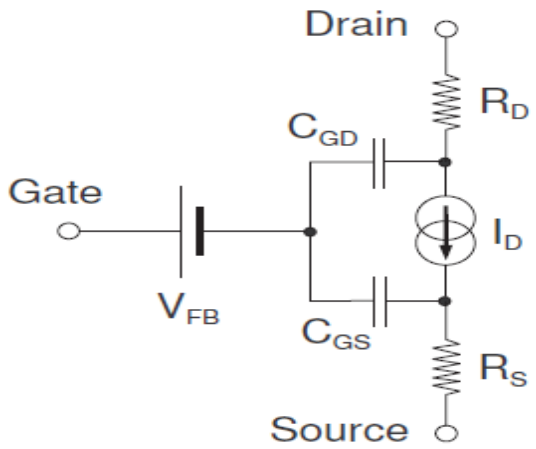


**Figure 2: Schematic of the CNTFET compact model.**

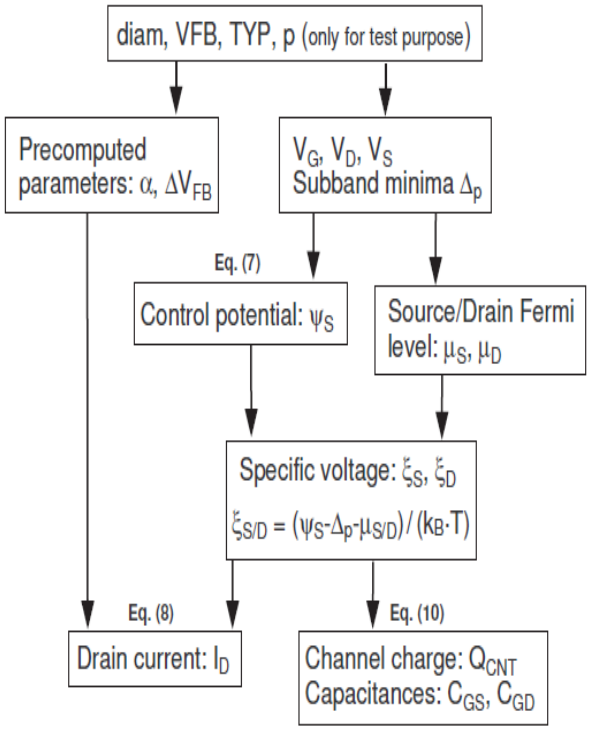


**Figure 3: Structure of the CNTFET compact model.**

The physical parameter diam is the nanotube diameter (in nm); it is one of the only three intrinsic parameters of our model, with the flatband voltage $V_{FB}$ and the TYP parameter (= +1/ − 1 for n- or p-type device). Let us emphasize the number of subbands p has been added as an input parameter only for test purpose [13].

Determination of the surface potential an important step in the model development is to re-late the control potential with the gate bias voltage. The knowledge of $\psi_S$ is useful to calculate the specific voltage $\xi$. This allows us to determine the drain current and the total charge. In [16], the following approximation has been proposed

$$Vgs - \Psi s = \begin{cases} 0 & for \quad Vgs < \Delta 1 \\ \alpha(Vgs - \Delta 1 & for\ Vgs \geq \Delta 1 \end{cases} \quad (1)$$

Where the $\alpha$ is given by

$$\alpha = \alpha_0 + \alpha_1 . V_{ds} + \alpha_2 . V_{ds}^2$$

where the parameter α is given by $\alpha = \alpha 0 + \alpha 1\ V_{DS} + \alpha 2\ V^2_{ds}$

where $\alpha_0$, $\alpha_1$ and $\alpha_2$ are dependent on both CNTFET diameter and gate oxide thickness [14]. Eq. (1) is correct to model the relationship between the gate volt-age and the surface potential, but is not well-suited for a compact model. Therefore, we propose an equivalent solution, given, but with an excellent behaviour of the derivative .

$$\Psi s = Vgs - \frac{\alpha(Vgs - \Delta 1) + \sqrt{[\alpha(Vgs - \Delta 1)]^2 + 4\epsilon^2}}{2}$$

## 3. QUANTUM-CAPACITANCE DERIVATION

With the knowledge of charge and surface potential as functions of gate bias, the gate input capacitance $C_G$ can be computed in terms of the device parameters and terminal voltages. The gate-input capacitance is given by

$$C_G = \frac{\partial Q_{CNT}}{\partial V_{gs}} \Rightarrow C_G = \frac{\partial Q_{CNT}}{\partial \Psi_S} . \frac{\partial \Psi_S}{\partial V_{gs}} (3)$$

The total charge $Q_{CNT}$ can be split up into $Q_S$ and $Q_D$ and, hence, the total gate capacitance can also be split up into $C_{GS}$ and $C_{GD}$ (see Fig. 2).To elaborate an efficient expression of $C_G$ for a com-pact model, it is important to first have a closed-form expression of $Q_{CNT}$ ($\psi_S$ ) and continuous derivatives of(3) as well as it is not possible to obtain a closed-form relationship for the quantum-charge in the channel, an empirical solution (fit) has been proposed in [16]. Noting that the number of carrier n increases almost linearly as ξ increases and falls off exponentially as ξ becomes negative, the following

$$n = \begin{cases} N_0 . A . exp\xi & for\ \xi < 0, \\ N_0 . (B . \xi + A) & for \xi \geq 0. \end{cases} \quad (4)$$

Where the parameters A and B are dependent on the energy level Δ.

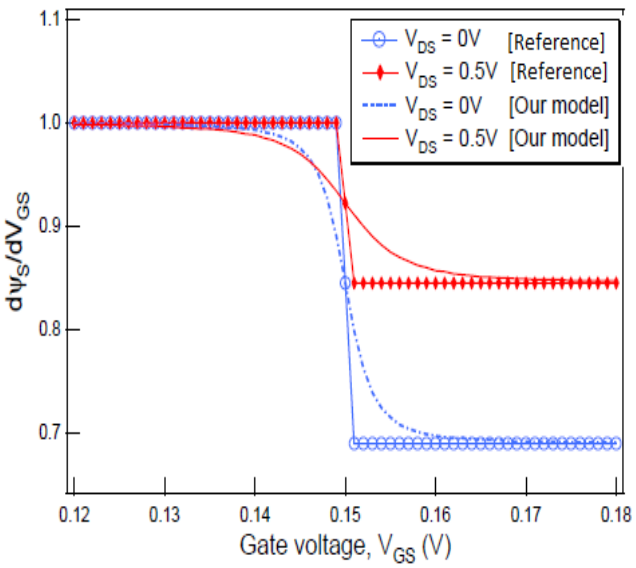


**Figure 4: Derivative of surface potential $\psi_S$ vs. $V_{GS}$ .**

Eq. (4) is unfortunately not appropriate for circuit simulation because its derivatives are not continuous (Fig. 4). So, the diff erent capacitances determined would not be correct to elaborate the CNTFET dynamic model. In addition, this would lead to numerical problems during simulation and wrong results.

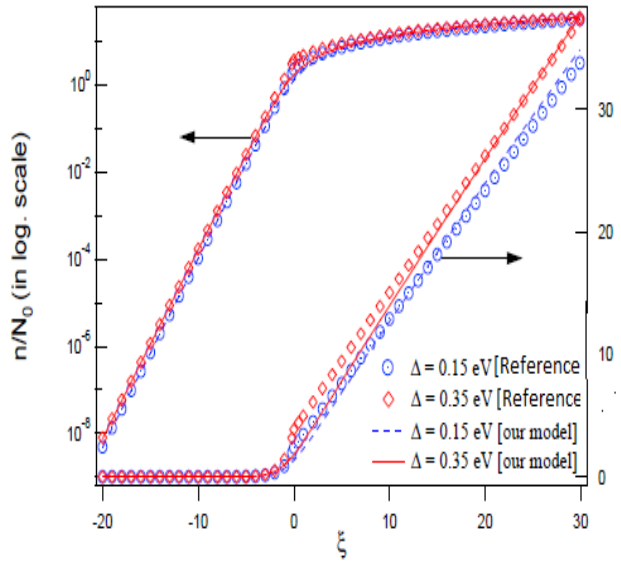


**Figure 5 : n/N o vs. ξ as a function of the energy level**

In order to solve the numerical problems, we have elaborated a new equation for n, similar to the interpolation function of the EKV MOSFET model [2]. This new expression and its derivatives are continuous [Fig. 5] and more appropriate for circuit simulation, especially in dynamic operation. Fig. 5 shows a comparison between (10) and our continuous equation. Let us note that the greatest difference can be observed around zero, where actually the former overestimates the quantum-charge.

Fig. 6 shows the drain current of a 1.4 nm diameter CNTFET with $C_{ox}$ = 3.8 pF/cm as a function of gate voltage. The dots correspond to the numerical solutions performed with the FETTOY simulator [nan] whereas the lines correspond to our

analytical compact model. A good agreement is found, which supports the validity of our approach.

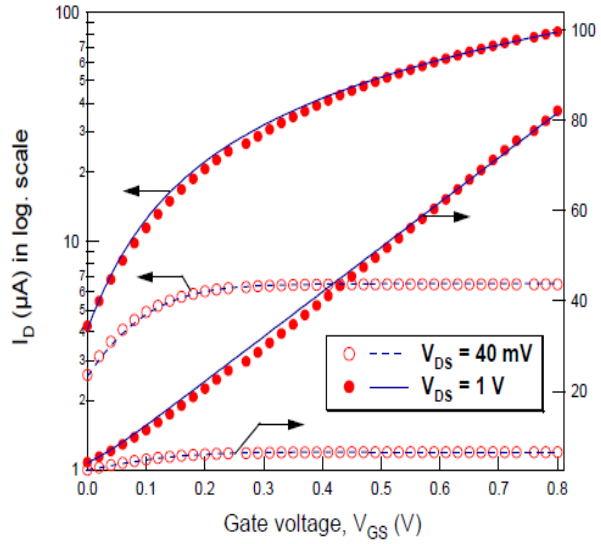


**Figure 6: Comparison between the results extracted from VHDL-AMS and numerical simulations (lines and dots, respectively) for the drain current of a MOSFET-like CNTFET (p=1, diam=1.4, TYP=+1, VFB=0).**

## 3.1 VHDL-AMS implementations

First, author has calibrated the model of Purdue with respect to numerical simulations. The best fits were obtained with p = 1 (i.e. one subband) which is coherent because the FETTOY simulator only accounts for the lowest subband. So, at the beginning, we fixed p = 1 in our model in order to validate it with respect to the numerical simulations. Then, if we consider CNTFETs with diameters ranging from 1 to 3 nm, and with a power supply lower than 1 V, we can set p = 5 to accurately describe all cases [17].
The whole VHDL-AMS code of the model requires about 90 lines. Only three **intrinsic** parameters are necessary: diam, TYP (+1 for n-type, -1 for p-type) and $V_{FB}$ .

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entity CNTFET is

    generic(diam  : real := 1.4; --diameter [nm]
                                 --n/p-CNTFET  (+1/-
    TYP           : real  := 1.0;  1)

    VFB           : real  := 0.0;  --flatband voltage

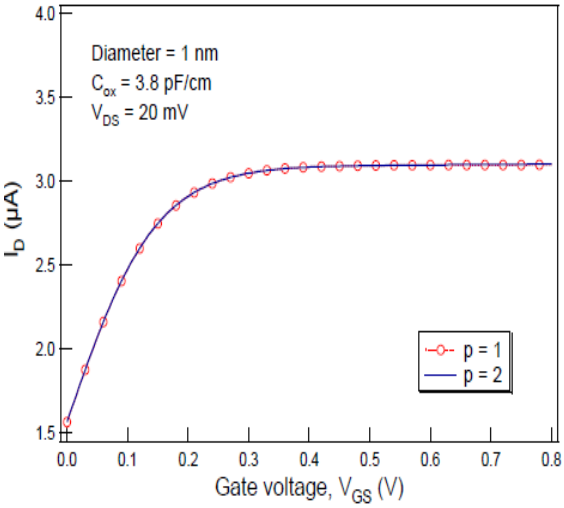
p : positive := 1; --subbands number

Rseries : real := 50.0e3); --RS+RD [ohm]

port(terminal g,d,s : electrical);

end;
```

Let us note that the number of subbands p has been defined as a generic parameter only for test purpose [14]. The parameters $\alpha_0$, $\alpha_1$ and $\alpha_2$] are determined in a precomputed module, with the help of one equation for each of them. For all details about the computation of the parameters α, the reader is referred to [14].



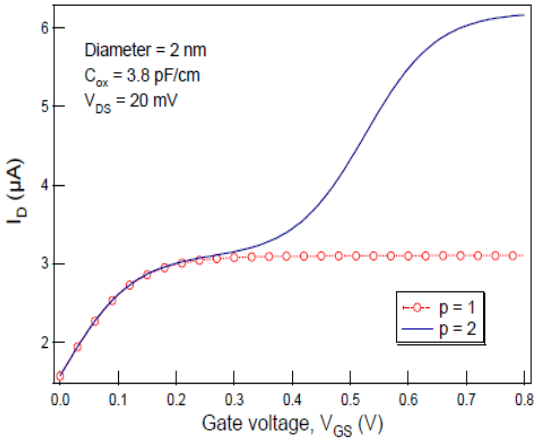




**Figure 7: VHDL-AMS simulations of $I_D$ vs. $V_{GS}$ at low drain bias.**

To conclude this section, Fig. 8 shows two VHDL-AMS simulations performed for different values of the parameters diam and p, in order to show the effect of the nanotube diameter on the number of subbands p to be accounted for. This behaviour may be useful to create novel multiple-valued logic design [17].

# 4. AMBIPOLAR CNTFET

Author present, for the first time to our best knowledge, a behavioural compact model that allows describing the ambipolar characteristic of SB CNTFETs. This model is built using the new model of CNTFET previously presented; an additional part has been added to the original model [17]. The entity (VHDL-AMS) corresponding to this new model is the same as the classical CNTFET model one.

The very particular $I_D$ –$V_{GS}$ characteristic of the ambipolarCNTFET is illustrated in Fig.8. It should be noted that this behaviour is quite similar to the numerical simulation results recently published in [9] and [5]. This ambipolar characteristic should allow circuit designers to devise new architectures using that specific behaviour [18]. Our compact model may be of help to this issue.

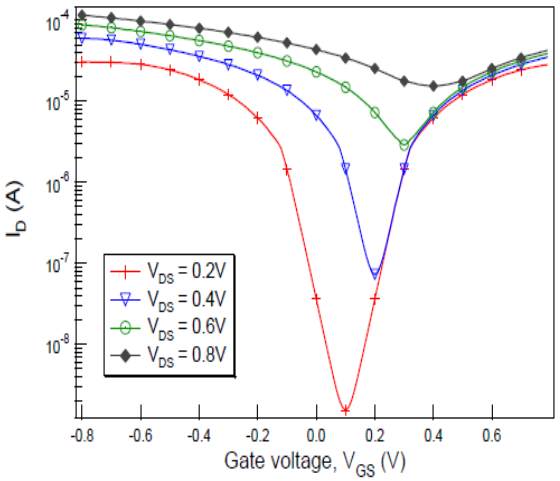



**Figure8: VHDL-AMS simulation of the drain current as a function of gate voltage for the ambipolar SB CNTFET (p=1, diam=1.4, TYP=+1, VFB=0).**

## 5. CONCLUTION

In this paper, different VHDL-AMS models for emerging technologies have been proposed. The paper deal with the compact modelling of the CNTFET with VHDL-AMS.Two CNTFET compact models have been presented, [9] the first one for carbon nanotubes with a classical behaviour (like MOSFET), and the second one for devices with an ambipolarbehaviour. Although CNTFET technology is still nascent, these compact models developed in VHDL-AMS are useful tools to help the designers to devise new architectures.

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## 7. REFERENCES

[1] P. Avouris, J. Appenzeller, R. Martel, andS.J. Wind.carbon nanotube electronics.proc. of IEEE, 91(11):1772–1784, 2003.

[2] C. Enz, F. Krummenacher, and E. Vittoz.An analytical MOS transistor model validin all regions of operation and dedicated tolow-voltage and low-current applications.journal of AICSP, pages 83–114, 1995.

[3] D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, and H-S.P. Wong. Device scaling limits of Si MOSFETs andtheir application dependencies. Proc. of [PLV05] IEEE, 89(3):259–288, 2001.

[4] J.G. Fossum, L. Ge, M-H. Chiang, V.P. Trivedi, M.M. Chowdhury, L. Mathew, G.O. Workman, and B-Y. Nguyen. A process/physics-based compact model for nonclassical CMOS device and circuit de-sign. Solid-State Electron., 48:919–926, 2004.

[5] J. Guo, S. Datta, and M. Lundstrom.A numerical study of scaling issues for schottky-barrier carbon nanotube tran-sistors. IEEE Trans. Electron Devices, 51(2):172–177, 2004.

[6] L. Ge and J.G. Fossum. Analytical model-ing of quantization and volume invesion in thin Si-film double-gate MOSFETs. IEEE Trans. Electron Devices, 49(2):287–294, 2002.

[7] J. Guo, M. Lundstrom, and S. Datta.Performance projections for ballistic car-bon nanotube field-effect transistors. App. Phys. Letters, 80(17):3192–3194, 2002.

[8] International technology roadmap for semiconductors 2004 update. [Online]. Available: http://public.itrs.net/ [May 2005].

[9] [9]J. Knoch, S. Mantl, and J. Appen-zeller.Comparison of transport propoer-ties in carbon nanotube field-effect tran-sistors with Schottky contacts and doped source/drain contacts. Solid-State Elec-tron., 49:73–76, 2005.

[10] NANOHUB online simulations and more, CNT bands. [Online]. Available: http://www.nanohub.org [April 2006].

[11] F. Pr´egaldiny, F. Krummenacher, B. Di-agne, F. Pˆecheux, J-M.Sallese, and C. Lallement. Explicit modelling of the double-gate MOSFET with VHDL-AMS.

[12] Int. Journ. of Numerical Modelling: Elec. Networks, Devices and Fields, 19(3):239– 256, 2006.

[13] F. Pr´egaldiny, F. Krummenacher, J-M.Sallese, B. Diagne, and C. Lallement.An explicit quasi-static charge-based compact model for symmetric DG MOSFET.InNSTI-Nanotech 2006, WCM, volume 3, pages 686–691, 2006. ISBN 0-9767985-8-1..

[14] F. Pˆecheux, C. Lallement, and A. Va-choux.VHDL-AMS and Verilog-AMS-static charge-based compact model for symmetric DG MOSFET.InNSTI-Nanotech 2006, WCM, volume 3,pages 686–691, 2006. ISBN 0-9767985-8-1.

[15] F. Pˆecheux, C. Lallement, and A. Va-choux.VHDL-AMS and Verilog-AMSasalternative hardware description languages for efficient modelling of multi-discipline systems. IEEE Trans. Computer-Aided Design, 24(2):204–224, 2005.

[16] Raychowdhury, S. Mukhopadhyay, andRoy. A circuit-compatible model of bal-listic carbon nanotube field-effect transis-tors. IEEE Trans. Computer-Aided De-sign, 12(10):1411–1420, 2004.

[17] Raychowdhury and K. Roy. Carbonnanotube-based voltage-mode multiple-valued logic design. IEEE Trans. Nan-otechno., 4(2):168–179, 2005.

[18] R.Sordan,K.Balasubramanian,M. Burghard, and K. Kern. Exclusive-ORgate with a single carbon

nanotube.App.Phys.Letters, 88, 2006. 053119.

[19] J-M. Sallese, F. Krummenacher, F. Pr´e-galdiny, C. Lallement, A. Roy A, andC. Enz. A design oriented charge-basedcurrent model for symmetric DG MOSFET and its correlation with the EKV formalism. Solid-State Electron., 49(3):485–489, 2005.

[20] J-M.SalleseandA.S. Porret.Anovelapproach to charge-based non-quasi-staticmodel of the MOS transistor valid in allmodes of operation. Solid-State Electron44:887–894, 2000.

[21] Y.Taur.Ananalytical solution toa double-gate MOSFET with undopedbody.IEEE Electron Device Lett.,21(5):245–247, 2000.

[22] Y.Taur, X. Liang, W. Wang, and H. Lu. Acontinuous, analytic drain-current modelfor DG MOSFETs. IEEE Electron DeviceLett., 25(2):107–109, 2004.