A Novel Full Adder with High Speed Low Area

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ABSTRACT

In most of the digital systems adder lies in the critical path that effects the overall speed of the system. So enhancing the performance of the 1-bit full adder cell is the main design aspect. The paper proposes the novel design of a 3T XOR gate combining complementary CMOS with pass transistor logic. The design has been compared with earlier proposed 4T and 6T XOR gates and a significant improvement in silicon area and power-delay product has been obtained. An eight transistor full adder has been designed using the proposed three transistor XOR gate. Compared to the earlier designed 10, 14, 16 transistor full adder, the proposed adder shows a significant improvement in silicon area and power delay product.

Keywords: XOR gate,full adder, improvement in speed, area minimization, transistor count minimization.

1.INTRODUCTION

Ever since its inception, the design of full adders which forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement, being motivated by three basic design goals,viz. minimizing the transistor count, minimizing the power consumption and increasing the speed [1-12]. Hosseinzadeh, Jassbi and Navi emphasized on circuit performance improvement in [1] through transistor count minimization. XOR gates form the fundamental building block of full adders. Enhancing the performance of the XOR gates can significantly improve the performance of the adder.

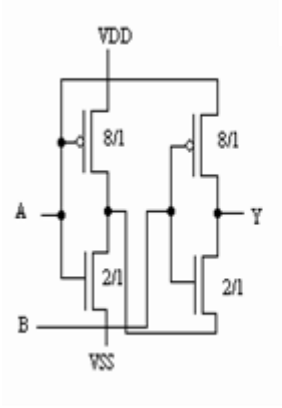


Fig. 1. (a)

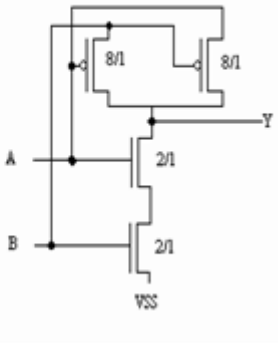


Fig. 1(b)

The early designs of XOR gates were based on either Eight transistors [3] or six transistors[3] that are conventionally used in most designs. Over the lastdecade, considerable emphasis has been laid on the design of four-transistor XOR gate [2, 4, 5, 6, 7, 8, 9, 10, 11]. Radhakrishnan proposed a formal approach of minimizing the transistor count in XOR and XNOR gates in [2]. Wang, Fang and Feng in [4] proposed novel XOR architectures shown in figures 1 (a) and (b) that could operate without requiring complementary inputs which is a severe drawback of CMOS transmission gate logic based XOR gates shown in [3]. The values of W/L ratios of the transistors have been shown in the figure besides the respective transistors. Bui, Wang and Jiang further improved the XOR gate proposed in [4] and designed a XOR gate without a V_{DD} [5] shown in figure 1(c). They further designed adders with some improvements in power delay products and used these XOR gates in their design [6, 7] but the silicon area remained unchanged. However, the proposed XOR gates consumed considerable silicon area for their optimum performance and the power delay product is also large. Wang, Fang and Feng also proposed another XOR gate in [4] and further studied by Shams, Darwish and Bayoumi in [8]. With a view of further optimization of performance of XOR gates in terms of silicon area and power delay product, considerable emphasis has been given in the present work on the design of three transistor XOR gates.

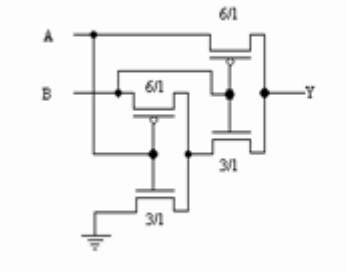


Fig. 1(c)

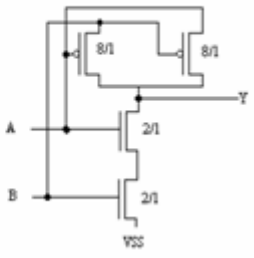


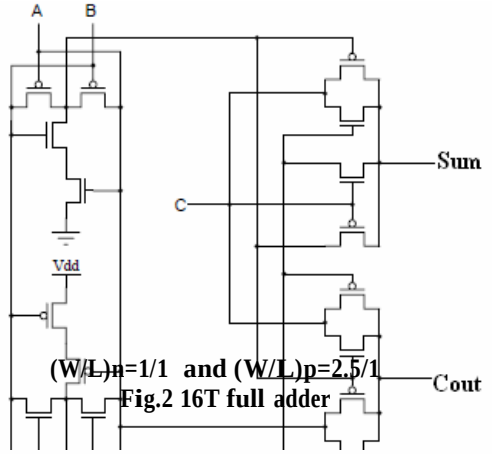
Fig. 1(d)

Fig. 1 Previous designs of XOR gates found in literature

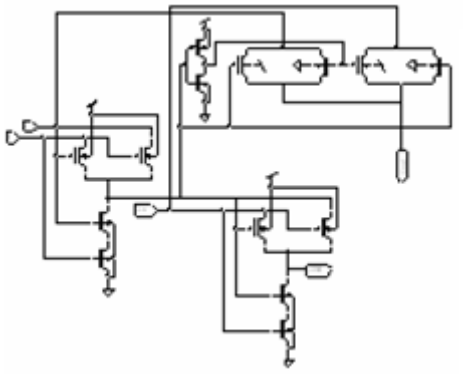
2. PREVIOUS WORK

The literature survey reveals very spectrum availability of adder designs over the past few decades. Several designs of low power and high speed adder cells are available in the literature. The full adder cell realization of the circuit using 16 transistor [1] is shown in Fig.2 This circuit can operate with

full output voltage swing but consumes significant amount of power and have more delay compared other adders having less transistor count.



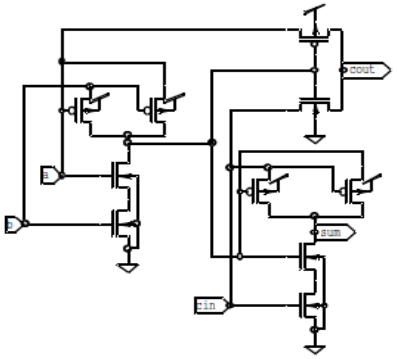
(W/L)n=1/1 and (W/L)p=2.5/1
Fig.2 16T full adder



(W/L)n=1/1 and (W/L)p=2.5/1
Fig.3 14T full adder

With the aim of further minimizing the number of transistor pass transistor logic based XOR and XNOR circuits [2] were used and as a result the 14T full adder circuit of Fig.3 was designed.

This circuit among all 14T full adder circuit [3],[4] shows the better results for delay and power as compared to 16T full adder but it suffers from the threshold loss problem of approximately 0.4v. It works well in high performance multipliers with low power consumption.



(W/L)n=1/1 and (W/L)p=2.5/1
Fig.4 10T Full adder

The further designed 10T full adder [5] of Fig.4 uses inverter-based 4T XOR gates in their design and shows remarkable results in power and delay. It also reduces the silicon area. This reveals better performance than the SERF 10T adder cell [5]. The drawback of this circuit is that it also suffers from threshold loss problem 0.35v approximately equal to 14T adder circuit.

3. DESIGN OF THREE-TRANSISTOR XOR GATE

The design of the full adder is based on the design of the XOR gate. The proposed design of full adder uses three transistor XOR gates. The design of a three transistor XOR gate is shown in figure 5. The design is based on a modified version of a CMOS inverter and a PMOS pass transistor. When the input B is at logic high, the inverter on the left functions like a normal CMOS inverter.

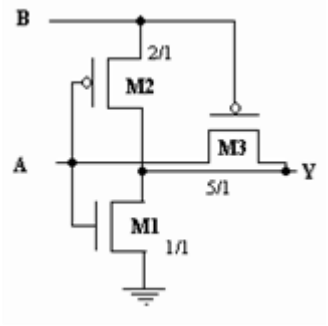


Fig. 5 Design of 3T XOR gate

Therefore the output Y is the complement of input A. When the input B is at logic low, the CMOS inverter output is at high impedance. However, the pass transistor M3 is enabled and the output Y gets the same logic value as input A. The operation of the whole circuit is thus like a 2 input XOR gate. However, when A=1 and B=0, voltage degradation due to threshold drop occurs across transistor M3 and consequently the output Y is degraded with respect to the input. The voltage degradation due to threshold drop can be considerably minimized by increasing the W/L ratio of transistor M3. Specifically from [22].

4. PROPOSED 8T FULL ADDER

This design of proposed full adder is based on three transistor XOR gate. It acquires least silicon area. The design of 3T XOR gate is shown in Fig.3. The heart of the design is based on a modified version of a CMOS inverter and a PMOS pass transistor. The Boolean equation for the design of the 8T full adder as follows:

$$S = A \oplus B \oplus Cin$$

$$Cout = Cin\,(A \oplus B) + AB$$

The logic circuit of the full adder is shown in figure 6. The OR gate can be realized using a wired OR logic [23].

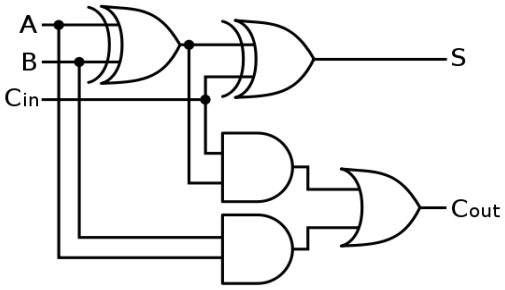


Fig. 6 Logic Circuit of the full adder

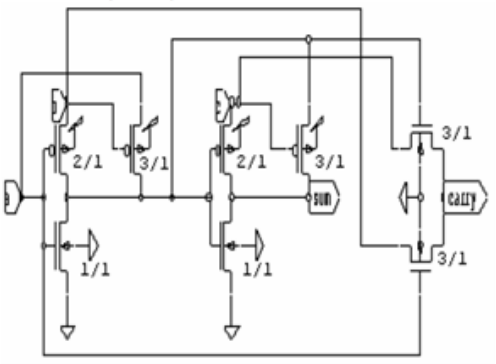


Fig. 7 Design of the eight transistor full adder

The circuit diagram of the eight transistor full adder is shown in fig.7. The sum output is basically obtained by a cascaded exclusive ORing of the three inputs in accordance with equation 1. The carry output is obtained in accordance with equation (2). The final sum of the products is obtained using a wired OR logic. The W/L ratios of transistors M1-M6 are same as the corresponding ones in figure 3. The W/L ratios of transistors M7 and M8 are taken as 5/1. It is quite evident from figure 6 that two stage delays are required to obtain the sum output and at most two stage delays are required to obtain the carry. The voltage drop due to the threshold drop in transistors M3 and M6 in figure 7 can be minimized by suitably increasing the aspect ratios of the two transistors. However, the threshold voltage drop of $|V_{T,p}|$ provided by the pMOS pass transistor M3 when a=0 and b=0 is used to turn on the nMOS pass transistor M8 and therefore we get an output voltage equal to $|V_{T,p}|-V_{T,n}$, where $V_{T,p}$ is the threshold voltage of the pMOS transistor and $V_{T,n}$ is the value is very close to 0V. Similarly, the threshold drop of the transistors M7 and M8 can be minimized by suitably increasing the aspect ratios of transistors M7 and M8.

5. SIMULATION RESULTS & LAYOUT DESIGN OF THE 8T FULL ADDER

The post layout simulation of proposed eight transistor full adder has been carried out with all combinations of inputs. The output waveforms show small voltage degradation for some input combinations. However these degradations can be minimized by use of CMOS inverters as level restorers at appropriate places in the circuit [20,25]. Such type of level restoring logic is required in a long cascading chain of adders so that the penalty paid in silicon area for introducing two transistors of the CMOS inverter is minimal.

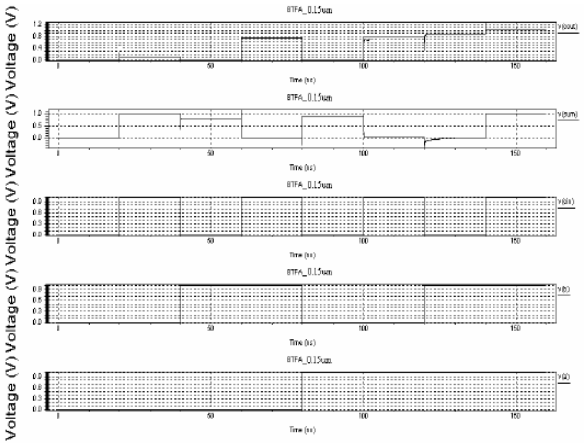


Fig. 8 simulation results of the eight transistor full adder

The layout of the proposed 8T full adder is shown below

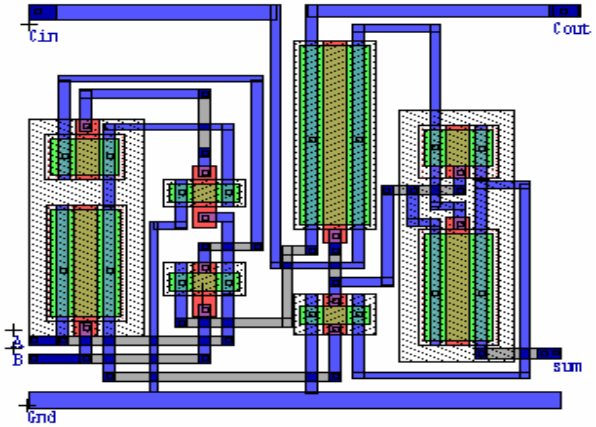


Fig. 9 Layout design of the proposed 8T full adder

6. CONCLUSION

The current work proposes the design of an 8T full adder, which is by far the full adder with the lowest transistor count. In designing the proposed 8T full adder, a novel 3T XOR gate has also been proposed. The noise margins of the proposed XOR gate has been studied and found to have quite acceptable values. The proposed XOR gate also has a much less delay and hence much less power delay-product than its peer designs. Using the XOR gate an eight-transistor adder has been realized using the conventional the equations of the full adder circuit. The designed adder is found to give better performance than most of the adders mentioned in literature so far as the power-delay product is concerned. The layout of the proposed full adder has also been designed and simulated. The proposed full adder can operate at low voltages, yet giving quite a good speed.

7. RFERENCES

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