Carry Speculative Adder with Variable Latency for Low Power VLSI

Subhashinee A.
Department of Electronics and Communication Engineering
K S Rangasamy College of Technology
Tiruchengode, India

Rajasekaran C.
Department of Electronics and Communication Engineering
K S Rangasamy College of Technology
Tiruchengode, India

ABSTRACT
Arithmetic logic units and digital signal processors widely uses adders. It is the most complicated arithmetic circuits in digital electronics. The existing adders suffer from critical path delay, area overhead and power consumption. Speculative adders are designed with variable latency that combines speculation technique along with correction methodology to attain high performance in terms of low area overhead over the existing adders. In speculative adders the sum and carry generation part is separated to reduce the area overhead. Carry Speculative Adder (CSPA) uses carry predictor circuit to reduce power consumption and to reduce the computational time and it uses error recognition and error correction circuit to detect the fault occurred in the partial sum generator and to recover it to get accurate results. CSPA circuit provides error free output so that it can be used in many digital applications. This speculative adder can reduce the delay upto 11.88 %.

Keywords
Speculative Adder, Variable Latency, Error Detection, Error Correction

1. INTRODUCTION
In electronics, addition of the binary numbers in various computers and other types of processors are performed by the adders. Adder circuits are used in various processors for calculating increment or decrement operations, table indices, addresses etc. The different formats like XS-3, Binary Coded Decimal (BCD) and gray code can be added using the adder circuits. Adder found wide range of applications in many fields and for many operations such as decoding, calculation etc. The critical path is not often activated in traditional adders, based on this observation speculative adders have been designed. Traditional adders depend on its previous values for its each output [1]. Particularly, the MSB of the sum depends on all the n bit previous outputs, where n is the block adder width. As the width of block adder increases, there will be an error growth. The error grows linearly with n. There will be a large area and large fanout at the primary inputs due to this error. Speculative adders can overcome the area problem but it has high error rate [2], [3]. For this error tolerant variable latency adder is design upon the speculative adder [4]. This variable latency adder consist of error recognition and correction circuit, which can overcome the high error rate and this design helps the speculative adder to use in many applications such as image and signal processing etc [5].

2. SPECULATIVE CARRY SELECT ADDER
Carry chain in the addition process is observed for the design of speculative carry select addition (SCSA) [6], [7]. The carry chain is observed because the long carry chain is rarely activated in the block adders. To overcome this problem, in SCSA the input bits are divided into two parts of equal sizes [8], [9]. A group of consecutive input bits are given as a input to a single block adder. A block adder is known as the window, the number of consecutive input bits is known as window size and it is The proposed speculative adder can be able to complete the addition process quickly when compared to the existing technique.

2.1 Speculative Adder
Speculative addition is widely used in asynchronous design. The speculative addition involves two cycles [7]. In the first cycle, the addition process is done and the end result is assumed as accurate sum. Meanwhile, a parallel carry propagation circuit checks whether the operation uses the carry long path known as the critical path. If it uses the longest path the system requires the additional clock cycle to complete the addition process. If it didn't use the longest path, bypass logic is used to reduce the clock cycle required. The block diagram of CSPA is shown in Figure 1.Assume the a, b are the two inputs then the (P/G) signal known as (PROPAGATE/GENERATE) is defined as

$$P_i=a_i \wedge b_i$$

$$G_i=a_i b_i$$

Then the sum and carry can be written as

$$S_i=P_i \wedge C_{i-1}$$

$$C_i=G_i+P_i C_{i-1}$$

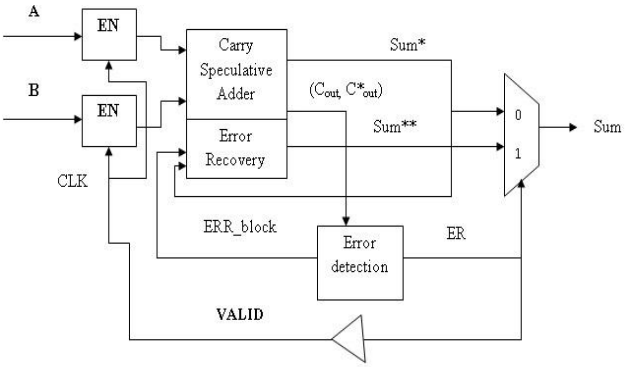

Fig 1: Block Diagram for Carry Speculative Adder

The carry speculative adder uses bits close to the MSB to predict the carry. By doing so, the time consumption for addition process is reduced.

2.2 Error Detection and Recovery
The carry prediction circuit may cause errors while predicting the carry [8]. In the existing speculative adder there is no error detection and error correction circuit. In this carry speculative adder, it has an additional block called error detection and error

recovery. In error detection circuit it uses EX-OR operation to find the error.

2.3 Error Analysis

There are two possible cases of errors.

Case (i)

Pix −1:x−k = 1 and Gi x−k−1:0 = 1,

Case (ii)

Px−1:0 = 1 and Gi−1 x−1:x−k = 1,

In case (i), Pix −1:x−k = 1 says that Gx−1:x−k=0. Ci∗ out of the ith block adder is recognized as incorrect. The carry out bit is corrected by using the following equation,

Ciout = Gix−1:x−k + Pix−1:x−kGix−k−1:0 + Pix−k−1:0Ci−1out

In case (ii), Pix −k−1:0 = 1 says that

Gi x−k−1:0 = 0.

This shows that the ith block adder output is 0. The correct carry out bit is calculated using the following equation,

Ci out = Gi x−1:0 + Pix −1:0Ci−1 out

The major advantage is that the error detection circuit can find which block adder prediction is wrong. By this advantage the work of the recovery circuit is simplified. The recovery circuit rectifies the affected block adder and corrects the output so that the output sum is accurate. This circuit is designed using variable latency design, so that if an addition process is completed it send a valid signal to the input side to fetch another set of inputs to perform addition. This will greatly reduce the time consumption

3. RESULTS AND DISCUSSIONS

Every block in the carry speculative adder is designed and simulated using Xilinx ISE. The simulation result is shown in figure 2. Here the existing and the proposed method are compared in terms of are, power and delay.

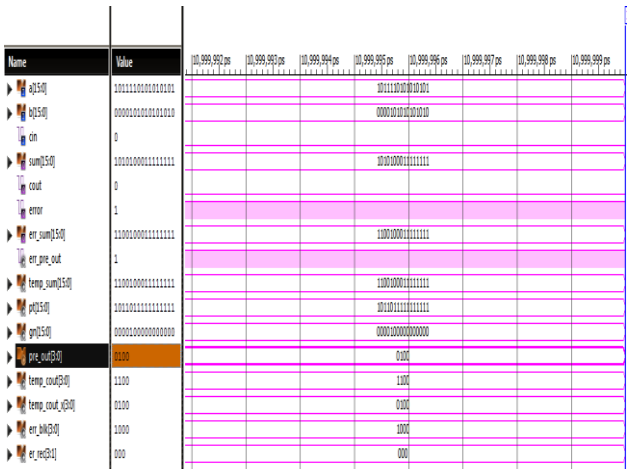

Fig 2: Simulation Output for Carry Speculative Adder

Table 1: Comparison of SCSA and CSPA

ADDER TYPE	TOTAL No. OF GATES USED	DELAY (ns)	POWER (mW)
SPCA-16 BIT	654	26.725	112
CSPA-16 BIT	502	18.259	89
MODIFIED CSPA-16 BIT	342	16.599	72
MODIFIED CSPA-32 BIT	1,158	45.125	73

The Table 1 shows the comparison of SCSA and the proposed CSPA. This tabular column clearly shows that the proposed CSPA has low power consumption and lower delay.

The Table 2 shows the error rate for different design in SCSA and CSPA. The SCSA I is the original speculative adder. The SCSA IM has the lesser block adder than the SCSA I. The CSPA I is the original design with error detection and correction circuit. The CSPA II has the less block adder than SCSA I.

Table 2: Error Rate Analysis

		Block adder size (No. of Block adders)	Error rate Adder width=16
SCSA I		4(4)	0.06%
SCSA IM	8-bit	4(4)	1.05%
	9-bit		0.82%
	10-bit		0.57%
	11-bit		0.33%
SCSA II		2(8)	3.55%
CSPA I	8-bit	3(6)	1.49%
	9-bit		0.73%
	10-bit		0.41%
	11-bit		0.16%
CSPA II	8-bit	2(6)	0.97%
	9-bit		0.68%
	10-bit		0.09%
	11-bit		0.05%

4. CONCLUSION

A variable latency adder that combines the speculative adder with error recognition and correction for unsigned random inputs, called variable latency carry speculation adder. The sum and carry generator are separated in CSPA and thus the carry signal and partial sum bit can be calculated faster. Carry predictor circuit of the block adder only uses the input bits near the MSB to predict the carryout bit. The hardware cost of the prediction circuit is reduced and the CSPA has minimal error rate increase. The proposed error detection circuit indicates which block adder produced an incorrect carry-out bit, and the error recovery circuit only focuses on recovering the block adders with incorrect partial sum bits. On comparing CSPA and SCSA, CSPA reduces 11.88% delay and also reduces computational complexity upto 11.38%.

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